Solid State Detectors

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Semi-Conductor based Detectors

- Materials and their properties
- Energy bands and electronic structure
- Charge transport and conductivity
- Boundaries: the p-n junction
- Charge collection, and signal generation.
- Energy and time resolution
- Radiation damage
- Other systems

Recap

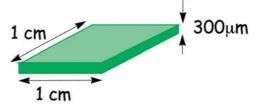
Charge Carrier Density

Thermally activated charge carriers in the conduction band Their density is given by

$$n_i = \sqrt{n_V n_C} \exp\left(-\frac{E_G}{2k_B T}\right) = 1.5 \times 10^{10} \,\mathrm{cm}^{-3}$$

at room temperature

In a typical Si detector volume one obtains 4.5×10^8 free carriers compared to 3.2×10^4 e-h pairs for MIP



For a detection of such an event, the number of free carriers has to be substantially reduced.

This can be achieved via

- a) cooling
- b) pn-junction in reverse bias

The p-n junction (1)

Donor region and acceptor region adjoin each other:



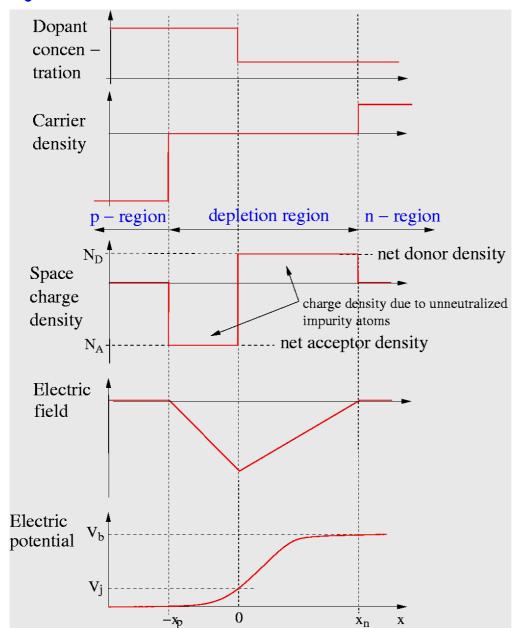
Thermal diffusion drives holes and electrons across the junction

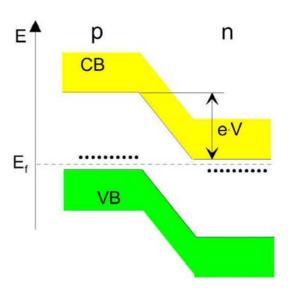
Electrons diffuse from the n- to the p-region, leaving a net positive space charge in the n-region and building up a potential (similar process for the holes)

The diffusion depth is limited when the space charge potential energy exceeds the energy for thermal diffusion

Due to preparation conditions (implantation), the p-n junction is often highly asymmetric

The p-n junction (2)





Depletion width of the p-n junction in reverse bias

Bias voltage:
$$V_b = \frac{q_e}{2\epsilon} (N_d x_n^2 + N_a x_p^2)$$

Charge neutrality:
$$N_d x_n = N_a x_p$$

Both equations can be solved for x_p and x_n , resulting in the following expression for the depletion width:

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon V_b}{q_e} \frac{N_a + N_d}{N_a N_d}}$$

If, for example, $N_a \gg N_d$, this expression simplifies to

$$W \approx x_n = \sqrt{\frac{2\varepsilon V_b}{q_e N_d}}$$

Depletion width and capacitance of the p-n junction

The doping concentration is commonly expressed in terms of the resistivity ρ :

$$\rho = (\mu q_e N)^{-1}$$

 μ is the charge mobility, that expresses the relation between applied field and carrier velocity. Then the depletion width is given by :

$$W = \sqrt{2\varepsilon\mu_n \rho_n V_b}$$

The depleted junction volume is free of mobile charge. This means, it forms a capacitor, bounded by the conducting p- and n-type semiconductors on each side

The capacitance is:

$$C = \varepsilon \, \frac{A}{W} = A \sqrt{\frac{\varepsilon \, q_e \, N}{2V_b}}$$

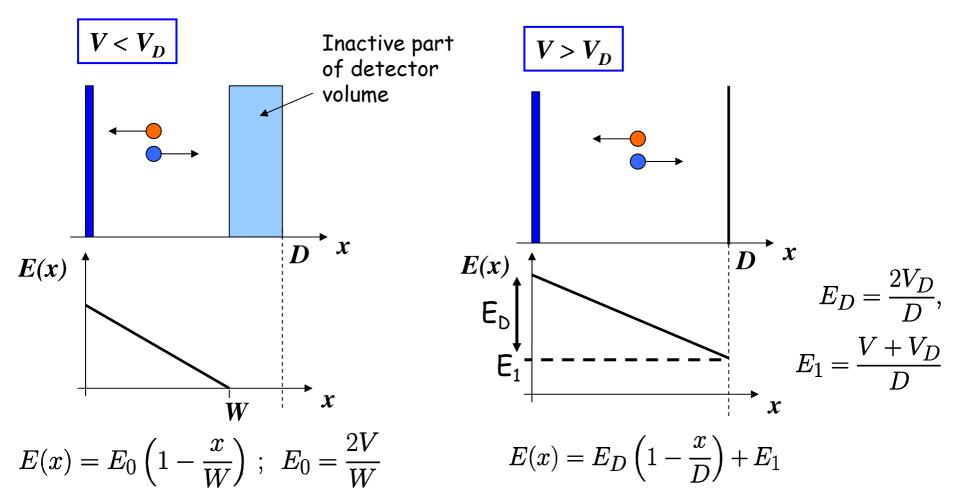
Charge collection (2)

A characteristic quantity is the voltage required to reach total

depletion of a diode of width D:

$$V_D = \frac{q_e N_d W^2}{2\epsilon}$$

One distinguishes two cases:



Charge collection (3)

The local velocity of a charge carrier is given by:

$$v(x) = \mu E(x)$$
 $\mu = mobility$

v(x) does not depend on the time during which the charge carrier is accelerated, as in normal ballistic motion.

The carriers are always in quilibrium with the crystal lattice, because characteristic times for phonon excitation are much smaller than transport times.

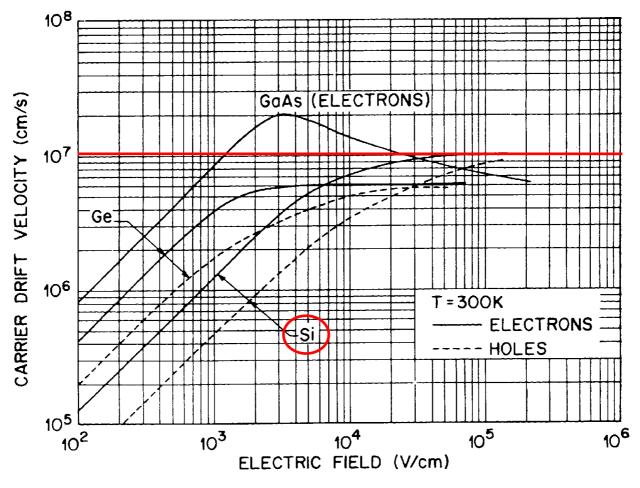
The carrier velocity is only a function of the electric field at every position in the depletion volume.

In Si at 300 K:

$$\mu$$
(electrons) = 1350 cm²/Vs μ (holes) = 480 cm²/Vs (valid at low fields E < 10⁴ V/cm)

The mobility is constant up to about 10⁴ V/cm. Beyond that value increased phonon emission reduces the energy going into electron motion, i.e., the mobility decreases

At high fields (E > 10^5 V/cm): constant drift velocity ~ 10^7 cm/s



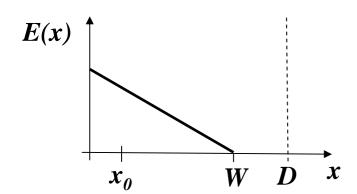
from Sze, Physics of Semiconductor Devices

Charge collection (4)

The time required for a charge originating at x_0 to reach a point x is given by:

$$t(x) = \int_{x_0}^{x} \frac{1}{v(x)} \, dx$$

Solution for $V < V_D$ (partial depletion)



$$t(x_0) = \tau_p \ln\left(\frac{W}{W - x_0}\right)$$
 $\tau_p = \frac{\epsilon}{\mu_p \, q_e \, N_d}$

$$au_p = rac{c}{\mu_p \, q_e \, N_d}$$

$$x(t) = W \left[1 - \exp(-t/\tau_n) \right]$$

(Relaxation time)

In n-type Si with a resistivity of 10 k Ω cm :

 $\tau_{\rm n}$ = 10.5 ns and $\tau_{\rm p}$ = 31.5 ns

A charge drifting towards the lowfield region is never collected

Criterion:
$$x_0 = 0.95 \text{ W} \longrightarrow$$

$$t_{c,n}$$
 = 30 ns, $t_{c,p}$ = 90 ns

Charge collection (5)

The collection time can be reduced by operating the detector at bias voltages exceeding the depletion voltage

Solution for $V > V_D$ (full depletion)

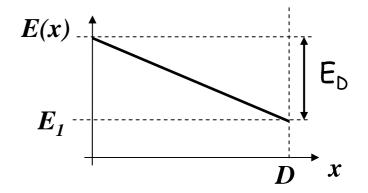
$$t(x) = \frac{D}{\mu E_D} \ln \left(\frac{E(x)}{E(x_0)} \right)$$

For holes originating at $x_0 = D$ and drifting to the p-electrode at x = 0:

$$t_{c,p} = \frac{D}{\mu_p E_D} \ln \left(1 + \frac{E_D}{E_1} \right)$$

For electrons originating at $x_0 = 0$ and drifting to the n-electrode at x = D:

$$t_{c,n} = \frac{D}{\mu_n E_D} \ln \left(1 + \frac{E_D}{E_1} \right)$$



For large overbias ($E_1 >> E_D$)

$$\ln(1 + \frac{E_D}{E_1}) \approx \frac{E_D}{E_1}$$

$$t_{c,np} = \frac{D}{\mu_{n,p} E_1}$$

Signal Generation

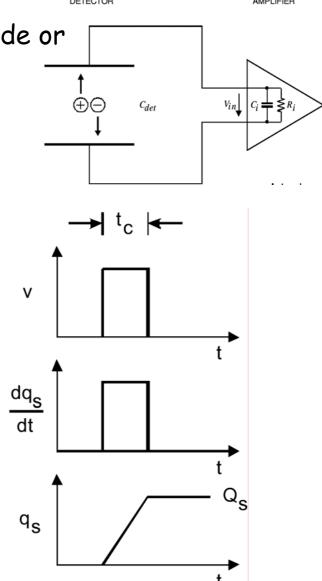
When does the signal current begin?

- a) when the charge reaches the electrode or
- b) when the charge begins to move?

When a charge pair is created, both the positive and the negative charges couple to the electrodes

- induction of mirror charges of equal magnitude
- negative current at the positive electrode and a positive current at the negative electrode

Although electrons and holes move in opposite directions, their contribution to the signal current is of the same polarity



Time Resolution

Advantage of semiconductor diodes: High velocity of charge carriers

The longest drift time of the carriers determines the maximum frequency at which the diode can be operated.

$$t_{\rm m} = D/(10^7 \text{ cm/s}) = 1 \text{ ns for } D = 100 \text{ }\mu\text{m}$$

The time resolution is determined by the variation of the drift velocities within the detector, as caused by different loci of absorption.

The shortest drift time is observed for generation of the carriers in the center of the depletion volume

The maximum time resolution is a factor of two better than the longest drift time

Steps in the Fabrication of Planar Silicon Diode Detectors

Polishing and cleaning

n - Si 🗕 n-Si wafer

Oxidation at 1300 K

OXIDE PASSIVATION

Deposition of photosensitive polymer, UV illumination

OPENING OF WINDOWS

Creation of p-n junction via implantation/diffusion

DOPING BY ION IMPLATATION

B : 15 keV 5 x 10¹⁶ cm⁻² As : 30 keV 5 x 10¹⁵ cm⁻²

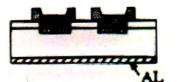
Annealing: implanted ions occupy lattice sites

ANNEALING AT 600 °C, 30 MIN

Deposition of Al and

AL METALLIZATION

patterning for electric contacts



AL PATTERNING AT THE FRONT

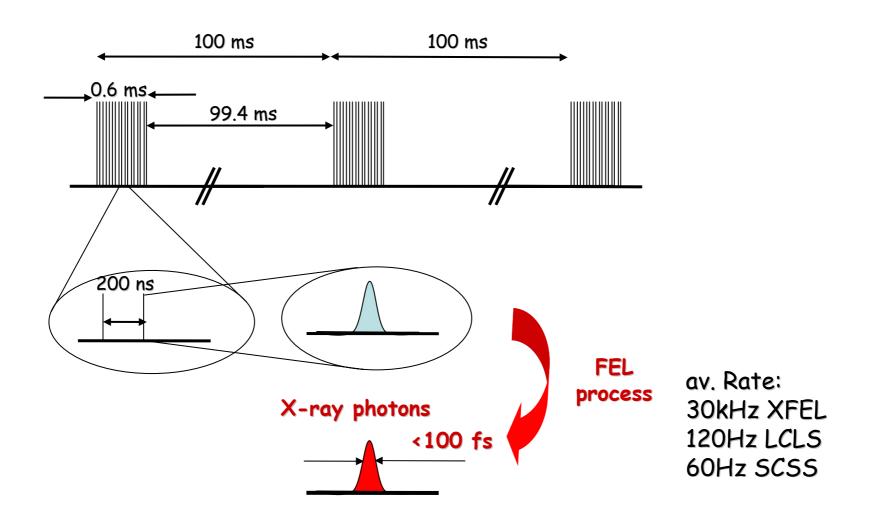
AL - REAR CONTACT

An Example: The AGIPD Detector for XFEL

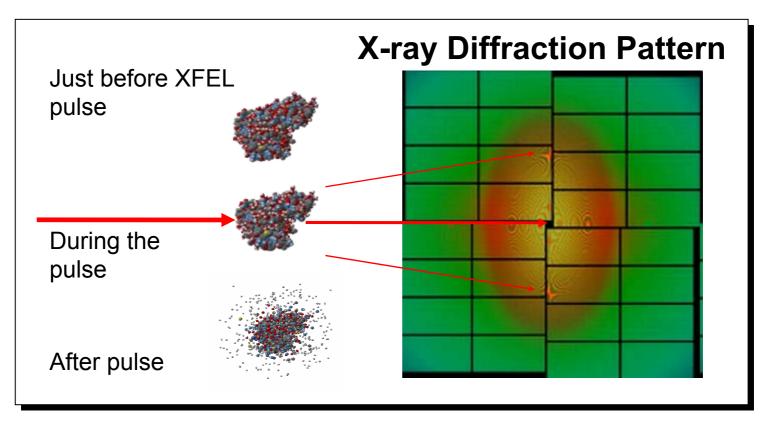


http://hasylab.desy.de/science/developments/detectors/index_eng.html

European XFEL Time Structure



Single Molecule Imaging



Henry Chapman, <u>Guillaume Potdevin</u>, <u>DESY</u> Janos Hajdu, <u>Uppsala University and Stanford</u>

XFEL Detector Requirements

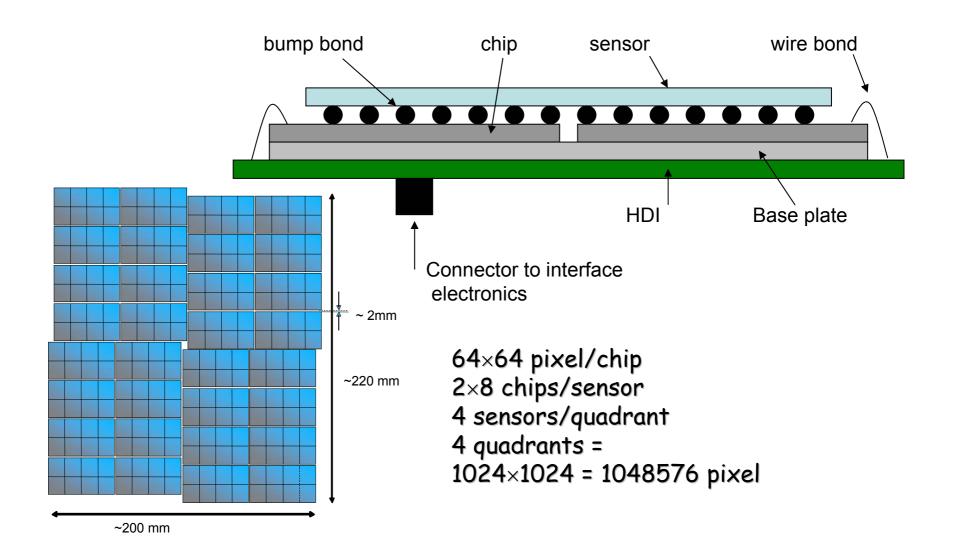
		PPnX	PPX	CDI	SPI	XPCS
•Energy 0.815keV	E (keV)	6–15	12	0.8-12	12.4	6 – 15
·No energy resolution—	∆E/E	No	No	No	No	No
	QE	>0.8	>0.8	>0.8	>0.8	>0.8
·High efficiency (>0.8)	Rad Tol	10 ¹⁶ ph	10 ¹⁶ ph	2×10 ¹⁶ ph	2×10 ¹⁵ ph	2 10 ¹⁴ ph
·High dose 1GGy/3a	Size	200 deg	120 deg	120 deg	120 deg	0.2 deg
•	Pixel	7 mrad	100 μm	0.1 mrad	0.5 mrad	4 μrad
·Low dead area <10% —	# pixels	500 × 500	$3k \times 3k$	20k × 20k	$4k \times 4k$	1k × 1k
·High dynamic range	tiling	<20%	<10%	See text		<20%
	L Rate	5×10 ⁴	3×10 ⁶	10 ⁵	10 ⁴	10 ³
XFEL Timing compliant	G Rate	3 x10 ⁷	10 ⁷	10 ⁷	10 ⁷	10 ⁶
·Low noise (<1 ph)	Timing	10Hz	10Hz	5MHz	10Hz	5MHz
	Flat F	1%	1%	1%	1%	1%
·Low crosstalk	Dark C	<1 ph	<1 ph	<1 ph	<1 ph	<1 ph
·Vacuum compatible	R Noise	<1 ph	<1 ph	<1 ph	<1 ph	<1 ph
	Linearity	1%	1%	1%	1%	1%
·Central hole	PSF	1 pixel	100 μm	1 pixel	1 pixel	1 pixel
	Lag	10 ⁻³	10^{-3}	7×10 ⁻⁵	10 ⁻³	10 ⁻³
	Vacuum	No	No	Yes	Yes	No
	Other	Hole	Hole			Hole

AGIPD Target Specs

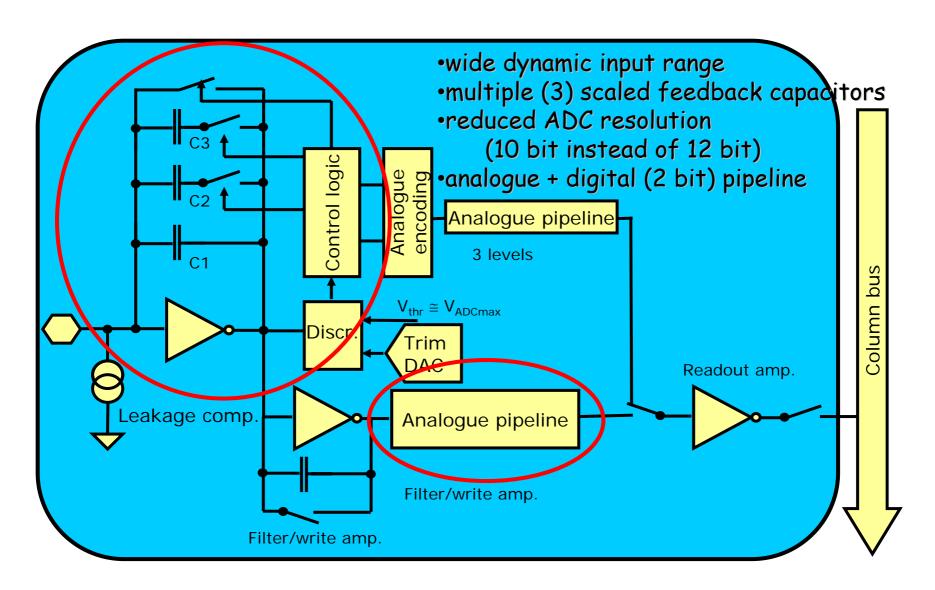
Basic parameters

- •1 Megapixel detector $(1k \times 1k)$
- •200 μ m × 200 μ m pixels
- Flat detector
- Sensor: Silicon 128 x 256 pixel tiles
- Single shot 2D-imaging
- •5MHz frame rate
- $\cdot 2 \times 10^4$ photons dynamic range
- Adaptive gain switching
- Single photon sensitivity at 12keV
- •Noise $\leq 150e$ (50 × 10⁻³ photons @ 12keV)
- •Storage depth ≥200 images
- Analogue readout between bunch-trains

The AGIPD Detector



AGIPD Pixel



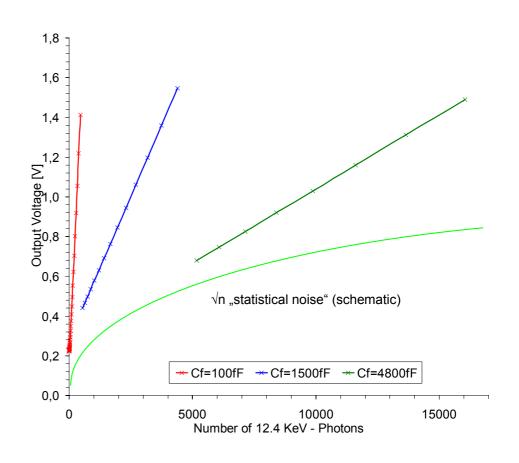
AGIPD Dynamic Range

Integrator gain requirements:

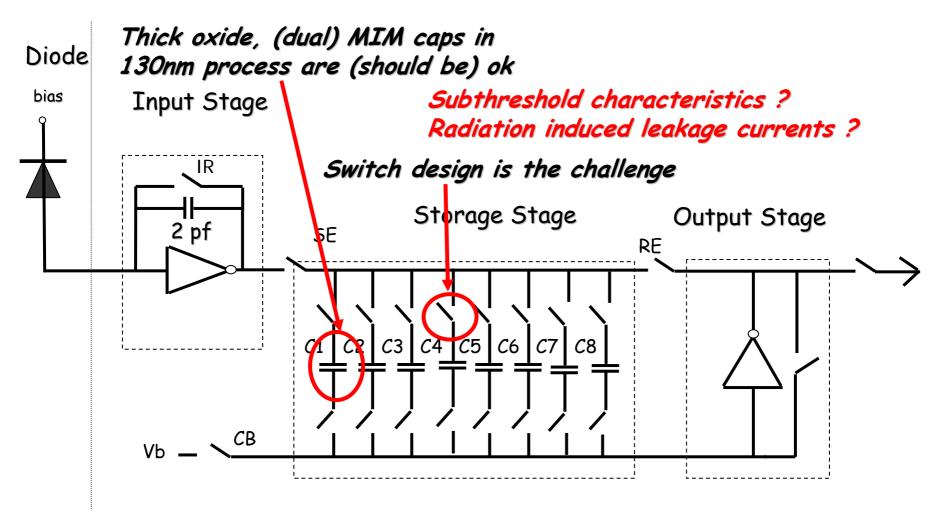
- Effective analogue resolution ≥ 8 bit
- Analogue resolution always better than "statistical noise" √n_{ph}
- maximum signal ≥ 10⁴ photons

range	norm. gain	Cf [fF]	max n _{ph}
1	1	100	256
2	1/16	1600	4096
3	1/64	6400	16384

Adaptive gain switching
Tested on a Si-strip readout chip
@ PSI by A.Mozzanica



100msec "loss free" Charge Storage



Radiation Damage in Silicon Detectors

Two basic radiation damage mechanisms:

Displacement damage

Incident radiation displaces silicon atoms from their lattice sites

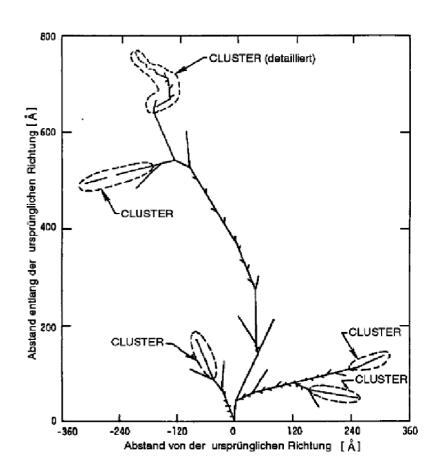
Creation of defect clusters

Depends on the non-ionizing energy loss, specific for particle type and energy

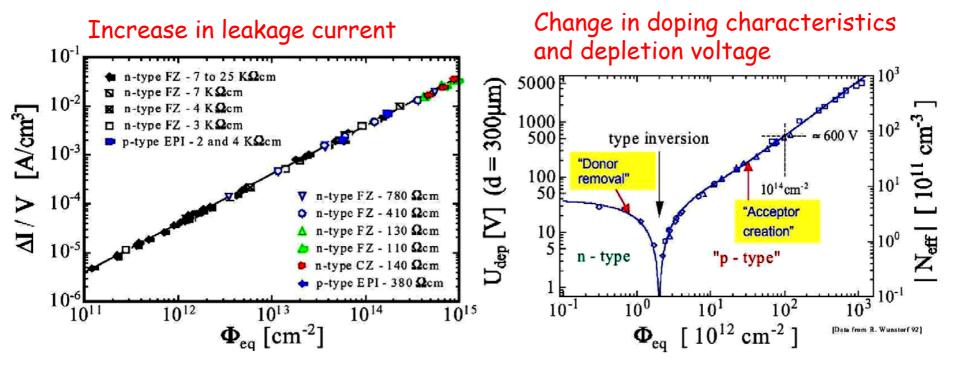
Ionization damage

Energy absorbed in insulating layers liberates charge carriers which diffuse or drift to other locations where they are trapped

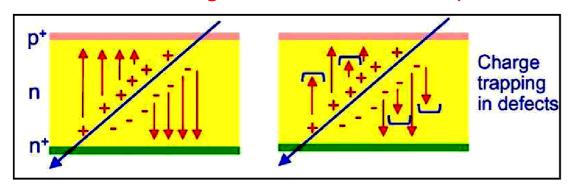
Depends primarily on the absorbed energy, independent on the type of radiation



Consequences of Radiation Damage



Decrease of charge collection efficiency



Mitigation techniques

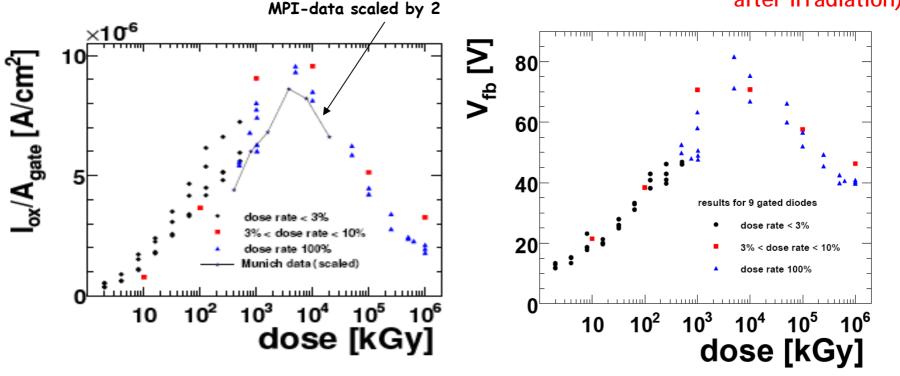
- Devices with higher depletion voltages
- Cooling
- Special structures

Summary Radiation Damage



1. Summary of radiation damage measurements and parameter extraction for simulation (from gated diode measurements)

Surface generation current vs dose + "Flat-band voltage" vs dose (immediately after irradiation)



→ V_{fb} [N_{Ox}+N_{it}] and I_{Ox} [N_{it}] reach maximum at few MGy - then decrease (tentative conclusion: decrease due to N_{it} at high doses - reason not clear)

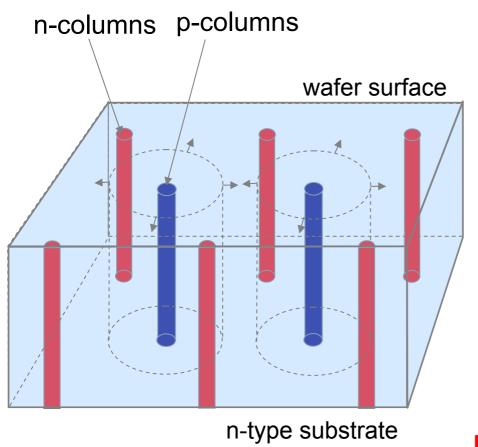
Summary Radiation Damage



- → Impact of parameters on sensor performance
 - 1. N_{ox}^{fix} fixed positive oxide charges \leftarrow shift of ideal CMOS-C/V-curve
 - → accumulation layer below oxide
 - → strong electric fields causing breakdown
 - 2. N_{Ox}^{mob} mobile oxide charges (close to interface) \leftarrow hysteresis C/V-curve
 - → same effects as above; dependence on time + surface potential!
 - 3. D_{it} interface traps (integral N_{it}) \leftarrow TSC (Thermally Stimulated Current)
 - → current generation, if interface is exposed to E-field
 - → contribution to surface charge density depends on
 - position of Fermi level
 - type of states
 - → acceptors compensate positive oxide charges
 - → donors enhance effect of positive oxide charges
 - → reliable simulation is not a simple task!

"Standard" 3D detectors - concept

Proposed by Parker et al. NIMA395 (1997)



ionizing particle

Short distance between electrodes:

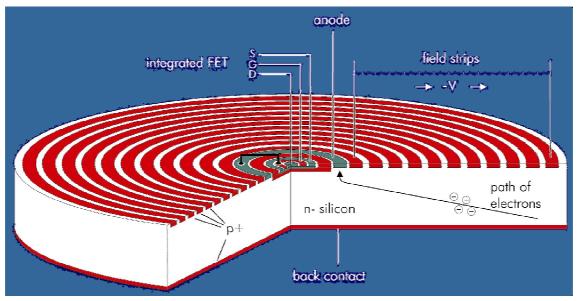
- low full depletion voltage
- short collection distance



more radiation tolerant than planar detectors!!

Some other Si-based detectors

A) The Silicon Drift Detector (SDD)

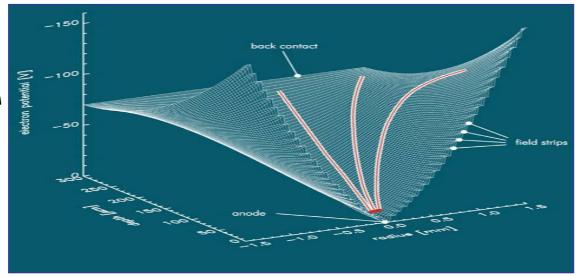


SDD with integrated SSJFET

time to drift from device edge to readout node:

 $\Delta t = \Delta \times v$

= $\triangle \times / \mu E$ = 200 ns for $\triangle r = 2 \text{ mm}$ i.e. $A = 13 \text{ mm}^2$ and E = 800 V / cm



Electrical
Potential in
a circular SDD

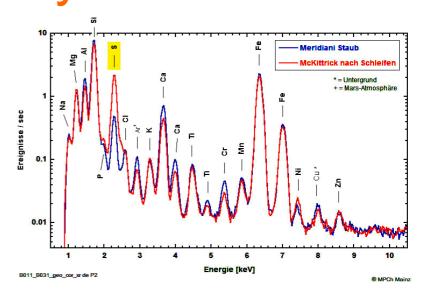
Advantages SDD's:

- Very small capacitance of readout node → very low noise possible → good energy resolving power, and good at low energies.
- Large detection volume possible; fully depleted silicon (>300 micron thick)
 → good for high energies.
- Back illuminated

 radiation resistant

SDDs on Mars Explorers Spirit and Opportunity





The APXS system of the MPICH in Mainz:

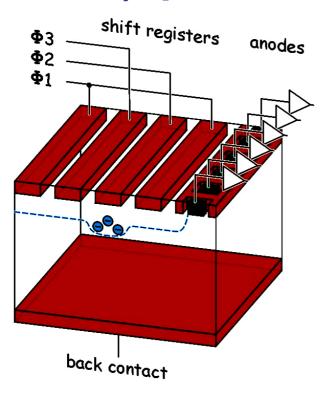
Excitation with Curium-244:

α – particles X – rays

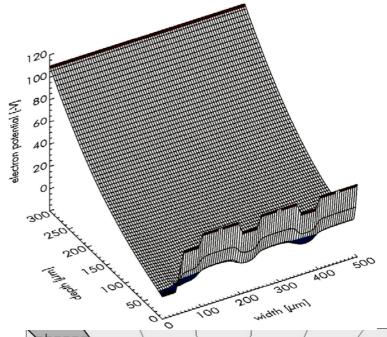
ΔE @ Spirit&Opportunity @ 1.5 keV: 80 eV ΔE @ Pathfinder @ 1.5 keV: 280 eV

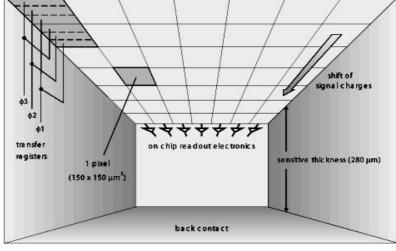
Barnacle Bill Martian Rock

b) pnCCD basics



- full depletion (50 μm to 500 μm)
- back side illumination
- radiation hardness
- · high readout speed
- pixel sizes from 36 μm to 650 μm
- charge handling: more than 10⁶ e⁻/pixel
- high quantum efficiency





How many charges can be stored in one pixel?

What determines the charge handling capacity in a pixel?

pixel volume:

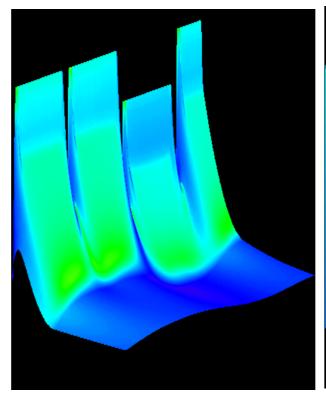
 $20 \times 40 \times 12 \ \mu \text{m}^3 \approx 1 \times 10^4 \mu \text{m}^3$

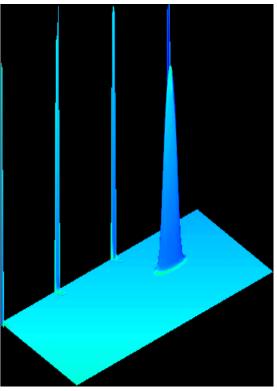
Doping: $10^2 P$ per μm^3

CHC = 1×10^6 per pixel

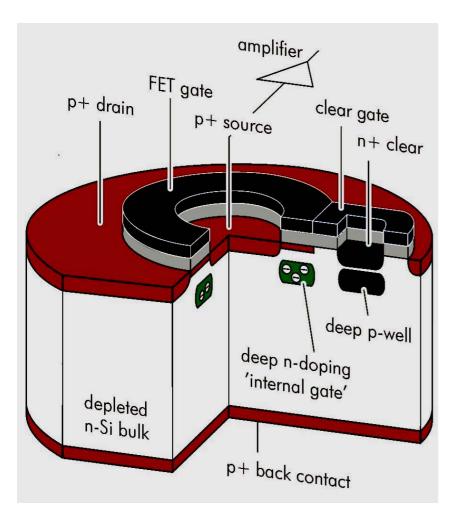
can be increased by external voltages

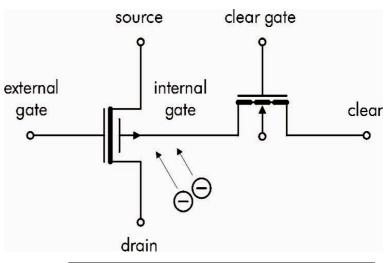
can be increased by doping

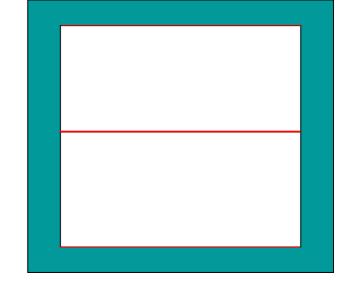




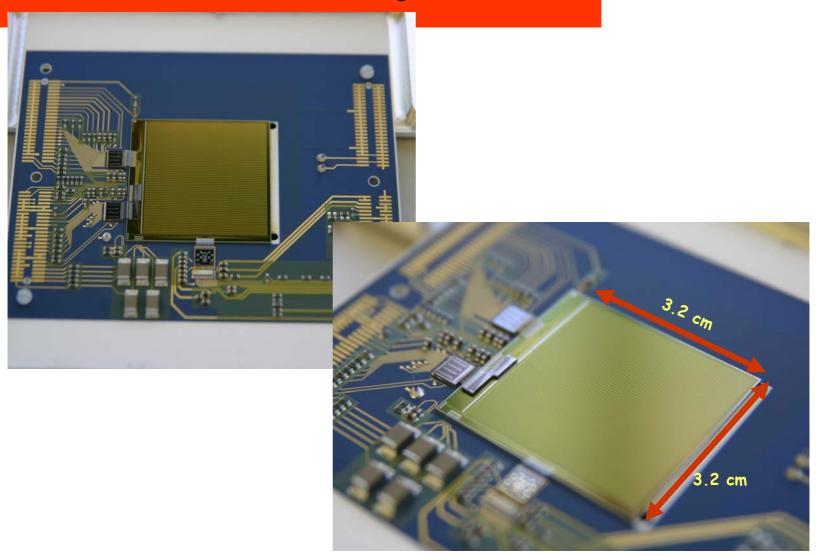
c) Circular DEPMOSFET pixels







SIMBOL-X-Hybrid



8.2 cm

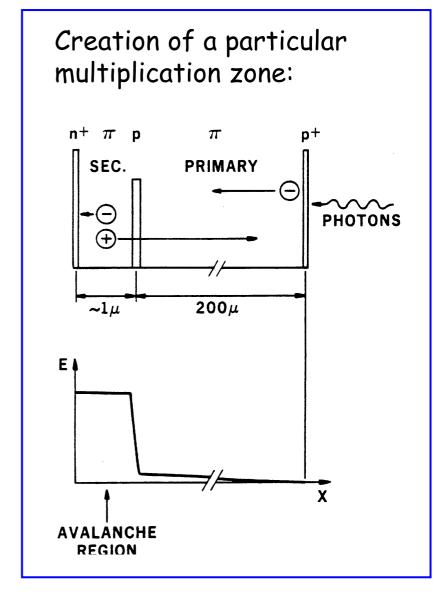
d) Avalanche Photodiodes

Solid state detectors with internal amplification (c.f. proportional counter)

Charge carriers are accelerated sufficiently to form additional electronhole pairs

Photon — d

An electron-hole pair is created on the left by incident light



Under the influence of the electric field the electron drifts and gains sufficient energy for ionization, i.e., formation of n additional electron-hole pair

The gain of this process is

$$G_n = e^{\alpha_n d}$$

where the electron ionization coefficient

$$\alpha_n = \alpha_{n0} e^{-E_n/|E|}$$

is a function of the electric field. The parameters α_{n0} and E_n are material constants

The secondary hole can also ionize and form additional electron-hole pairs.

The combined multiplication of electrons and holes leads to a sustained avalanche.

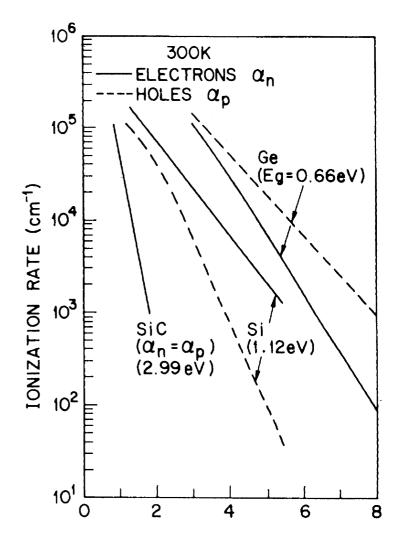
In Si the ratio of electron to hole ionization coefficients is strongly different and field dependent:

$$\frac{\alpha_n}{\alpha_p} = 0.15 \cdot \exp\left(\frac{1.15 \cdot 10^6}{|E|}\right)$$

Amplification depends on position:

$$M(x) \sim \exp[(\alpha_n - \alpha_p) x]$$

Exponential dependence only when $\alpha_n \neq \alpha_p$



- The ratio of the ionization rates should be strongly different from unity
- Only carriers with higher ratio into the avalanche zone

This leads to the following limits of gain and detector thickness vs. electric field:

Electric field	Gain	Thickness	Voltage
$E=$ 2 $^{\cdot}$ 10 5 V/cm	$G_n = 2.2 \cdot 10^3$	$d=$ 520 μ m	$V_b =$ 10 kV
E = 3 ·10 5 V/cm	G_n = 50	d = 5 μ m	V_b = 150 V
E = 4 ·10 5 V/cm	$G_n = 6.5$	d = 0.5 μ m	$V_b =$ 20 V
E = 5 ·10 5 V/cm	G_n = 2.8	$d=$ 0.1 μ m	$V_b =$ 5 V

To achieve gains in the range of 100 - 1000 requires:

- 1) A depletion region of several 100 μm
- 2) Bias voltages in the range 500 1000 V
- 3) Excellent control of the electric field distribution

Properties of APDs

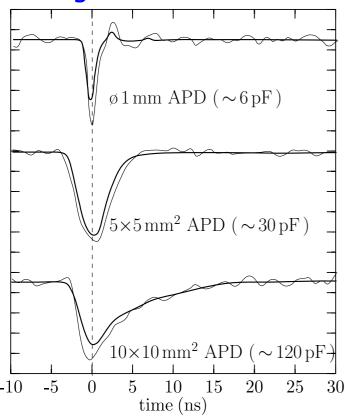
Very high electric fields: Short transit times of charge carriers

Short pulse rise times of a few ns, time resolution < 1 ns

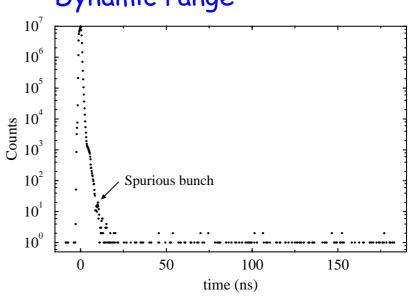
Statistical fluctuations in the avalanche process

Poor energy resolution

Timing



Dynamic range



Single-photon counting with signal/noise ratio of > 10⁷

A.Q.R. Baron et al., NIMA 400, 124 (1997)

Germanium Detectors for γ - spectroscopy

Advantage of Ge: Low bandgap (0.7 eV) \rightarrow high energy resolution

Disadvantage of pn-junction semiconductor detectors: Relatively

insensitive to highly penetrating radiation

Limit determined by depletion depth

Solutions: Reducing N_d via

A) High-purity material (HPGe)

For N_d = 10¹⁰ atoms/cm³ a depletion depth of 10 mm can be reached for V_b < 1000 V

B) Compensation by doping: Ge(Li)

Lithium ion drifting after growth of the crystal, Li as interstitial donor atom

 $D = \sqrt{\frac{2\varepsilon V_b}{q_e N_d}}$

 V_b : reverse bias voltage

 N_d : net impurity concentr.

 ϵ : dielectric constant

 q_e : electronic charge

For Si detectors only Li drifting possible, because maximum purity less than Ge Operation of Ge detectors always at low temperatures, because of thermally induced leakage current

Ge(Li) detectors have to be kept at cryogenic temperatures (LN₂, T = 77 K) all time, otherwise a detrimental redistribution of the drifted Li would result

HPGe detectors can be warmed to room temperature between uses.

Ge detectors are fitted with an interlock to prevent the application of high voltage at room temperature: Otherwise the high leakage current would destroy the input FET of the preamp.

Since the FET is normally mounted inside the cryostat for cooling, ist replacement is not routine