X-ray Radiation Damage Studies and Design of a Silicon Pixel Sensor for Science at the XFEL

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Abstract

Experiments at the European X-ray Free Electron Laser (XFEL) require silicon pixel sensors which can withstand X-ray doses up to 1 GGy. For the investigation of X-ray radiation damage up to these high doses, MOS capacitors and gate-controlled diodes built on high resistivity n-doped silicon with crystal orientations <100> and <111> produced by four vendors, CiS, Hamamatsu, Canberra and Sintef, have been irradiated with 12 keV X-rays at the DESY DORIS III synchrotron-light source. Using capacitance/conductance-voltage, current-voltage and thermal dielectric relaxation current measurements, the densities of oxide charges and interface traps at the Si-SiO_2 interface, and the surface-current densities have been determined as function of dose. Results indicate that the dose dependence of the oxide-charge density, the interface-trap density and the surface-current density depend on the crystal orientation and producer.

In addition, the influence of the voltage applied to the gates of the MOS capacitor and the gate-controlled diode during X-ray irradiation on the oxide-charge density, the interface-trap density and the surface-current density has been investigated at doses of 100 kGy and 100 MGy. It is found that both strongly depend on the gate voltage if the electric field in the oxide points from the surface of the SiO_2 to the Si-SiO_2 interface.

To verify the long-term stability of irradiated silicon sensors, annealing studies have been performed at 60 °C and 80 °C on MOS capacitors and gate-controlled diodes irradiated to 5 MGy as well, and the annealing kinetics of oxide charges and surface current were determined.

Moreover, the macroscopic electrical properties of segmented sensors have slao been investigated as function of dose. It is found that the defects introduced by X-rays increase the full depletion voltage, the surface leakage current and the inter-electrode capacitance of the segmented sensor. An electron-accumulation layer at the Si-SiO_2 interface is observed. Its width increases with dose and decreases with applied bias voltage. The electron-accumulation layer is relevant for the change of the electrical properties of segmented sensors.

Finally, according to the optimum parameters of silicon pixel sensors from TCAD simulations taking the damage-related parameters into account, a radiation-hard silicon pixel sensor for the AGIPD Project has been designed.

Kurzfassung

Die an dem *European X-ray Free Electron Laser* (XFEL) geplanten Experimente werden Silizium-Pixel-Sensoren erfordern, die Röntgen-Dosen bis zu 1 GGy standhalten können. Für die Untersuchung der Strahlenschäden bei solch hohen Dosen wurden MOS-Kondensatoren sowie Gate-gesteuerte Dioden mit 12 keV Röntgenstrahlen der DESY DORIS-III Synchrotronquelle bestrahlt. Die verwendeten Strukturen wurden auf n-dotiertem Silizium mit hohem Widerstandswert und mit den Kristallorientierungen <100> sowie <111> von vier verschiedenen Herstellern gefertigt (CiS, Hamamatsu, Canberra und Sintef). Mit Hilfe von Messungen der Kapazität, der Konduktivität und des Stroms als Funktion der angelegten Spannung, sowie TDRC-Messungen (*Thermal Dielectric Relaxation Current*), wurden die Dichten von Oxydladungen und Interface-Traps an dem Si-SiO_2 Übergang, sowie die Oberflächen Stromdichten als Funktion der Strahlendosis bestimmt. Die Ergebnisse zeigen, dass die Dosisabhängigkeit der Oberflächendichte, der Oxydladungen und der Oberflächen Stromdichte von der Kristallorientierung und dem Hersteller abhängen.

Darüber hinaus wurde der Einfluss der während der Röntgenbestrahlung an den Gates des MOS-Kondensators und an der Gate-gesteuerten Diode anliegenden Spannung auf die Oxid-Ladungsdichte, auf die Dichte der Traps an der Grenzfläche sowie auf die Oberflächen-Stromdichte im Dosisbereich von 100 kGy bis 100 MGy untersucht. Dabei wurde herausgefunden, dass diese stark von der angelegten Spannung abhängen, falls das elektrische Feld in dem Oxid von der Oberfläche des SiO_2 zu der Si-SiO_2 Grenzfläche zeigt.

Um die langfristige Stabilität der bestrahlten Silizium-Sensoren zu überprüfen, wurden *annealing*-Studien bei 60 °C und 80 °C mit bis zu 5 MGy bestrahlten MOS-Kondensatoren und Gate-gesteuerten Dioden durchgeführt und so das Ausheilverhalten der Oxidladungen und des Oberflächenstroms bestimmt.

Weiter wurden die makroskopischen elektrischen Eigenschaften von segmentierten Sensoren als Funktion der Dosis untersucht. Es wurde dabei festgestellt, dass die durch Röntgenstrahlung verursachten Schäden die Verarmungsspannung, den Oberflächen Leckstrom und die Kapazität zwischen den Elektroden des segmentierten Sensors erhöhen. Eine Elektron-Akkumulationsschicht an der Si-SiO_2 Schnittstelle wurde beobachtet. Dessen Breite wächst mit der Dosis und nimmt mit der angelegten Spannung ab. Die Elektron-Akkumulationsschicht ist von Bedeutung für die Veränderung der elektrischen Eigenschaften von segmentierten Sensoren.

Die somit gewonnenen Erkenntnisse zu Strahlenschäden in Silizium-Pixel-Sensoren erlaubten das Optimieren der relevanten Paramter mit Hilfe von TCAD-Simulationen und letztendlich die Entwicklung eines strahlenharten Pixel-Sensors für das AGIPD-Projekt.

摘要

在欧洲X射线自由电子激光上所要进行的实验中，硅像素传感器将被广泛使用。在三年的使用期中，传感器所接受的X射线辐射剂量为1 GGy。为了评估X射线对传感器所引起的辐射损伤，对基于高阻硅材料的MOS管和门控二极管进行了辐照。所选用的MOS管和门控二极管由CiS、Hamamatsu、Canberra和Sintef半导体公司生产。在DORIS III同步辐射光源上完成了对这些测试结构的辐照工作，辐照选用了12 keV的X射线。辐照后，对MOS管和门控二极管的电学性质进行了测量，其中包括电容/电导-电压曲线，电流-电压曲线，以及热介电松弛电流随温度的变化曲线。通过上述测量，获得了氧化层电荷的密度、硅-二氧化硅界面陷阱的密度，以及表面电流密度随剂量变化的关系。实验结果表明氧化层电荷、界面陷阱以及表面电流的密度在高剂量辐照后对硅的晶向和半导体生产过程中所使用的技术存在依赖关系。

此外，实验上观测了在辐照过程中应用于MOS管和门控二极管的门电压对于氧化层电荷、界面陷阱以及表面电流所造成的影响。研究发现：如果二氧化硅层内的电场由二氧化硅表面指向硅-二氧化硅界面，由辐射所引发的上述物理量对门电压具有较强的依赖性。

为了验证经过辐照的硅传感器的电学性质具有长期稳定性，对辐照5 MGy剂量的MOS管和门控二极管进行了高温退火研究。退火温度选取60摄氏度和80摄氏度。此工作确定了氧化层电荷和表面电流的退火动力学：二者在不同温度下随时间的变化可以用幂函数表述。基于该工作，幂函数中的未知参数得以确定，以此可预测其余温度下氧化层电荷和表面电流的退火行为。

另外，对硅条形传感器辐射后的宏观电学性质进行了观测。实验发现：X射线所引起的辐射损伤可以增加全耗尽电压、增大暗电流以及电极之间的电容值。测量结果表明在硅晶体内部、硅-二氧化硅界面下形成了一个电子累积层。电子累积层的宽度随辐射剂量值的增大而增大、随传感器偏压值的增大而减小。此电子累积层与条形探测器电学性质的变化息息相关。

最后，使用有限元数值模拟程序对硅像素传感器的几何参数进行了优化。在模拟中考虑并输入了与辐射损伤相关的参数，这些参数由上述实验获得。根据优化结果，为AGIPD探测器设计了抗辐射的硅像素传感器。

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1. Introduction

The next generation light source, the European X-ray Free Electron Laser (XFEL) [1], is now being constructed at DESY, Hamburg and its commissioning is scheduled for 2015. The European XFEL will deliver 27,000 fully coherent, high brilliance X-ray pulses per second each with a duration below 100 fs (as seen in figure 1.1). Studies will be performed in physics, chemistry, life science, materials research and other disciplines with X-ray beam of unique quality. Some unique applications include the structural analysis of single complex organic molecules, the investigation of chemical reactions at the femtosecond-time scale and the study of processes that occur in the interior of planets.

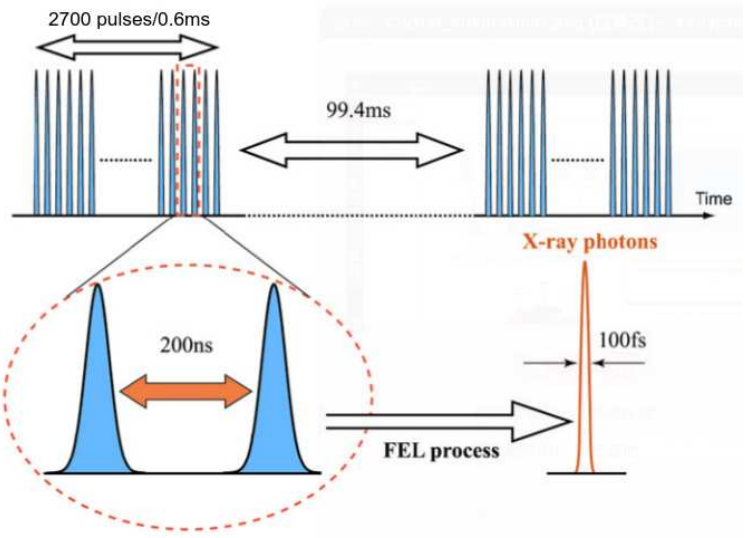


Figure 1.1: The bunch structure of X-ray pulses at the European XFEL: The bunch trains with up to 2700 X-ray pulses, each of a duration of less than 100 femtosecond and separated by 220 ns, repeated 10 times per second.

At the European XFEL, silicon pixel detectors will be used for imaging experiments. They must meet the following extraordinary requirements [2]:

- Large energy range of photons from 0.5 keV to 24 keV
- Sensitivity of single-photon detection
- A dynamic range of up to more than 10^4 12.4 keV photons per pixel per bunch
- A frame rate of 4.5 MHz to satisfy the high repetition rate of X-ray pulses
- Radiation tolerance of 1 GGy (sensor) and 100 MGy (ASIC) for 3 years of operation

1.1. The detector projects for the XFEL: AGIPD, LPD and DSSC

There are three ongoing projects of 2-dimensional imaging detectors for the European XFEL: the Adaptive Gain Integrating Pixel Detector (AGIPD), the Large Pixel Detector (LPD), and the DEPFET (Depleted P-Channel Field Effect Transistor) Sensor with Signal Compression (DSSC).

All the three detectors have to deal with single photon detection and at the same time 10^4 ph/pixel/bunch simultaneously. However, the solutions taken by the three detectors are different: For AGIPD, a dynamic gain switching circuit is designed in ASIC, whose gain can be automatically switched according to the charge produced by the photons. For LPD, three parallel amplifier stages are designed, and the appropriate one can be chosen. For DSSC, its sensor has an intrinsic non-linear gain.

The frontend parameters of the AGIPD, LPD and DSSC are give in table 1.1 [3–5].

Parameter	AGIPD	LPD	DSSC
technology	silicon	silicon	silicon, DEPMOS
energy range	[3 keV, 24 keV]	[1 keV, 24 keV]	[0.5 keV, 24 keV]
pixel size	$200 \times 200\ \mu m^2$	$500 \times 500\ \mu m^2$	$204 \times 236\ \mu m^2$
single photon sensitivity	yes	yes	yes
soft X-ray detection	no	no	yes
dynamic range	2×10^4	10^5	$\sim 10^4$
frame rate	4.5 MHz	4.5 MHz	4.5 MHz
storage cells	352	512	640
ADC gain control	switched 1 fold	3 fold	non-linear

Table 1.1: Parameters of the AGIPD, LPD and DSSC detectors.

1.2. Motivation and structure of this thesis

To address the fore-mentioned challenges, in particular the question of radiation tolerance of 1 GGy in silicon sensor, a good understanding of radiation damage caused by X-rays is required.

The aim of this thesis is to

- understand the radiation damage induced by X-rays,
- extract the damage-related parameters, i.e. the oxide-charge density and the surface-current density, which are the main inputs for sensor optimization with Technology Computer Aided Design (TCAD) [6] simulation,
- investigate the effects due to the voltage applied to the gates of the MOS capacitor and the gate-controlled diode during irradiation,
- verify the long-term stability and performance of silicon sensors with the help of annealing studies,

- investigate the influence of X-ray irradiations on the electrical properties of segmented sensors, and
- design a radiation-hard silicon pixel sensor for the AGIPD Project according to the optimized layout as a result of TCAD simulations.

For the investigation of X-ray radiation damage up to 1 GGy, MOS capacitors and gate-controlled diodes built on high resistivity n-doped silicon with crystal orientations <100> and <111> produced by four vendors, CiS, Hamamatsu, Canberra and Sintef, have been irradiated with 12 keV X-rays at the DESY DORIS III synchrotron light source. The irradiation facility is introduced in chapter 7. Using solid-state measurements, together with model calculation, the oxide-charge density, the interface-trap density and the surface-current density have been determined as function of dose. The measurement set-ups and principles are introduced in chapter 5, the model calculation in chapter 6, the extraction methods in chapter 8, and the results shown in chapter 9.

In addition, the influence of the voltage applied to the gates of the MOS capacitor and the gate-controlled diode during X-ray irradiation on the oxide-charge density, the interface-trap density and the surface-current density has been investigated at doses of 100 kGy and 100 MGy. The results are presented in chapter 10.

To understand the long-term stability of irradiated sensors, annealing studies have also been performed at 60 °C and 80 °C on MOS capacitors and gate-controlled diodes irradiated to 5 MGy and the annealing kinetics of oxide charges and surface current determined and given in chapter 11.

The macroscopic electrical properties of segmented p^+n sensors as function of X-ray dose have been also investigated and results are presented in chapter 12.

Finally, chapter 14 shortly summarizes the efforts by the detector group of Hamburg University for an optimized radiation-hard silicon pixel sensor for the AGIPD Project, and the optimized sensor layout according to the results of TCAD simulation with damage-related parameters.

2. Properties of silicon crystals

The physics of silicon devices is naturally dependent on the physics of silicon crystals. The chapter presents a short introduction to the basic physics and properties of silicon.

2.1. Crystal structure of Si

Silicon crystals have a well-structured periodic placement of silicon atoms. The smallest assembly of silicon atoms is called a primitive cell, whose dimension is characterized by the lattice constant a (a = 0.543 nm at 300 K). The primitive cell is repeated to form the entire silicon crystal.

The silicon crystal has a diamond lattice structure. Such a structure belongs to the tetrahedral phases, in which each silicon atom is surrounded by four neighbouring atoms sharing covalent bonds (figure 2.1(a)). Figure 2.1(b) shows the crystal structure of silicon in face-centred cubic orientation.

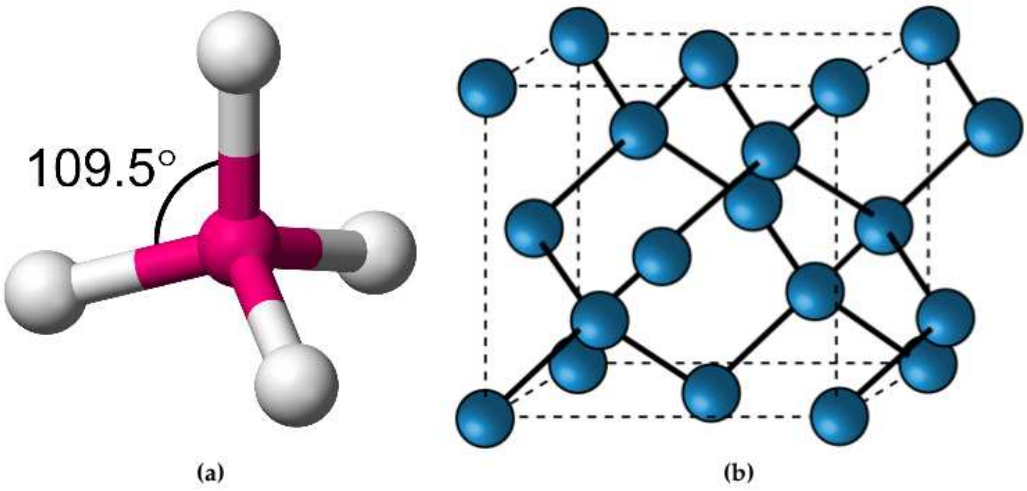


Figure 2.1: (a) Tedrahedral structure of silicon atoms with four neighbouring atoms sharing covalent bonds. (b) Crystal structure of silicon in face-centred cubic orientation. Picture taken from [7].

The orientations and properties of the planes of crystal surface are important. A method to characterize the orientation of planes in a crystal is to use Miller indices: The indices are determined by first finding the intercepts of the plane with the three axe in a (x,y,z) coordinate system in terms of primitive cells, and then taking the reciprocals of these numbers and reducing them to the smallest integers having the

same ratio [8]. The result is enclosed in parentheses (*hkl*) called the Miller indices for a single plane or a set of parallel planes *hkl*. Figure 2.2 shows the Miller indices of important planes in a cubic crystal.

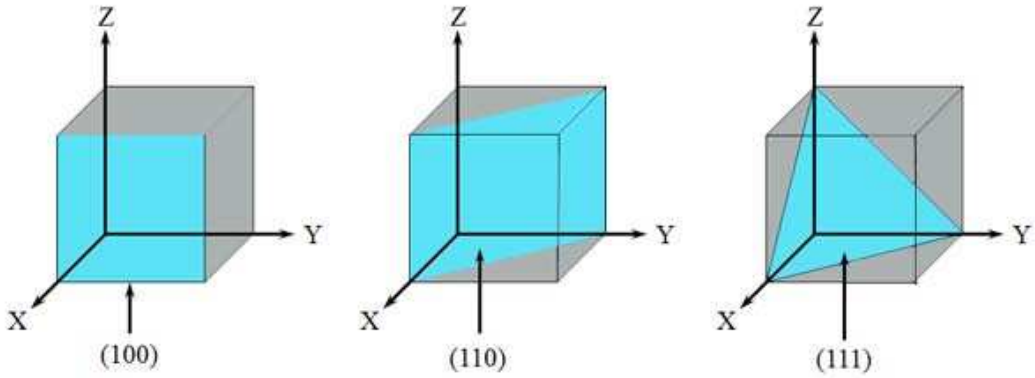


Figure 2.2: Miller indices of some important planes in a cubic crystal. Picture taken from [8].

2.2. Band structure of silicon

Semiconductors like silicon have unique electric conductive properties, which are related to the energy difference between the valence and conduction band. The energy difference is called *band gap*. Compared to metals and insulators, semiconductors have an intermediate level of electric conductivity at room temperature. The band gap of a semiconductor is so small that a slight increase of temperature promotes sufficient electrons from the lowest energy level in the valence band to the conduction band. However, the band gap of an insulator is normally large (> 4 eV) so that it dose not allow for electron motion. For metals, their conduction and valence bands overlap, thus electrons can move quite freely between energy levels without a high energy cost.

The band structure of silicon is shown in figure 2.3. Silicon has a so-called indirect band gap (E_g = 1.12 eV at 300 K), which is the (minimum) energy difference between the lower edge of the conduction band and the upper edge of the valence band at different momenta **k** of the electrons.

2.3. Intrinsic and non-intrinsic silicon

A silicon without any dopant is defined as an intrinsic silicon. The numbers of electrons occupied conduction-band levels and holes occupied valence-band levels in an intrinsic silicon crystal are the same and they equal to the intrinsic carrier density at thermal equilibrium condition. The intrinsic carrier density n_i depends on the effective densities of states in the conduction and valence bands, N_c and N_v, temperature, T, and silicon band gap, E_g: $n_i = \sqrt{N_c N_v}\exp(-E_g/(2k_B T))$, with k_B the Boltzmann constant.

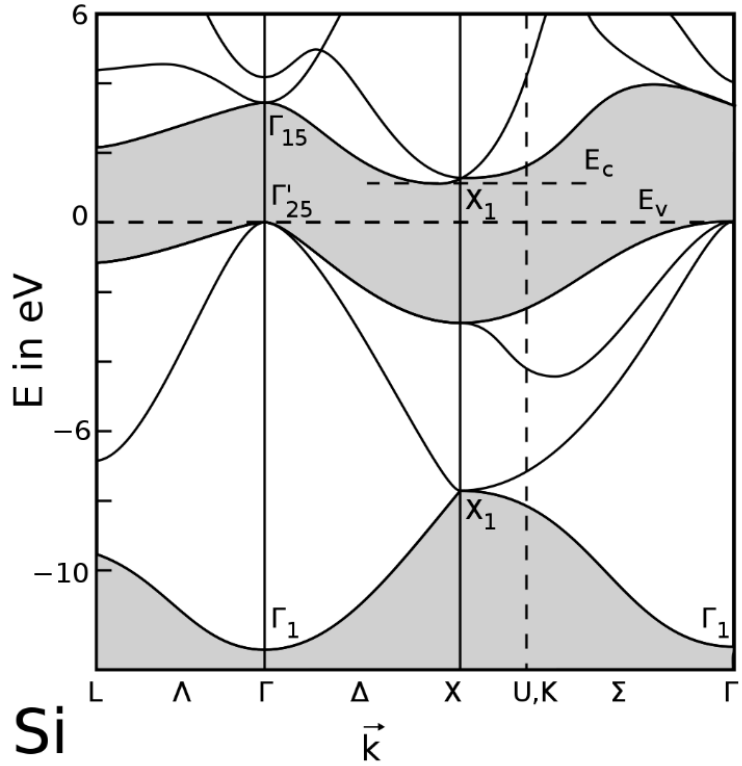


Figure 2.3: Band structure of silicon at a temperature of 300 K. The energy difference between the lower edge of the conduction band (close to X) and the upper edge of the valence band (at Γ) is 1.12 eV. X and Γ are the particular directions/points of the wave vector within the Brillouin Zone (BZ) corresponding to the crystal lattice of silicon. Picture reproduced from [7].

One of the most important properties of silicon is that it can be doped with different types and concentrations of impurities to change its resistivity. In addition, when these impurities are ionized and the carriers are depleted, they leave a charged region which results in an electric field and sometimes a potential barrier inside the doped silicon. The mostly used dopants in silicon sensors are phosphorus and boron. The doped atoms of phosphorus or boron in silicon replace silicon atoms in the lattice and results in an excess of electrons or holes.

Figure 2.4 shows three basic bond pictures of silicon. (a) Intrinsic silicon, which is pure and contains no impurities. Each silicon shares its four valence electrons with the four neighbouring silicon atoms, which forms four covalent bonds. (b) n-type silicon (phosphorus as dopant), where a phosphorous atom with five valence electrons replaces a silicon atom and leaves an electron donated to the lattice in the conduction band. The dopant, which is able to produce excess electrons, is called *donor*. (c) p-type silicon (boron as dopant), where a boron atom with three valence electrons replaces a silicon atom in the lattice and leaves a hole created in the valence band. The dopant producing excess holes is called *acceptor*.

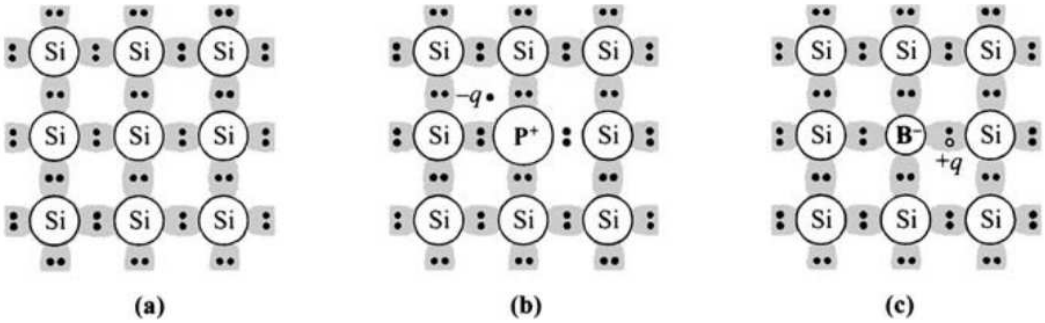


Figure 2.4: Three basic bond pictures of silicon. (a) Intrinsic Si without impurities. (b) n-type Si with donor (phosphorus). (c) p-type Si with acceptor (boron). Picture taken from [8].

For n-type silicon, the number of electrons in the conduction band is given by the effective density of states in the conduction band N_c and the Fermi energy level E_F,

$$n = N_c \exp\left(-\frac{E_c - E_F}{k_B T}\right) \tag{2.1}$$

with E_c the energy of conduction band. Similarly, for a p-type silicon, the number of holes in the valence band can be written as

$$p = N_v \exp\left(-\frac{E_F - E_v}{k_B T}\right) \tag{2.2}$$

where E_v is the energy of valence band. For an intrinsic silicon, due to the fact that $n = p = n_i$, the Fermi energy level is given by

$$E_F = E_i = \frac{E_c + E_v}{2} + \frac{k_B T}{2} \ln\left(\frac{N_v}{N_c}\right) \tag{2.3}$$

Hence the intrinsic Fermi level E_i of a silicon is located very close to the middle of the band gap. However, the Fermi levels E_F of an n-type silicon and a p-type silicon lie in the upper half and the lower half of the band gap, respectively. Figure 2.5 shows the Fermi level E_F as function of temperature T and doping concentration (N_d for n-type silicon; N_a for p-type silicon). At low temperature, the Fermi level E_F moves to the band edge of silicon.

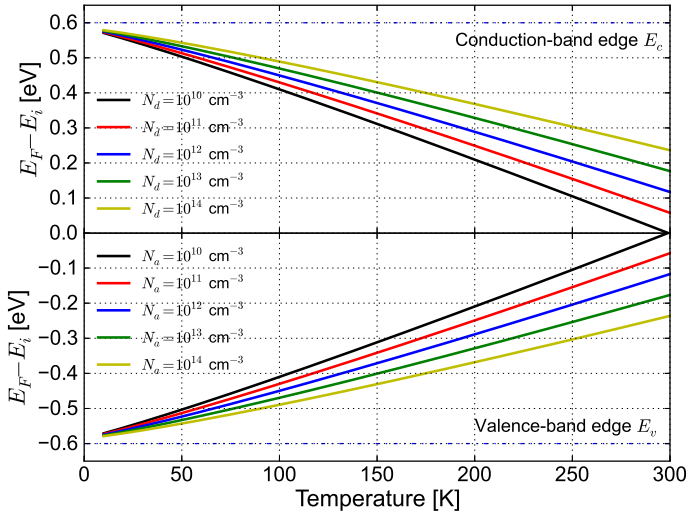


Figure 2.5: The Fermi level E_F as function of temperature T and doping concentration (N_d for n-type silicon; N_a for p-type silicon). The conduction-band edge E_c and valence-band edge E_v, which are taken from the values at $\sim$ 0 K, are shown here for eye-guidance.

The occupation of conduction-band levels, valence-band levels and defects levels in the forbidden band of silicon is a strong function of temperature and energy, and is determined in equilibrium condition ($pn = n_i^2$) by the Fermi-Dirac distribution function

$$F(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)} \tag{2.4}$$

Figure 2.6 shows the schematic band diagram, states density, Fermi-Dirac distribution and carrier concentrations in the conduction band and valence band for intrinsic, n-type and p-type silicon at thermal equilibrium condition.

2.4. Transport of carriers

When an electric field exists in a silicon crystal, holes can drift in the direction of the electric field and electrons in the opposite direction. The drift of carriers inside a silicon causes a current. The drift current under an electric field is given by

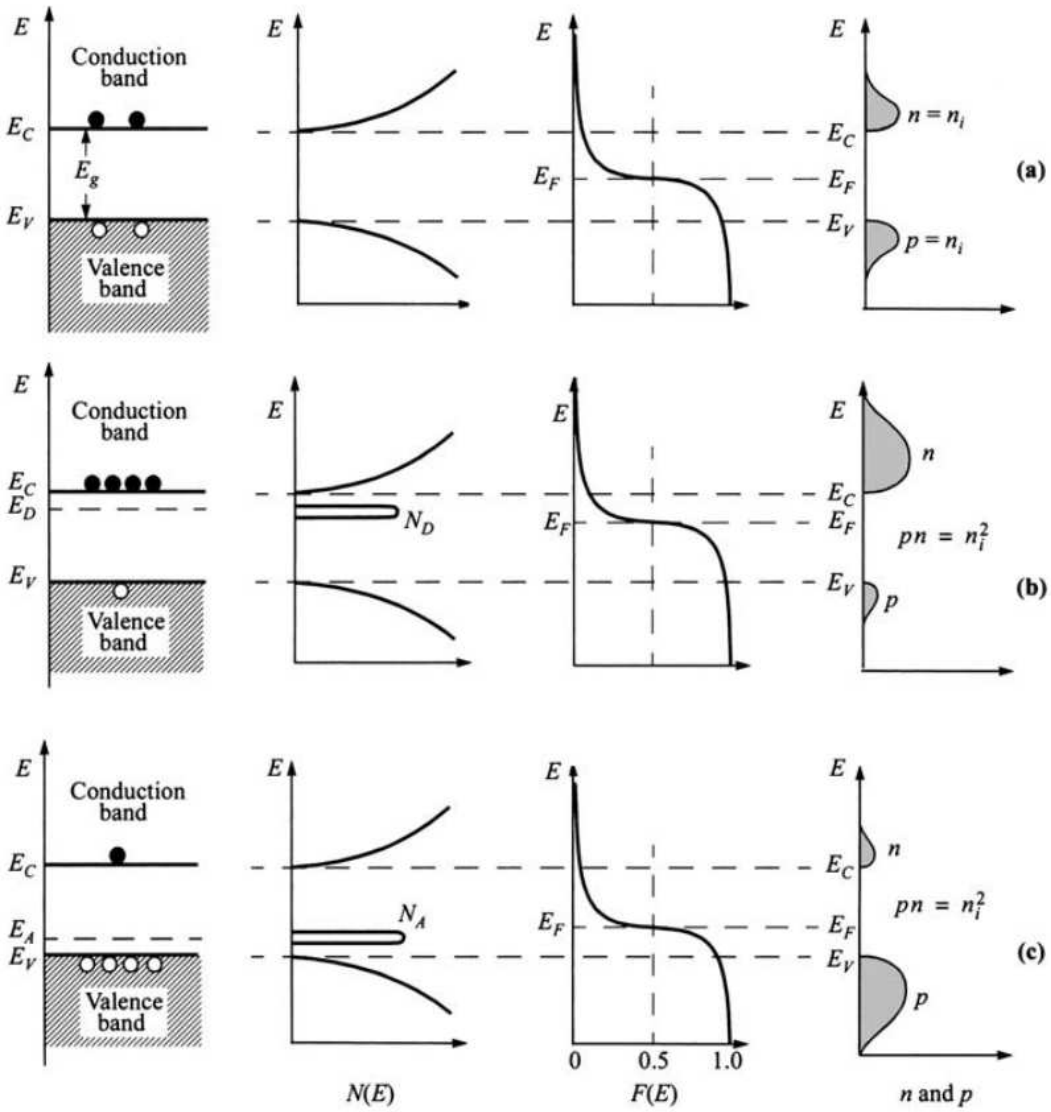


Figure 2.6: Schematic band diagram, states density, Fermi-Dirac distribution, and carrier concentration for (a) intrinsic, (b) n-type, and (c) p-type silicon at thermal equilibrium. Picture taken from [8].

$$\vec{\mathbf{J}} = \sigma\vec{\mathbf{E}} \tag{2.5}$$

where σ is the conductivity,

$$\sigma = \frac{1}{\rho} = q_0\left(\mu_n n + \mu_p p\right) \tag{2.6}$$

and ρ is the resistivity of the silicon material. μ_n and μ_p are the mobilities of electrons and holes in silicon (unit: $cm^2/(V{\cdot}s)$). The mobilities of electrons and holes depend on the electric field and their values saturate at higher field. For an n-type silicon, due to $n \gg p$, the conductivity is given by $\sigma = q_0\mu_n n$.

In the electric field, carriers drift with a velocity. The drift velocity can be written as

$$\vec{\mathbf{v}}_\mathbf{d} = \pm\mu(E)\vec{\mathbf{E}} \tag{2.7}$$

with "+" for holes and "-" for electrons.

In addition, carriers undergo a random diffusion in silicon due to their thermal energy. One important parameter related to the diffusion is the diffusion length of carriers in silicon, which is a direct reflection of diffusion current. The diffusion length L depends on the diffusion coefficient of carriers D and their lifetime τ: $L = \sqrt{D\tau}$, with $D = \mu k_B T/q_0$ the Einstein relation. The larger the diffusion length, the smaller the diffusion current in silicon.

2.5. Generation and recombination of carriers

When the thermal-equilibrium condition of a silicon is changed (i.e., $pn \neq n_i^2$), recombination or thermal generation process restores the system to equilibrium (i.e., $pn = n_i^2$).

One recombination process is the band-to-band direct electron-hole recombination: Electrons jump from the conduction band to the valence band with a photon emitted (radiative process) or with energy transferred to another free carrier (Auger process). Another important recombination process is indirect recombination of electrons and holes with the help of defect levels in the forbidden band gap of silicon. Those defects in silicon not only change the electrical properties of silicon but also influence the lifetime of carriers.

The defect levels in the forbidden band gap of silicon are able to capture electrons and holes. The capture rates are denoted as c_n and c_p. They can also emit the captured electrons and holes to the conduction and valence bands, respectively. The emission rates are denoted as e_n and e_p. The processes that a defect emits/captures a hole to/from the valence band are equivalent to that a defect captures/emits an electron from/to the valence band. Figure 2.7(A) and (D) are the generation and recombination processes of carriers through the defect level. Figure 2.7(B) shows the electron-capture and -emission processes through a defect level in the upper half of the band gap; figure 2.7(C) shows the hole-capture and -emission processes through a defect level in the lower half of the band gap.

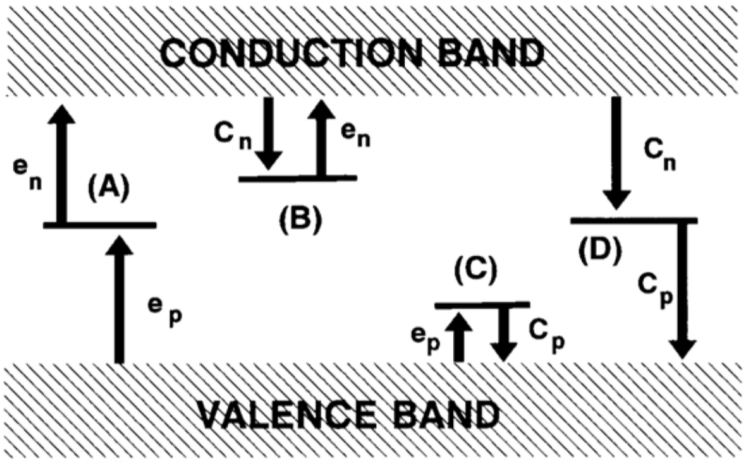


Figure 2.7: Generation and recombination processes of carriers: Generation (A), electron trapping (B), hole trapping (C) and recombination (D).

For a generation/recombination centre, the steady-state condition is that the difference between the capture and emission rates of electrons $(c_n - e_n)$ equal to $(c_p - e_p)$ for holes. Hence, the recombination rate of non-equilibrium carriers U: $U = c_n - e_n = c_p - e_p$. It can be described by the Shockley-Read-Hall statistics as [8]

$$U = \frac{\sigma_n \sigma_p v_{th} N_t \left(pn - n_i^2\right)}{\sigma_n \left[n + n_i \exp\left(\frac{E_t - E_i}{k_B T}\right)\right] + \sigma_p \left[p + n_i \exp\left(\frac{E_i - E_t}{k_B T}\right)\right]} \tag{2.8}$$

where σ_n and σ_p are the electron- and hole-capture cross sections, E_t and N_t the energy level and density of defects, and v_{th} the thermal velocity of free carriers.

The generation/recombination of non-equilibrium carriers causes leakage current in case they are exposed to an electric field. According to equation (2.7), it is seen that the recombination rate U is very sensitive to the energy level of defects and its peak value appears at $E_t = E_i$ for $\sigma_n/\sigma_p = 1$. Hence, the leakage current caused by defect levels is a direct reflection of defect density at the middle of silicon band gap in this situation.

3. Radiation damage induced by X-rays

Silicon detectors are used in nuclear and particle physics since 1960s. However, the real breakthrough came in the early 1980s when micrometer position resolution for charged particles has been achieved and their superior performance for tracking down short-lived particles in experiments of particle physics demonstrated. Since then silicon detectors also found many applications outside of particle physics. Most prominent are the applications of silicon pixel detectors for X-rays in astronomy and at synchrotron radiation sources. New accelerators, in particular the High Luminosity Large Hadron Collider (HL-LHC) and the European X-ray Free Electron Laser, will lead to much higher beam intensities and result in radiation damage in silicon sensors and electronics. The high dose radiation in silicon sensors damages the silicon crystal and its insulating layer, which changes the sensor properties and shorten their lifetime.

This chapter introduces the radiation effects and gives a general understanding of radiation damage, especially the mechanism, microscopic and macroscopic effects of radiation damage induced by X-rays.

3.1. Bulk and surface damage

There are two kinds of radiation damage: bulk damage and surface damage. The former is due to the non-ionizing energy loss (NIEL) [9] of incident particles, i.e. protons, neutrons, electrons and gamma-rays, which cause silicon crystal damage; the latter is due to the ionizing energy loss of charged particles or X-ray photons, which causes the build-up of positive charges and traps in the SiO_2 and at the Si-SiO_2 interface.

Bulk damage

Hadrons, electrons and gamma-rays interact with the silicon atoms via the electromagnetic and strong forces. The silicon atoms can be displaced and create interstitials I and vacancies V. In addition, some more complex configurations, for example di-vacancies V_2 and triple-vacancies V_3, can be created. Figure 3.1 is an exemplary selection of atomic displacements in the silicon lattice after collision with incident particles.

The bulk defects can be classified as point defects and defect clusters. The point defects are so-called *Frenkel-pairs*, which simply consist of a pair of vacancy and interstitial. The defect clusters are dense agglomerations of defects, which usually form at the end of a track of the non-ionizing interaction/collision. The minimum recoil energy of a silicon atom (E_{rec}^{Si}) to produce point defects is 25 eV. Both point defects

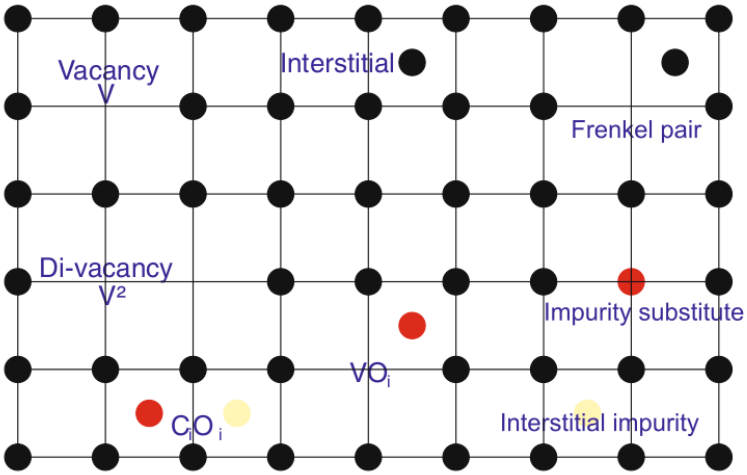


Figure 3.1: An exemplary selection of atomic displacements in the silicon lattice caused by the interactions of incidence particles [10]. V - vacanies; I - interstitials; V_2 - di-vacancies; VO_i - combination of vacancies and oxygen interstitials; C_iO_i - combination of carbon and oxygen interstitials. Picture taken from [10].

and defect clusters can be produced for $E_{Si}^{rec} > 5$ keV [9]. The point defects can be caused by gamma-rays and low energy electrons ($E_e < 1$ MeV), and the defect clusters caused by high energy electrons ($E_e > 8$ MeV) and hadrons.

As seen in figure 3.2, the defects in silicon crystal change the following properties of silicon sensors:

- increase of leakage current
- change of full depletion voltage
- change of effective doping concentration
- change of trapping time
- decrease of charge-collection efficiency

The bulk defects and their influence on the electrical properties of silicon sensors for experiments at the LHC have been studied extensively and can be found elsewhere [9, 12–14].

Surface damage

Radiations by X-rays, gamma-rays and charged particles, e.g. electrons and protons, ionize the Si atoms of crystal and the molecules in the insulating layer, which covers the silicon crystal. Typically, the average ionization energy to produce an electron-hole pair is 3.6 eV for silicon and 17 eV for SiO_2. The carriers produced by ionizing radiation in silicon can be collected by the electrodes. However for the carriers in the insulating layer, some of them cannot escape from this layer, and those remaining form permanent charges in the insulating layer and traps at the interface between silicon and the insulating layer. Hence, the ionizing radiation only damages the in-

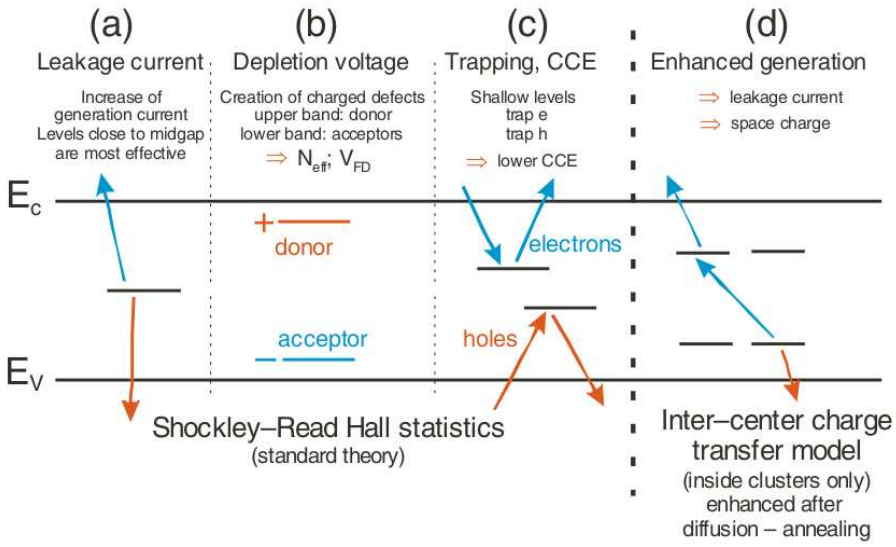


Figure 3.2: The energy levels of bulk defects and their effects. (a) Energy levels close to the mid-gap of silicon are responsible for the generation of leakage current. In addition to high leakage current, levels around the mid-gap of silicon with high states density change the electric field in silicon bulk and further cause the double junction effect [11]. (b) Donors and acceptors in the upper half and lower half of the band gap change the effective doping concentration. (c) Shallow levels trap electrons and holes, and further reduce the charge-collection efficiency (CCE). (d) The inter-center charge transfer model indicates the combination of different defects in the defect clusters and further enhance the effects. Figure taken from [10].

sulting layer and the interface between the insulating layer and the silicon. SiO_2 is the commonly used insulating layer for silicon devices, however an additional insulating layer of Si_3N_4 on top of the SiO_2 is sometimes used to reduce the shift of the flatband voltage or threshold voltage[1] caused by ionizing radiation. The effects of the Si_3N_4 will be discussed in section 3.4.

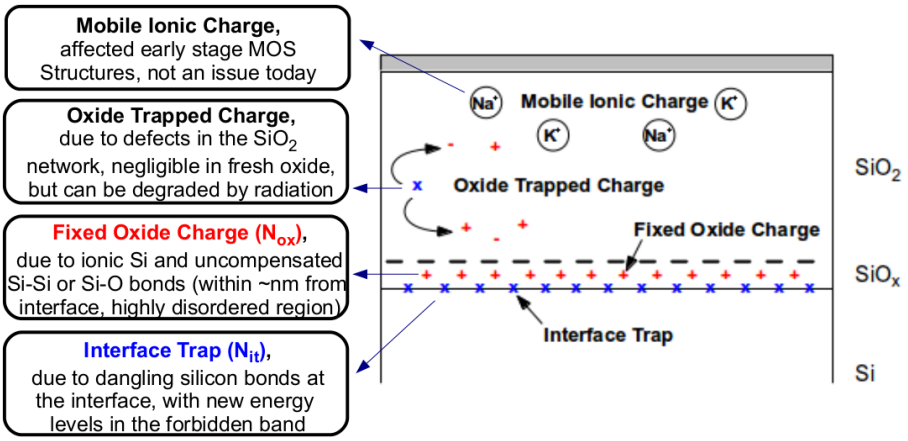


Figure 3.3: Schematic illustration of defects in the SiO_2 and at the Si-SiO_2 interface. Picture reproduced from [8].

For a silicon device, there are mainly four kinds of defects in the SiO_2 and at the Si-SiO_2 interface:

Mobile ionic charge For early silicon devices, ions like K^+, Na^+, Li^+ and perhaps H^+ existed in the SiO_2. The ions are positive charged, thus they can move from the Si-SiO_2 interface to the aluminium gate or vice versa. These ions in the SiO_2 are so-called *mobile ionic charges*. The direction that ionic charges move to depends on the electric field inside the oxide. The mobile ionic charges influence the threshold voltage or flatband voltage for early stage silicon devices. However, this is not an issue today.

Oxide trapped charge The electrons and holes produced by ionizing radiation can be captured by electron traps or hole traps in the SiO_2, and cause *oxide trapped charges*. The oxide trapped charges can be positive or negative, depending on the type of the trap: For an electron trap, the charge stored in the trap is negative when it captures electrons; for a hole trap, the charge is positive when the trap captures holes. The oxide trapped charge is negligible in a fresh oxide, but it can be degraded by radiation damage.

Fixed oxide charge Within several nm from the Si-SiO_2 interface, the region is highly disordered, where the deep level defects are located. The deep levels in the SiO_2 can

[1] The shifts of flatband voltage and threshold voltage are usually used to evaluate the densities of oxide charges and interface traps introduced by ionizing radiation. The flatband voltage and threshold voltage will be described in chapter 4.

trap holes and form *fixed oxide charges*. The fixed oxide charge is positive and can exist in the silicon device for long time [2]. The fixed oxide charges are also known as E′ centres, which consist of two silicon atoms joined by a weak, strained Si-Si bond with an oxygen atom missing, sometimes referred to as oxygen vacancy. Figure 3.4 shows the schematic illustration of an E′ center: Each silicon atom is bonded to three oxygen atoms and one silicon atom; the Si-Si bond breaks when a hole is trapped. The density of E′ center increases with ionizing radiation dose. It is one of the most important radiation-induced defects.

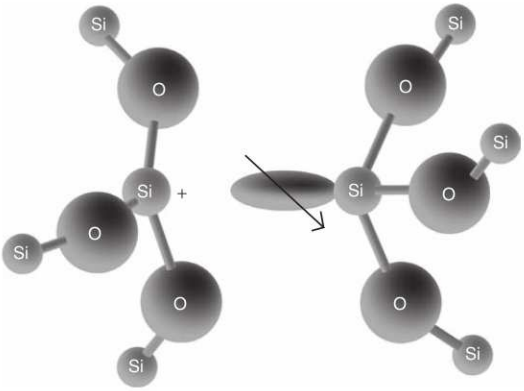


Figure 3.4: Schematic illustration of E′ center in the SiO_2. Picture taken from [15].

Interface trap The dangling silicon bonds at the Si-SiO_2 interface are the origin of *interface traps*. The interface traps have energy levels distributed throughout the band gap of silicon. Those energy levels close to the mid-gap contribute to the surface-generation current according to the Shockley-Read-Hall theory. The interface traps are also known as P_b and P_{bo} centres. Figure 3.5 shows their configurations. P_b and P_{bo} centres exist at the Si-SiO_2 interface of <111> and <100> silicon respectively, however with similar distributions of interface-states levels: One in the upper half of the silicon-band gap, one in the lower half. Compared to <111> silicon, additional centres named P_{b1} also exist at the Si-SiO_2 interface of the <100> silicon. Their densities can be increased by radiation and decreased through a reaction with hydrogen atoms (known as passivation).

Border trap In addition to the fore-mentioned defects, Fleetwood in 1992 suggested that *border traps* should also be included, which have been designated as slow states, near-interface oxide traps, switching oxide traps, and others. The border traps are located within several nm of the Si-SiO_2 interface. They can communicate with electrons and/or holes in the conduction and/or valence band of silicon.

With increasing ionizing radiation dose, the densities of oxide trapped charges, fixed oxide charges, interface traps and border traps increase. In general, the radiation-

[2]This can be seen in chapter 11 of the annealing study.

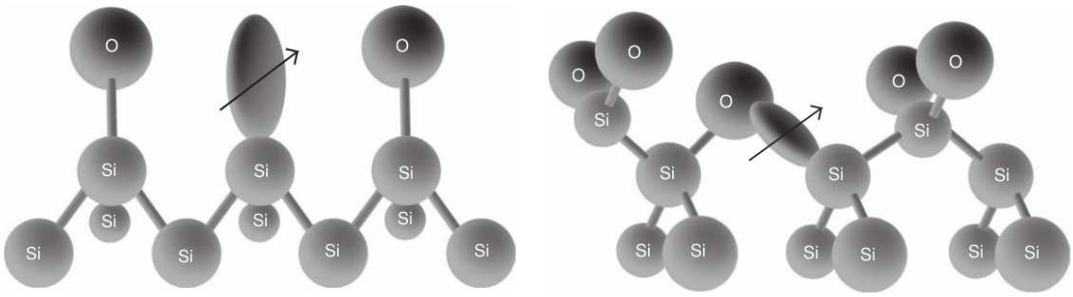


Figure 3.5: Schematic illustration of P_b and P_{bo} centers. Left: P_b center at the <111> Si-SiO_2 interface. Right: P_{bo} center at the <100> Si-SiO_2 interface. Picture taken from [15].

induced defects due to ionizing radiation influence electrical properties and performance of silicon sensors, which can be summarized as follow:

- increase of leakage current dominated by surface current
- increase of full depletion voltage for a p^+n sensor
- formation of an electron-accumulation layer below the Si-SiO_2 interface
- charge losses close to the Si-SiO_2 interface
- increase of interpixel capacitance for a pixel sensor
- decrease of minority-carrier mobility
- decrease of breakdown voltage

3.2. Basic mechanisms of surface damage

The threshold energy for X-rays to cause bulk damage is $\sim$ 300 keV. Therefore, the main damage in silicon sensors at the European XFEL with a typical X-ray energy of 12 keV is surface damage.

The mechanisms of surface damage, in particular the formation of oxide charges and interface traps, have been described extensively in [16–20]. They can be summarized as follow:

(1) X-rays (or charged particles) produce electron-hole pairs in the SiO_2. To produce one electron-hole pair, an average energy of 17 eV is required. Depending on the strength of the electric field in the SiO_2 and the type of incident particles (the density of ionization), a fraction of electrons and holes recombine. Figure 3.6(a) indicates the fraction of unrecombined electrons and holes as function of electric field in the SiO_2 for different radiations: The fraction of electrons and holes escaping from the initial recombination increases with increasing electric field.

(2) The electrons and holes escaping from the initial recombination either drift to the electrode or to the Si-SiO_2 interface, depending on the direction of the electric field in the SiO_2. Some of the holes which drift close to the interface, can be captured by oxygen vacancies (most of the vacancies are located in the SiO_2 close to the Si-SiO_2 interface) and form trapped positive charges in the oxide (oxide charges). The

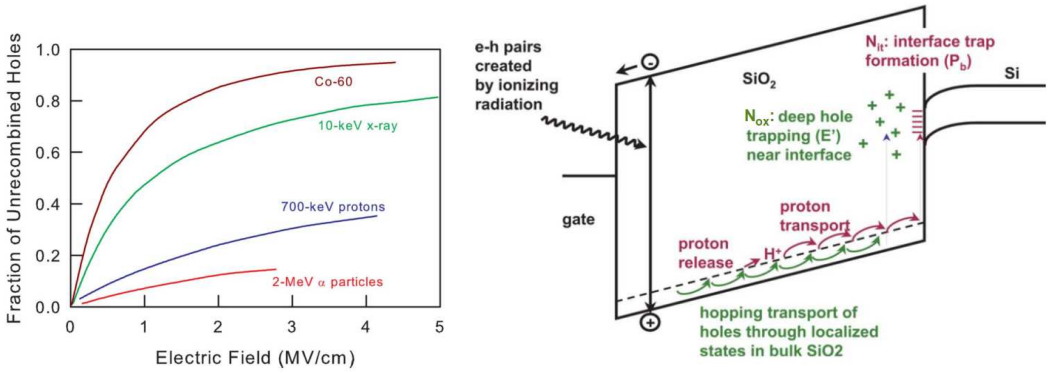


Figure 3.6: (a) Fraction of electrons and holes escaping from initial recombination. (b) Mechanisms of formation of oxide charges and interface traps, shown in the band diagrams of SiO_2, Si-SiO_2 interface and Si. Pictures taken from [20].

reaction is expressed as

$$V_{ox} + h^+ \rightarrow V_{ox}^+ \tag{3.1}$$

where V_{ox} is denoted as oxygen vacancy, h^+ the hole, and V_{ox}^+ the trapped positive charge. The trapped positive charge, V_{ox}^+, is able to capture an electron and form a neutral vacancy,

$$V_{ox}^+ + e^- \rightarrow V_{ox} \tag{3.2}$$

(3) During the transport of holes, some react with hydrogenated oxygen vacancies ($V_{ox}H_2$) and result in protons (H^+). The involved reactions are the capture of holes by $V_{ox}H_2$ to form $V_{ox}H_2^+$ and its reverse reaction,

$$V_{ox}H_2 + h^+ \leftrightarrows V_{ox}H_2^+ \tag{3.3}$$

and the release of protons, H^+, by positively charged oxygenated vacancy, $V_{ox}H_2^+$,

$$V_{ox}H_2^+ \rightarrow V_{ox}H + H^+ \tag{3.4}$$

and the recombination of $V_{ox}H_2^+$ with electrons,

$$V_{ox}H_2^+ + e^- \rightarrow V_{ox}H_2 \tag{3.5}$$

(4) Those protons, which drift to the interface, break the hydrogenated silicon bonds (SiH) at the interface and produce dangling silicon bonds (interface traps, denoted as Si·), with energy levels distributed throughout the band gap of silicon. The reaction is written as

$$H^+ + SiH \rightarrow Si\cdot + H_2 \tag{3.6}$$

Figure 3.6(b) shows the mechanisms of formation of oxide charges (with density N_{ox}) and interface traps (with density N_{it}) in a MOS capacitor biased with positive

gate voltage. The values of N_{ox} and N_{it} induced by X-ray ionizing radiation mainly depend on dose, electric field in the SiO_2, annealing time and temperature, crystal orientation, and quality of the oxide, which will be discussed in section 3.4 in detail.

3.3. Modelling of damage mechanisms

The change of the densities of oxide charges and interface traps with irradiation can be modelled with a set of equations related to drift and diffusion of free carriers in the SiO_2, trapping of electrons and holes by neutral defects, and reactions of passivated silicon bonds at the Si-SiO_2 interface with protons.

Generation of electron-hole pairs To produce an electron-hole pair in SiO_2, 17$\pm$1 eV is needed for X-rays and other kinds of ionizing radiations. According to this energy, the electron-hole pairs per unit volume per rad is: $g_0 = 8.1 \times 10^{14}$ pairs/(cm^3·Gy). But this density is quickly reduced by the initial recombination of electrons and holes.

Initial recombination process When electrons and holes are produced by radiations, they will recombine instantly. The fraction of electrons and holes escaping from the initial recombination mainly depends on two factors: the strength of the electric field in the SiO_2 during irradiation which separates the electrons and holes, and the line density of electron-hole pairs. The line density is determined by the linear energy transfer (LET), which depends on the type of incident particle and its energy (as already seen in figure 3.6(a)). For a higher line density of electron-hole pairs, the average separation distance between electron-hole pairs is small; therefore, more recombination between electrons and holes occur. There are two models describing the initial recombination: geminate recombination model and columnar recombination model, which can be seen in figure 3.7(a) and (b). In the geminate recombination model, the average separation distance between electron-hole pairs is much larger than the thermalization distance, which is the distance between the electron and the hole in a pair. The charges in one electron-hole pair can be treated as an "isolated pair", which have a mutual Coulomb attraction. The electron and the hole in the "isolated pair" drift in opposite directions under the driving force of the electric field in the SiO_2 and have a random diffusion motion due to the thermal velocity. But interactions between one "isolated pair" and another are neglected. In the columnar recombination model, the separation distance between the electron-hole pairs is much smaller than the distance between the electron and the hole in one electron-hole pair. There are more electrons "staying" closer to the hole than the electron in the electron-hole pair; therefore, the recombination probability between electrons and holes is much greater than in the case described by geminate model [19]. Hence, it is expected that the geminate recombination model describes the case for low dose rates better, however the columnar recombination model for high dose rates.

For the geminate recombination model, the generation probability of electron-hole pairs, $Y(E)$, escaping from the initial recombination can be described as function of the electric field E in the SiO_2:

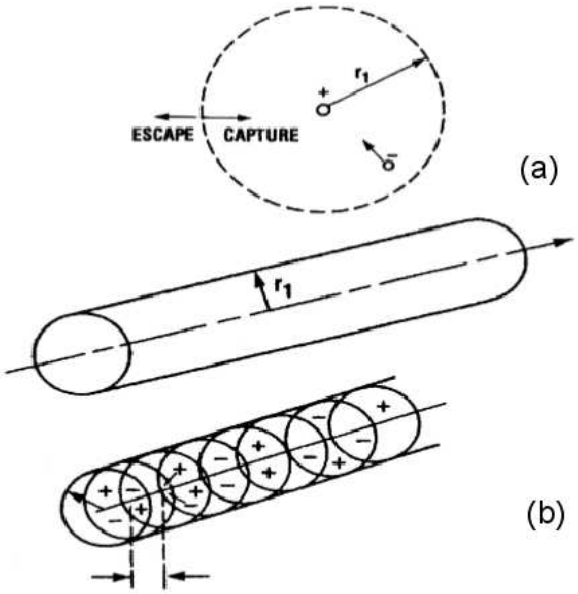


Figure 3.7: Schematic diagrams of the models for initial recombination: (a) geminate model and (b) columnar model.

$$Y(E) = Y_0 + (1 - Y_0)\left(\frac{E}{E + E_0}\right)^m \tag{3.7}$$

with Y_0 = 0.065, m = 0.9, E_0 = 1.35 MV/cm for 10 keV X-rays and m = 0.7, E_0 = 0.55 MV/cm for gamma-rays (^{60}Co). Y_0 is the fraction of electrons and holes escaping from the initial recombination at zero field due to the thermal agitation [21].

Hence, the generation rate of electrons and holes, $G(E)$, can be written as

$$G(E) = g_0 \cdot Y(E) \cdot D' \tag{3.8}$$

where D' is the dose rate of the irradiation.

Transport of electrons, holes and protons The reactions of (3.1)-(3.6) can be formulated into continuity equations describing the transport of electrons, holes and protons. For each kind of charge carrier, the continuity equation is given by

$$\frac{\mathrm{d}n_i}{\mathrm{d}t} + \frac{1}{q_0} \bigtriangledown \cdot \vec{\mathbf{J}}_i = G_i - R_i \tag{3.9}$$

where $n_i = n_i(\vec{\mathbf{r}}, t)$ is the density for each kind of charge carrier (labelled as i) which is a function of position $\vec{\mathbf{r}}$ and time t. $\vec{\mathbf{J}}_i$, G_i and R_i are the current density, generation rate and reaction rate (or call it consuming rate) of each kind of charge carrier. To be more specific, the density of electrons is denoted as n, holes as p and protons as n_{H^+}. Considering a simple 1D structure for SiO_2, the space and time dependent continuity equations are

$$\frac{\partial n}{\partial t} = -\frac{1}{q_0}\frac{\partial |\vec{\mathbf{J}}_n|}{\partial x} + G_n - R_n \tag{3.10}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q_0}\frac{\partial |\vec{\mathbf{J}}_p|}{\partial x} + G_p - R_p \tag{3.11}$$

$$\frac{\partial n_{H^+}}{\partial t} = -\frac{1}{q_0}\frac{\partial |\vec{\mathbf{J}}_{n_{H^+}}|}{\partial x} + G_{n_{H^+}} - R_{n_{H^+}} \tag{3.12}$$

where G_n, G_p and $G_{n_{H^+}}$ are the generation rates, and R_n, R_p and $R_{n_{H^+}}$ are the reaction rates of electrons, holes and protons. $\vec{\mathbf{J}}_n$, $\vec{\mathbf{J}}_p$ and $\vec{\mathbf{J}}_{n_{H^+}}$ are the current densities of electrons, holes and protons, respectively. They can be expressed as

$$\vec{\mathbf{J}}_n = q_0 n \mu_n \vec{\mathbf{E}} + q_0 D_n \frac{\partial n}{\partial x} \tag{3.13}$$

$$\vec{\mathbf{J}}_p = q_0 p \mu_p \vec{\mathbf{E}} - q_0 D_p \frac{\partial p}{\partial x} \tag{3.14}$$

$$\vec{\mathbf{J}}_{n_{H^+}} = q_0 n_{H^+} \mu_{H^+} \vec{\mathbf{E}} + q_0 D_{H^+} \frac{\partial n_{H^+}}{\partial x} \tag{3.15}$$

with μ_n, μ_p and μ_{H^+} the mobilities of electrons, holes and protons in the SiO_2. D_n, D_p and D_{H^+} are the electron, hole and proton diffusivities in the SiO_2. $\vec{\mathbf{E}}$ is an electric field vector, which is a function of position: $\vec{\mathbf{E}} = \vec{\mathbf{E}}(x)$ for 1D case. $\vec{\mathbf{E}}(x)$ can be obtained by solving Poisson's equation,

$$\frac{\partial E}{\partial x} = \frac{q_0}{\varepsilon_{SiO_2}}\left(-n + p + n_{H^+} + n_{V_{ox}^+} + n_{V_{ox}H_2^+} \pm n_{Si\cdot}\right) \tag{3.16}$$

where $n_{V_{ox}^+}$ is the concentration of positively charged oxygen vacancies, $n_{V_{ox}H_2^+}$ the concentration of hydrogenated oxygen vacancies after trapping holes, and $n_{Si\cdot}$ the concentration of charged dangling silicon bonds at the Si-SiO_2 interface region. However, the sign of $n_{Si\cdot}$ depends on the type of the interface trap (acceptor or donor) and the trap filling.

Formation of trapped charges and interface traps During the transport of electrons, holes and protons, they can be involved in the reactions (3.1)-(3.6) and result in the formation of oxide-trapped charges and interface traps. The equations for the reactions are given by

$$\frac{\partial n_{V_{ox}^+}}{\partial t} = \frac{1}{q_0}\left(\sigma_{V_{ox}tp}|\vec{\mathbf{J}}_p|N_{V_{ox}} - \sigma_{V_{ox}^+rn}|\vec{\mathbf{J}}_n|n_{V_{ox}^+}\right) \tag{3.17}$$

$$\frac{\partial n_{V_{ox}H_2^+}}{\partial t} = \frac{1}{q_0}\left(\sigma_{V_{ox}H_2tp}|\vec{\mathbf{J}}_p|N_{V_{ox}H_2} - \sigma_{V_{ox}H_2^+rn}|\vec{\mathbf{J}}_n|n_{V_{ox}H_2^+}\right) - \left(r_{V_{ox}H_2^+rp} + r_{V_{ox}H_2^+rH^+}\right) n_{V_{ox}H_2^+} \tag{3.18}$$

$$\frac{\partial n_{Si\cdot}}{\partial t} = \frac{1}{q_0}\sigma_{it}|\vec{\mathbf{J}}_{H^+}|N_{SiH} \tag{3.19}$$

The description of the symbols in the above equations (3.17)-(3.19) are listed in table 3.1.

Symbol	Description
$N_{V_{ox}}$	concentration of V_{ox}
$N_{V_{ox}H_2}$	concentration of $V_{ox}H_2$
N_{SiH}	concentration of SiH
$\sigma_{V_{ox}tp}$	capture cross section of holes by V_{ox}
$\sigma_{V_{ox}^+rn}$	capture cross section of electrons by V_{ox}^+
$\sigma_{V_{ox}H_2tp}$	capture cross section of holes by $V_{ox}H_2$
$\sigma_{V_{ox}H_2^+rn}$	capture cross section of electrons by $V_{ox}H_2^+$
$r_{V_{ox}H_2^+rp}$	reaction rate of $V_{ox}H_2^+$ dissolved to holes
$r_{V_{ox}H_2^+rH^+}$	reaction rate of $V_{ox}H_2^+$ dissolved to protons
σ_{it}	cross section of protons react with SiH

Table 3.1: Description of symbols in the equations (3.17)-(3.19)

Hence, the generation rates and reaction rates in the continuity equations (3.10)-(3.12) can be expressed as

$$G_n - R_n = G - \frac{1}{q_0}\sigma_{V_{ox}^+rn}|\vec{\mathbf{J}}_n|n_{V_{ox}^+} - \frac{1}{q_0}\sigma_{V_{ox}H_2^+rn}|\vec{\mathbf{J}}_n|n_{V_{ox}H_2^+} \tag{3.20}$$

$$G_p - R_p = G + r_{V_{ox}H_2^+rp}n_{V_{ox}H_2^+} - \frac{1}{q_0}\sigma_{V_{ox}tp}|\vec{\mathbf{J}}_p|N_{V_{ox}} - \frac{1}{q_0}\sigma_{V_{ox}H_2tp}|\vec{\mathbf{J}}_p|N_{V_{ox}H_2} \tag{3.21}$$

$$G_{H^+} - R_{H^+} = r_{V_{ox}H_2^+rH^+}n_{V_{ox}H_2^+} - \frac{1}{q_0}\sigma_{it}|\vec{\mathbf{J}}_{H^+}|N_{SiH} \tag{3.22}$$

Solving the above electron- and hole-continuity equations, the Poisson equation for the electric field, and the equations related to those reactions, the concentrations of trapped charges by oxygen vacancies ($n_{V_{ox}^+}$) and dangling silicon bonds are obtained. Thereafter, the oxide-charge density, N_{ox}, defined as the density of equivalent charges at the Si-SiO_2 interface can be determined by integrating the concentration of trapped charges by oxygen vacancies, $n_{V_{ox}^+}$, throughout the entire SiO_2 region. These partial differential equations (PDEs) are highly coupled; hence, one needs to turn to a numerical scheme with dedicated algorithms and a finite element method (FEM) in order to solve the equations.

3.4. Factors influencing the densities of oxide charges and interface traps

The oxide-charge density, N_{ox}, and interface-trap density, N_{it}, are very sensitive to ionizing radiation and the operating conditions: For example, the total ionizing dose (TID), dose rate and bias voltage of silicon devices which leads to different electric fields in the SiO_2. In addition, the oxide thickness, additional insulating layer on top of the SiO_2, post-irradiation conditions also influence N_{ox} and N_{it}. These factors will be discussed separately.

Total ionizing dose Due to the exposure of silicon devices to ionising radiation, positive charges and interface traps will build-up and accumulate within the bulk of the oxide and at the Si-SiO_2 interface. The oxide-charge density and interface-trap density change significantly with the accumulated dose in the oxide. With increasing dose, the number of holes produced through the ionization of SiO_2 molecules by radiations and of protons released from the positively charged hydrogenated oxygen vacancies increase. This results in more oxide charges formed and interface traps build-up. This effect is so-called total ionizing dose (TID) effect [22, 23].

Dose rate Different dose rates result in different densities of electron-hole pairs. The density of electron-hole pairs for a high dose rate is larger than that for a low dose rate. Hence, the initial recombination between electrons and holes follows the geminate model for low dose rates, but the columnar model for high dose rates: The former leaves more electrons and holes in the oxide compared to the latter. Hence, it is expected that, for a certain dose, more oxide charges and interface traps are formed for low dose rates compared to high dose rates. In addition, the reduction of oxide charges and interface traps for irradiations with high dose rates is also explained by a charge-sheet model [24]: The high concentration of positive charges (holes), after escaping from the initial recombination, forms a charge sheet in the oxide, which pushes the holes above this layer away from the interface and prevents the oxygen vacancies close to the Si-SiO_2 interface to trap holes.

Electric field The fraction of electrons and holes escaping from the initial recombination depends on the strength of electric field in the oxide. The stronger the electric field, the larger the yield of electrons and holes, $Y(E)$ as specified by formula (3.7). The large amount of holes, in principle, results in more holes trapped by the oxygen vacancies. In addition, if the electric field in the oxide points to the Si-SiO_2 interface, holes drift to the interface and thus produce more oxide charges and interface traps. The presence of an electric field in the oxide is able to break the equilibrium between the trapping of holes by oxygen vacancies (the 2^{nd} term of eq.(3.17)) and the recombination of trapped holes with electrons (the 3^{rd} term of eq.(3.17)). Then the oxide-charge density and the interface-trap density can be much larger than the values obtained for an irradiation without any electric field.

Oxide thickness For a thicker oxide, more electrons and holes can be produced per unit dose. If an electric field exists in the oxide and it points to the Si-SiO_2 interface, the oxide-charge density and interface-trap density are approximately linearly dependent on the oxide thickness t_{ox}. This is due to the number of holes produced by radiation per unit dose linearly depends on t_{ox}. However, the situation changes according to the spatial distribution of the oxygen vacancies in the oxide and the direction of the electric field: If oxygen vacancies are concentrated in a very thin layer with a typical depth of $t_{V_{ox}}$, which is far thinner than the oxide thickness ($t_{V_{ox}} < t_{ox}$), N_{ox} and N_{it} do not strongly depend on t_{ox} if no electric field is present or the electric field points away from the Si-SiO_2 interface, but linearly increase with t_{ox} if the electric field points to the interface. If oxygen vacancies are uniformly distributed in the oxide, N_{ox} increase with t_{ox} independent of the direction of the electric field. In addition, a thinner oxide results in an effect called *dose enhancement effect*: Most of the energy deposition of photons is actually due to secondary electrons. In general, the charged particle equilibrium (CPE) is maintained in a homogeneous slab of material due to the fact that the number of secondary electrons scattering into the other volume is equal to the number of electrons scattered out of it. However, the CPE is not maintained in an metal-oxide-semiconductor device because more secondary electrons cross an interface from the high-Z side than from the low-Z side [19]. As seen in figure 3.8, the dose in the SiO_2 equals to the actual one for thick oxide, but is enhanced for thin oxide. For an oxide with a thickness of less than 100 nm, the dose is enhanced by about 50% [25]. However, for an oxide typically used for silicon sensors with a thickness in-between 250 nm and 750 nm, the dose in the oxide is enhanced by $\sim$ 20% [25].

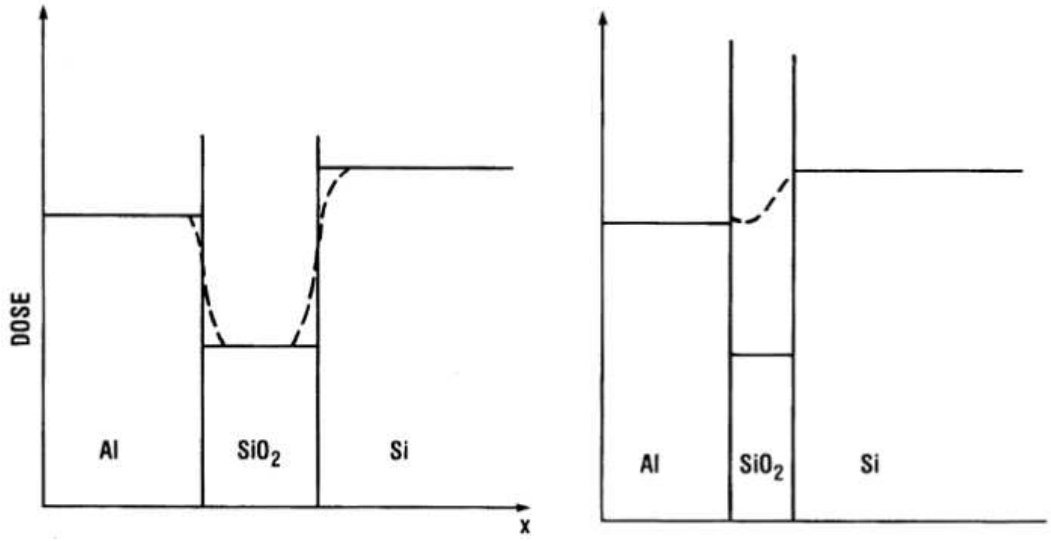


Figure 3.8: Schematic diagram of the dose enhancement effect in thick and thin oxide layers. Solid - equilibrium doses in the oxide. Dashed - actual doses. Pictures taken from [19].

Additional insulating layer An additional insulating layer, for example Si_3N_4, on top of the SiO_2 helps improving the radiation hardness of a silicon device. The advantage is that such a combination of SiO_2 and Si_3N_4 insulating layers reduces the shift of flatband voltage or threshold voltage due to ionizing radiation. The band gap of Si_3N_4 is 5.1 eV, which is smaller than the band gap of SiO_2 of 8.8 eV. Both the conduction and valence bands of Si_3N_4 are within the band gap of SiO_2. This means that the electrons and holes produced by ionizing radiation in the Si_3N_4 insulating layer cannot cross the barrier at the SiO_2-Si_3N_4 interface and drift into the SiO_2; however, the electrons and holes produced in the SiO_2 are able to cross the barrier and drift to the gate. For an electric field pointing to the Si-SiO_2 interface, holes produced in the Si_3N_4 drift to the SiO_2-Si_3N_4 interface and are trapped there. This results in trapped positive charge at the SiO_2-Si_3N_4 interface. For an electric field pointing away from the Si-SiO_2 interface and a "zero" electric field, electrons produced in the Si_3N_4 drift to the SiO_2-Si_3N_4 interface and are trapped at the interface. The trapped negative charge reduces the shift of flatband voltage or threshold voltage caused only by the oxide charges. The charge layer built up at the SiO_2-Si_3N_4 interface in turn influences the electric field inside the SiO_2, which affecting the oxide-charge density and interface-trap density as discussed above.

Post-irradiation condition After exposing the silicon device to the ionizing radiation, oxide charges and interface traps are built up in the SiO_2 and at the Si-SiO_2 interface. The amount of oxide charges and interface traps decreases with time and temperature, which is also called *annealing* of defects. The annealing of oxide charges and interface traps happens at high temperature, room temperature and even below zero degree. In principle, the higher the temperature and the longer the time, the more oxide charges and interface traps are annihilated. However, if the temperature is high enough, for example larger than 450 °C [17], reverse annealing can happen: The oxide-charge density and interface-trap density increase with annealing time. Therefore, carefully selecting the post-irradiation condition for silicon devices help with recovering their electrical properties and performance.

Others Some other factors like the crystal orientation and the gate material are also able to influence the formation of oxide charges and interface traps. It is well known that, before irradiation, N_{ox} and N_{it} for <100> orientation are lower than that for <111>. But little difference in N_{ox} and N_{it} is expected for the two orientations after irradiation. However, it is not clear to the author whether there is a difference in the spatial distribution of oxygen vacancies in the SiO_2 for devices with the same oxide thickness but different orientation, which is supposed to be the factor influencing the oxide-charge density if the irradiation condition (dose and dose rate) is fixed. The other factor, like a different gate of poly-silicon, may affect the formation of interface traps. As other gates are not commonly used for silicon sensors, it is not a real issue for the design of a radiation-hard sensor.

3.5. Electrical properties of defects in the SiO_2 and at the Si-SiO_2 interface

Oxide charges The oxide charges are mainly located close to the Si-SiO_2 interface but also extend deeper into the oxide. They are positive charges in the oxide and thus induce negative charges accumulating below the Si-SiO_2 interface and at the gate for a MOS capacitor. The electrons accumulated below the interface result in a large bending of the conduction band and valence band of the silicon. The presence of oxide charges in the SiO_2 causes a shift of flatband voltage for a MOS capacitor and a shift of threshold voltage for a MOS Field Effect Transistor (MOSFET). In a segmented p^+n sensor, the region below the Si-SiO_2 interface with accumulated electrons is insensitive to detection, and the electric field in this region is small so that electrons and/or holes produced by ionizing radiation may get lost there. In a segmented n^+n or n^+p sensor, the electron-accumulation layer is able to short the neighbouring implanted electrodes and the spatial resolution of the sensor is lost. Hence, for such sensors, a layer with (moderate) boron is usually implanted below the interface to prevent that the electrons accumulate due to oxide charges.

Interface traps The interface traps, with energy levels distributed throughout the silicon-band gap, are located at the Si-SiO_2 interface. They can be charged or discharged, depending on the type of the trap and the position of the energy levels with respect to the quasi Fermi level in the silicon bulk. In general, the type of interface traps can be acceptors or donors [3]. For an acceptor, the charge stored in the trap is negative when it is filled by electrons (energy level below the quasi Fermi level) and neutral when it is empty (energy level above the quasi Fermi level). For a donor, the charge stored in the trap is positive when it is filled by holes (energy level above the quasi Fermi level) and neutral when it is empty (energy level below the quasi Fermi level). How many charges are stored in the interface traps follows the Fermi-Dirac statistic,

$$Q_{it}\left(\psi_s\right) = \begin{cases} -q_0 A \int_0^{E_g} D_{it}\left(E_{it}\right) f_{it}^0\left(E_{it},\psi_s\right) dE_{it} & for\ acceptors \\ q_0 A \int_0^{E_g} D_{it}\left(E_{it}\right)\left(1 - f_{it}^0\left(E_{it},\psi_s\right)\right) dE_{it} & for\ donors \end{cases} \tag{3.23}$$

with q_0 the elementary charge, A the gate area, $D_{it}(E_{it})$ the distribution of interface-states density within the silicon band gap. $f_{it}^0(E_{it},\psi_s)$ the probability of a trap being occupied with an electron (sometimes called *occupation probability*), which is a function of the energy level of the interface states E_{it} and the band bending ψ_s,

$$f_{it}^0\left(E_{it},\psi_s\right) = \frac{1}{1 + \frac{-(E_c - E_{it}) - q_0\psi_s - E_F}{k_B T}} \tag{3.24}$$

with k_B and T the Boltzmann constant and the temperature, respectively.

[3] In some papers, the interface traps with energy levels located close to the mid-gap of silicon are assumed to be neutral.

Hence, the interface traps change the band bending, depending the type of charge stored in the traps.

In addition, the interface states close to the mid-gap of silicon act as generation (recombination) centres, and contribute to surface-generation current following the Shockley-Read-Hall statistics (SRH). If the interface traps are exposed to an electric field, they cause an increase in leakage current of a silicon sensor.

Border traps The border traps are located in the SiO_2 but close to the Si-SiO_2 interface. Different from the oxide charges, although the border traps are in the oxide, they are able to communicate with electrons and holes in the conduction and valence bands of silicon. However, the exchange of carriers between border traps and silicon is a slow process, as the carriers need to cross the large barriers at the Si-SiO_2 interface and tunnel into the SiO_2. Nevertheless, the border traps, similar to interface traps, are also able to cause shifts of the flatband voltage and threshold voltage but in a different time scale.

3.6. Characteristic parameters of surface damage

To characterize the properties of an oxide and the interface between the oxide and silicon, the following parameters usually need to be known: oxide-charge density N_{ox}, distribution of interface-states density $D_{it}(E_{it})$ and surface-current density J_{surf}. N_{ox} and $D_{it}(E_{it})$ are microscopic parameters, which can be determined from the solid-state measurements like capacitance/conductance-voltage (C/G-V) and thermal dielectric relaxation current (TDRC) on MOS capacitors, whereas J_{surf} is a macroscopic parameter, which can be extracted from the current-voltage (I-V) measurement on gate-controlled diodes. N_{ox}, $D_{it}(E_{it})$ and J_{surf} are the important parameters which we have used in TCAD simulation for an optimized design of the AGIPD sensor aiming for a radiation dose as high as 1 GGy.

3.6.1. Oxide-charge density N_{ox}

Instead of referring to the individual charge contribution in the oxide, the oxide-charge density N_{ox} in the thesis is used to describe an equivalent density of charges at the Si-SiO_2 interface. All charges in the oxide contribute to N_{ox},

$$N_{ox} = N_{fo} + N_m + N_{ot} \tag{3.25}$$

with the fixed oxide-charge density, N_{fo}, the equivalent density of mobile charges at the interface, N_m, and the equivalent density of oxide-trapped charges, N_{ot}. The equivalent density of charges at the interface is proportional to the distance of the charges in the SiO_2 to the surface of the SiO_2 divided by the thickness of the SiO_2. N_m and N_{ot} can be written as

$$N_m = \frac{1}{t_{ox}} \int_0^{t_{ox}} x \rho_m(x) \mathrm{d}x \tag{3.26}$$

and

$$N_{ot} = \frac{1}{t_{ox}} \int_0^{t_{ox}} x\rho_{ot}(x)\mathrm{d}x \tag{3.27}$$

where t_{ox} is the thickness of the SiO_2, $\rho_m(x)$ and $\rho_{ot}(x)$ the concentrations of mobile charges and oxide-trapped charges. x is the distance of the charge/trap to the surface of the SiO_2.

3.6.2. Interface-states density $D_{it}(E_{it})$ and the integrated value N_{it}

The interface-states density $D_{it}(E_{it})$ as function of the position of the energy level within the silicon band gap can be obtained experimentally by the TDRC measurement.

The interface-trap density N_{it} denotes the number of interface traps per unit area (with the unit of cm^{-2}). It is the integral of the distribution of interface-states density $D_{it}(E_{it})$ throughout the silicon band gap,

$$N_{it} = \int_{E_v}^{E_c} D_{it}(E_{it})\mathrm{d}E_{it} \tag{3.28}$$

3.6.3. Surface-current density J_{surf}

The surface-current density J_{surf} is a result of the surface-generation current I_{surf} caused by interface traps per unit area. The unit of J_{surf} is A/cm^2. J_{surf} has a direct relation with a microscopic parameter called *surface-generation velocity* S_0, which is an important input in TCAD simulation,

$$J_{surf} = q_0 n_i S_0 \tag{3.29}$$

with n_i the intrinsic carrier density.

For a homogeneous distribution of interface states across the silicon band gap, S_0 can be obtained by

$$S_0 = \sigma_{eff} v_{th} \pi k_B T D_{it} \tag{3.30}$$

where σ_{eff} is the effective capture cross sections, $\sigma_{eff} = 1/2\sqrt{\sigma_e \sigma_p}$. v_{th} is the average thermal velocity of the minority carriers and D_{it} the interface-states density.

In addition to the above characteristic parameters for surface-radiation damage, the mobility of minority carriers at the Si-SiO_2 interface μ_{surf} is a commonly used parameter to characterize the interface property determined from a MOSFET. μ_{surf} is related to N_{it}: In principle, the larger N_{it} the lower μ_{surf}.

4. Silicon test structures for damage characterization

Pad diodes are usually used to characterize the properties and concentrations of defects related to bulk damage, whereas MOS capacitors, gate-controlled diodes (GCD) and MOS Field Effect Transistors (MOSFET) are used to characterize the defects due to surface damage. In this chapter, these commonly used silicon devices for characterizing damage-related parameters and their operating principles will be introduced.

4.1. Pad diode

The simplest device to detect radiations is the pad diode, which consists of a pn junction. The pn junction is the basic element of silicon sensors. Under reverse bias, electrons and holes produced by radiations will be separated and drift to the two electrodes of the pad diode due to the electric field in the diode.

A pad diode is usually used to characterize the microscopic and macroscopic parameters related to bulk damage. The macroscopic measurements like capacitance-voltage (C-V) and current-voltage (I-V) give the information on the effective doping concentration N_{eff} and the generation current I_{bulk} due to the defects in silicon bulk. The microscopic measurements like deep level transient spectroscopy (DLTS) and thermal stimulated current (TSC) give the detailed information on the concentrations, energy levels and cross sections of defects in the silicon bulk.

For a p^+ on n pad diode, if no external bias voltage is applied, free electrons and holes diffuse from one side to another, which leaves the immobile acceptor ions in the p-doped region and donor ions in the n-doped region. The region consisting of ionized acceptor and donor ions is called *space charge region* (or conventionally *depletion region*). The 2 plots on top of figure 4.1 are the distributions of electrons, holes, and acceptor and donor ions in silicon for an abrupt junction with constant doping concentrations in both p side and n side in the absence of significant bulk damage. Inside the space charge region, an electric field exists due to the presence of ionized acceptor and donor ions. The electric field causes an potential difference between the two sides of the diode. The potential difference here is called *built-in voltage* V_{bi}. It is a function of the concentrations of p-doping and n-doping,

$$V_{bi} = \frac{k_B T}{q_0} \ln\left(\frac{N_a \cdot N_d}{n_i^2}\right) \tag{4.1}$$

where N_a and N_d are the doping concentrations of acceptors and donors. Typically, the built-in voltage is in the range from 0.5 V to 1.0 V.

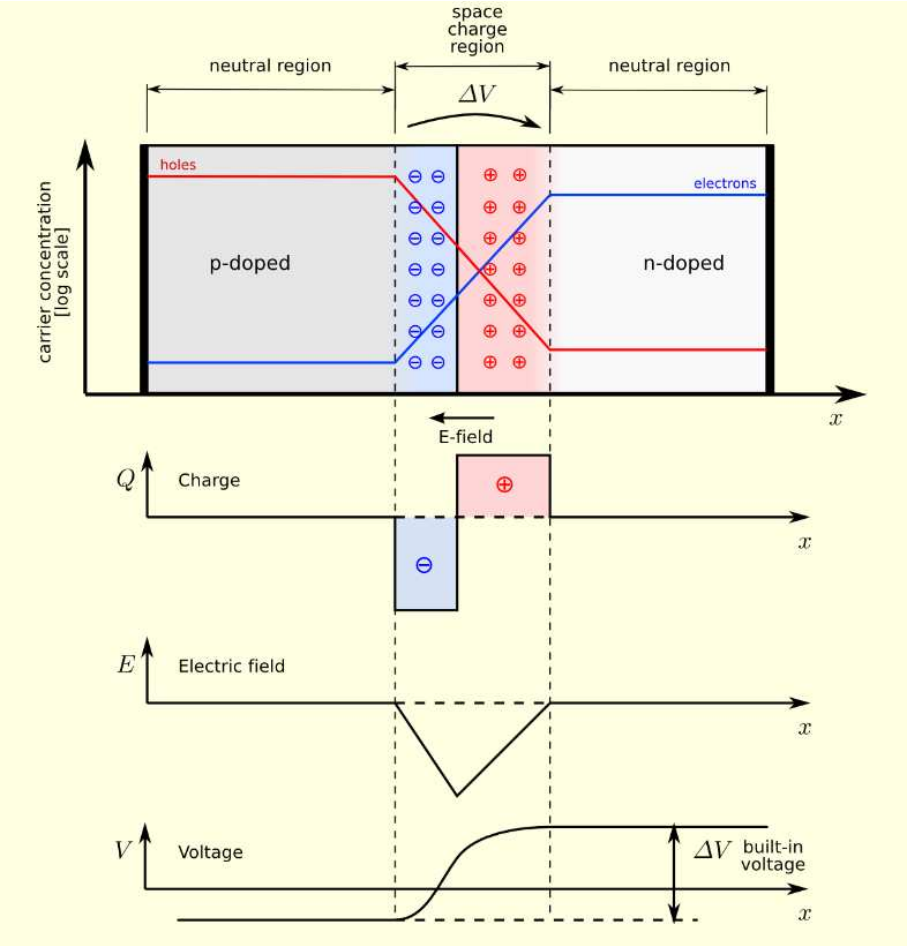


Figure 4.1: Schematic drawing of an abrupt p on n pad diode in thermal equilibrium with zero bias voltage applied. In the first figure, the distribution of electron concentration and hole concentration in silicon are shown in blue and red lines. In the second figure, the concentration of space charges are shown. The third and the fourth are the distributions of electric field and voltage in silicon. Picture taken from [7].

Applying an external bias voltage V_{bias} to the diode the width of the space charge region is changed. If the potential at the p-side is higher than the potential at n-side, the barrier created by the built-in voltage reduces and the diode becomes conductive and behaves like a conductor. This kind of bias condition is called *forward bias*. However, if the potential at n-side is increased (bias voltage added to built-in voltage), electrons and holes are separated further and the width of the space charge region increases. Such a bias condition is called *reverse bias*. The width of the space charge region, W_{sc}, is approximated as

$$W_{sc} = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}(N_a + N_d)(V_{bi} + V_{bias})}{q_0 N_a N_d}} \tag{4.2}$$

with $\varepsilon_0\varepsilon_{si}$ the dielectric constant of silicon.

Capacitance-voltage (C-V) characteristic is an important characteristic of a diode. From the C-V curve, the doping concentration can be determined directly. The capacitance of a diode per unit area, C', is given by

$$C' = |\frac{\mathrm{d}Q}{\mathrm{d}V}| = \frac{\varepsilon_0\varepsilon_{si}}{W_{sc}} = \sqrt{\frac{\varepsilon_0\varepsilon_{si} q_0 N_a N_d}{2(N_a + N_d)(V_{bi} + V_{bias})}} \tag{4.3}$$

For a p^+n diode, $N_a \gg N_d$; hence, the eq.(4.3) is simplified to

$$C' = \sqrt{\frac{\varepsilon_0\varepsilon_{si} q_0 N_d}{2(V_{bi} + V_{bias})}} \tag{4.4}$$

Hence, according to eq.(4.4), it is shown that $1/C'^2$ linearly depends on the bias voltage,

$$\frac{1}{C'^2} = \frac{2(V_{bi} + V_{bias})}{\varepsilon_0\varepsilon_{si} q_0 N_d} \tag{4.5}$$

The doping concentration N_d can be determined from the slope of $1/C'^2$ vs. V_{bias} curve.

The capacitance of a diode decreases with reverse bias voltage until the boundaries of the space charge region reach the two ends of the diode. The corresponding voltage is the *full depletion voltage*. Replacing the capacitance C' in eq.(4.5) by the geometrical capacitance, the full depletion voltage, V_{dep}, can be written as

$$V_{dep} = \frac{q_0 T_{si}^2 N_d}{2\varepsilon_0\varepsilon_{si}} - V_{bi} \tag{4.6}$$

where T_{si} is the effective thickness of the silicon diode. Hence, another method to determine the doping concentration N_d is to extract the V_{dep} from a C-V measurement and then calculate N_d according to eq.(4.6).

Another important characteristic of a diode is the current-voltage (I-V) characteristic. The current flow into an external circuit under a reverse bias voltage is due to two sources: Diffusion current and bulk-generation current. The former is caused by the diffusion of minority carriers (electrons in the p side and holes in the n side):

when minority carriers diffuse through the space charge region, they will drift into the region of the electric field. The diffusion current, I_{diff}, can be written as

$$I_{diff} = \left(\frac{q_0 D_n n_{p0}}{L_n} + \frac{q_0 D_p p_{n0}}{L_p} \right) \left[\exp\left(-\frac{q_0 V_{bias}}{k_B T} \right) - 1 \right] \tag{4.7}$$

where D_n and D_p are the diffusion coefficients of electrons and holes, L_n and L_p the diffusion lengths of electrons and holes, and n_{p0} and p_{n0} the electron concentration in p-doped silicon and hole concentration in n-doped silicon at equilibrium. The bulk-generation current per unit area, I_{bulk}, which is due to the generation of carriers by deep defects in the space charge region, is given by

$$I_{bulk} = \frac{q_0 n_i W_{sc}}{\tau_g} \tag{4.8}$$

with τ_g the generation lifetime, which is related to the lifetimes of electrons and holes in silicon and the energy level of bulk defects.

In general, due to the presence of bulk defects in imperfect silicon, the current under reverse bias is dominated by the bulk-generation current. Figure 4.2 shows the $1/C^2$-V and I-V curves of a p^+n pad diode. Both curves saturate at the full depletion voltage.

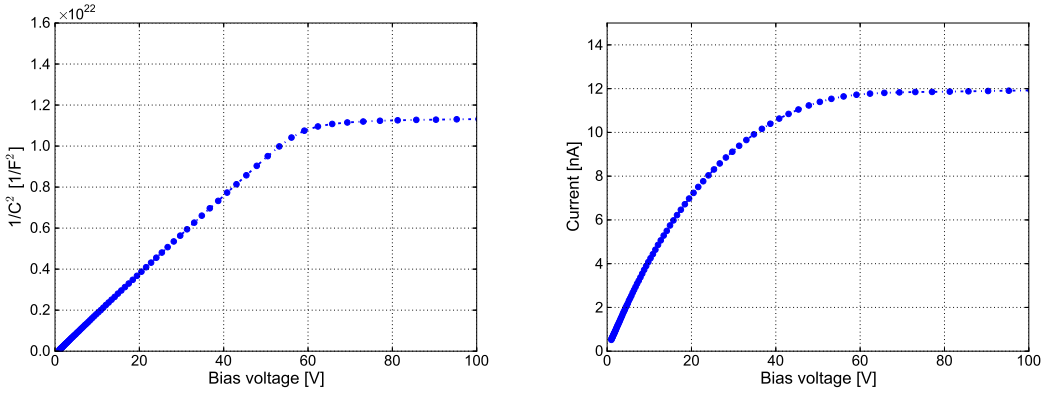


Figure 4.2: Left: Capacitance-voltage ($1/C^2$-V) curve of a p^+n pad diode. Right: Current-voltage (I-V) curve of a p^+n pad diode. The thickness and area of the pad diode are 285 μm and 25 mm^2, respectively.

4.2. MOS capacitor

The sandwich of metal, silicon-dioxide, and semiconductor, called MOS capacitor, is commonly used to characterize the defects in the SiO_2 and at the Si-SiO_2 interface. In case a bias voltage is applied between the metal gate and the rear side of the silicon substrate, no direct current flows through the external circuit thanks to the insulting layer. Therefore, thermal equilibrium can be assumed in both regions: metal gate and silicon substrate. This means that the (quasi) Fermi level in each region is constant.

If the potential at the Si-SiO_2 interface changes, the conduction and valence bands of silicon will be moved with respect to the Fermi level, which causes a change in the spatial distribution of electrons or holes. The operation of a MOS capacitor built on n-doped silicon is illustrated in figure 4.3.

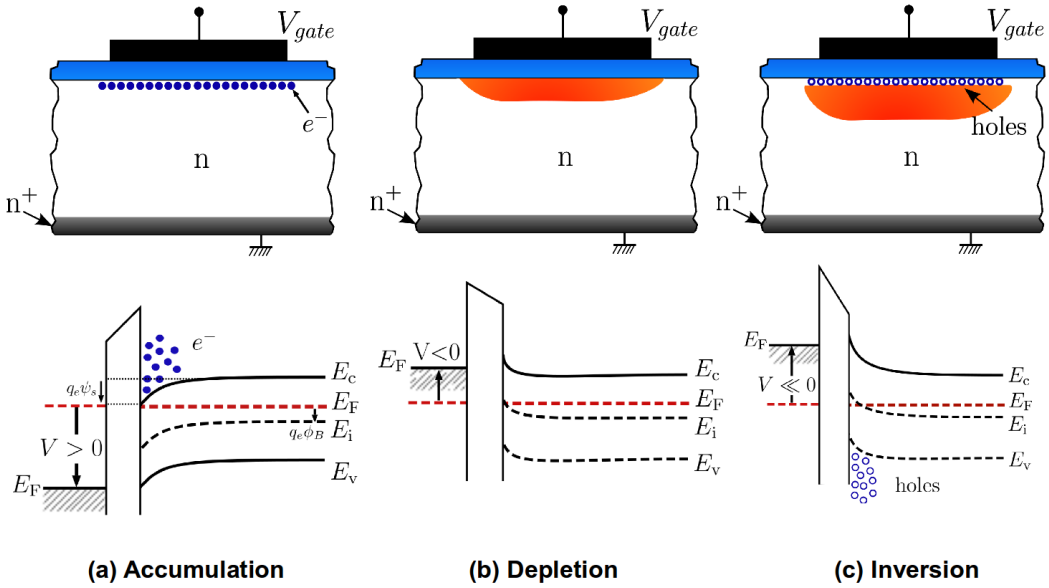


Figure 4.3: Cross section and operating principle of a MOS capacitor built on n-doped silicon. Pictures reproduced from [26].

Accumulation For an ideal MOS capacitor, when a positive voltage is applied to the gate as seen in figure 4.3(a), the Fermi level of the metal gate is lower than that of the silicon substrate. The conduction and valence bands bend downwards at the Si-SiO_2 interface and the band bending ψ_s is positive ($\psi_s > 0$); hence, electrons accumulate at the Si-SiO_2 interface due to the potential difference between the interface and the silicon substrate. This situation is called *accumulation*. The densities of electrons and holes at the Si-SiO_2 interface, n_s and p_s, for a MOS capacitor built on n-doped silicon with a uniform doping concentration of N_d in the silicon substrate, is given by

$$n_s = N_d \cdot \exp\left(\frac{q_0\psi_s}{k_B T}\right) \tag{4.9}$$

$$p_s = \frac{n_i^2}{n_s} = \frac{n_i^2}{N_d} \cdot \exp\left(-\frac{q_0\psi_s}{k_B T}\right) \tag{4.10}$$

Due to the difference of work functions between the metal (ϕ_m) and the silicon (ϕ_s), electrons still accumulate at the Si-SiO_2 interface even without any gate voltage applied. The work function difference ϕ_{ms} is typically in a range between -0.1 V and -1.0 V, which is a function of doping concentration N_d and temperature T,

$$\phi_{ms} = \phi_m - \phi_s = \phi_m - \left(\chi + \frac{E_g}{2q_0} - \phi_B\right) \tag{4.11}$$

with $\phi_B = (E_F - E_i)/q_0 = k_B T/q_0 \cdot \ln(N_d/n_i)$ the potential difference between the Fermi level and the intrinsic Fermi level. χ is the electron affinity for the silicon, $\chi = 0.415$ V, and the work function of the aluminium gate $\phi_m = 0.41$ V. Hence, for a MOS capacitor with a doping concentration of 10^{12} cm^{-3}, the work function ϕ_{ms} is -0.49 V at a room temperature.

Flatband The situation that the conduction and valence bands are flat throughout the silicon substrate, namely the band bending ψ_s equals to zero ($\psi_s = 0$), is called *flatband*. For flatband situation, the Fermi level of the metal gate is the same as the Fermi level of the silicon substrate. In addition, the concentration of majority carriers at the Si-SiO_2 interface is the same as the doping concentration N_d.

Depletion When a negative voltage is applied to the gate, the Fermi level of the metal gate is higher than that of the silicon. The conduction and valence bands bend upwards at the Si-SiO_2 interface and the band bending ψ_s is negative ($\psi_s < 0$); hence, the electric field in the silicon substrate points to the Si-SiO_2 interface. In this situation, electrons are swept out of the interface region and a depletion layer forms close to the interface. This situation is called *depletion*, as seen in figure 4.3(b).

Inversion When the negative voltage on the gate increases, the depletion layer extends deeper and deeper into the silicon until the intrinsic Fermi level at the Si-SiO_2 crosses the (quasi) Fermi level. When intrinsic and quasi Fermi levels are the same, the concentrations of electrons and holes at the interface are equal to the concentration of intrinsic carriers: $n_s = p_s = n_i$. With "increasing" gate voltage, the concentration of holes increases and a layer filled with minority carriers forms. This layer is called *inversion* layer. The *inversion* condition is that $|\psi_s| = \phi_B$. Figure 4.3(c) shows the cross section and band diagram of a MOS capacitor in *inversion* situation. For $\phi_B < |\psi_s| < 2\phi_B$, the concentration of holes at the interface is lower than the doping concentration, but higher than the concentration of electrons. The interface is weakly inverted and the situation is defined as *weak inversion*. For $|\psi_s| \geq 2\phi_B$, the concentration of holes at the interface is even higher than the doping concentration. Hence, the interface is strongly inverted and the situation is defined as *strong inversion*. The onset of strong inversion condition is $|\psi_s| = 2\phi_B$, in which case the concentration of holes at the interface equals to the doping concentration of the silicon substrate.

Figure 4.4(a) shows the relation between the gate voltage V_g and the band bending ψ_s of an ideal MOS capacitor built on n-doped silicon, produced by the model presented in chapter 6. The work function difference between the metal gate and the silicon substrate is not taken into account. In this case, the gate voltage V_g can be simply written as a function of band bending ψ_s as follow,

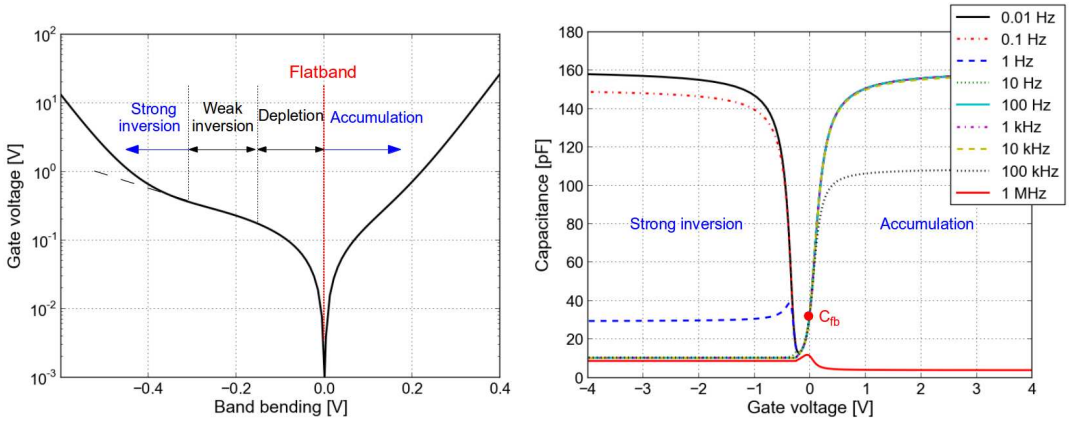


Figure 4.4: (a) Relation between the gate voltage and band bending of a MOS capacitor built on n-doped silicon. The absolute value of gate voltage is shown in a logarithmic scale. (b) Ideal C-V curves of a MOS capacitor built on n-doped silicon for frequencies between 10^{-2} Hz and 1 MHz. Results produced by the model described in chapter 6 with the following parameters: $T_{ox} = 377$ nm, $T_{si} = 285$ μm, $\tau_e = \tau_h = 1$ ms, $N_d = 10^{12}$ cm^{-3} and $N_{ox} = N_{it} = 0$ cm^{-2}.

$$V_g(\psi_s) = \psi_s - \frac{Q_s(\psi_s)}{C_{ox}} \tag{4.12}$$

where Q_s is the surface density of total charge (of unit charge per unit area), and C_{ox} the oxide capacitance. Hence, it can seen that V_g is related to the total charge at the Si-SiO_2 interface. In accumulation, $Q_s \sim \exp(\frac{q_0\psi_s}{k_BT})$; in depletion and weak inversion, $Q_s \sim \sqrt{\psi_s}$; and in strong inversion, $Q_s \sim \exp(\frac{q_0|\psi_s|}{k_BT})$. Hence, V_g follows the same dependence on the band bending ψ_s as Q_s.

Figure 4.4(b) is the corresponding capacitance-voltage (C-V) curves (in parallel mode) with frequencies between 10^{-2} Hz and 1 MHz for figure 4.4(a). The capacitance is obtained by $C = |\frac{dQ_s(\psi_s)}{d\psi_s}|$. In accumulation, the low-frequency capacitance equals to the oxide capacitance C_{ox}. A reduction of capacitance with higher frequencies is observed, which is due to the resistance from the quasi-neutral silicon substrate. With decreasing gate voltage, the surface density of total charge decreases due to the reduction of majority carriers (electrons) close to the interface. Hence, a sharp decrease of the capacitance is seen. The capacitance at the band bending equals to zero ($\psi_s = 0$, namely the flatband condition), is known as *flatband capacitance* C_{fb} and the corresponding voltage is called *flatband voltage* V_{fb}. In depletion, the increase of the depletion layer results in a decrease in the capacitance. The capacitance in strong inversion is constant, however shows again a strong frequency dependence. For higher frequencies, the minority carriers are not able to respond to the AC signal so that the equivalent circuit of a MOS capacitor can be modelled as a capacitor due to the oxide, a capacitor due to the depletion layer and a resistor for the non-depleted silicon substrate arranged in series. Hence, the capacitance measured in inversion for a high frequency is given by the capacitance from the depletion layer together with the oxide

capacitance. For lower frequencies, the minority carriers are able to respond and to follow the AC signal so that the minority carriers can move to the Si-SiO_2 interface from the non-depleted silicon region due to diffusion. The movement of minority carriers in the depletion layer shorts the capacitance; hence, the capacitance measured in inversion for a low frequency equals to the oxide capacitance. The frequency below which the minority carriers respond to the AC signal depends on the lifetime of electrons and holes in silicon and the energy level of defects in silicon.

4.3. Gate-controlled diode (GCD)

The gate-controlled diode (GCD) is a combination of a diode and a MOS capacitor. It is usually used to extract the surface current due to the interface traps. Figure 4.5 shows the cross section and the operating principle of a gate-controlled diode with n-doped silicon: A reverse bias voltage, V_{diode}, is applied to the diode to partially deplete the diode and a voltage applied to the gate, V_{gate}, to control the current flow into the backside. Similar to a MOS capacitor, the gate-controlled diode is able to be operated in three situations: Accumulation, depletion and inversion.

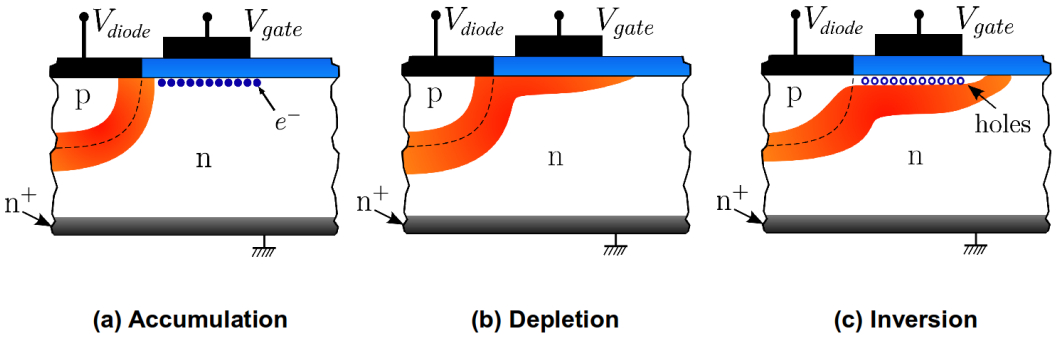


Figure 4.5: Cross section and operating principle of a gate-controlled diode. Pictures reproduced from [26].

Accumulation In this situation ($V_{gate} > V_{fb}$), electrons accumulate below the Si-SiO_2 interface. The current flowing into the backside, is due to the bulk-generation current, $I_{bulk,diode}$, the defects in the depleted region of the diode and the diffusion current, I_{diff}. As shown in figure 4.6, the current measured in this situation I_{acc} is given by $I_{acc} = I_{bulk,diode} + I_{diff}$.

Depletion For $V_{gate} \leq V_{fb}$, the interface region below the gate starts to be depleted. Then an additional depletion layer forms and it merges with the depletion layer of the diode. Interface traps below the gate are exposed to an electric field and contribute to the surface current. The measured current in depletion, I_{dep}, is given by the sum of the surface current, I_{surf}, bulk-generation current due to the defects in the depleted

region of the diode and the MOS capacitor, $I_{bulk,diode}$ and $I_{bulk,MOS}$, and the diffusion current, I_{diff}: $I_{dep} = I_{surf} + I_{bulk,diode} + I_{bulk,MOS} + I_{diff}$.

Inversion Different from the inversion condition for the MOS capacitor, the gate-controlled diode is not in strong inversion for $|\psi_s|$ slightly higher than $2\phi_B$. For $|V_{fb}| \leq |V_{gate}| < |V_{fb}| + |V_{diode}|$, a lateral electric field at the Si-SiO_2 interface exists which points from interface below the gate to the p^+ implant of the diode. Hence, holes produced in this situation drift to and are collected by the p^+ electrode of the diode. Therefore, the interface region is still depleted even if the inversion condition is satisfied for a MOS capacitor. Up to $|V_{gate}| = |V_{fb}| + |V_{diode}|$, the direction of the lateral electric field at the interface changes and holes accumulate at the interface. Hence, the gate-controlled diode is in inversion. The inversion layer below the interface, shields the interface traps and thus the surface current is suppressed. It can be referred in figure 4.6. The current measured in inversion, I_{inv}, is due to all components contributed to I_{dep} except for the surface current I_{surf}, which is suppressed due to the presence of the inversion layer.

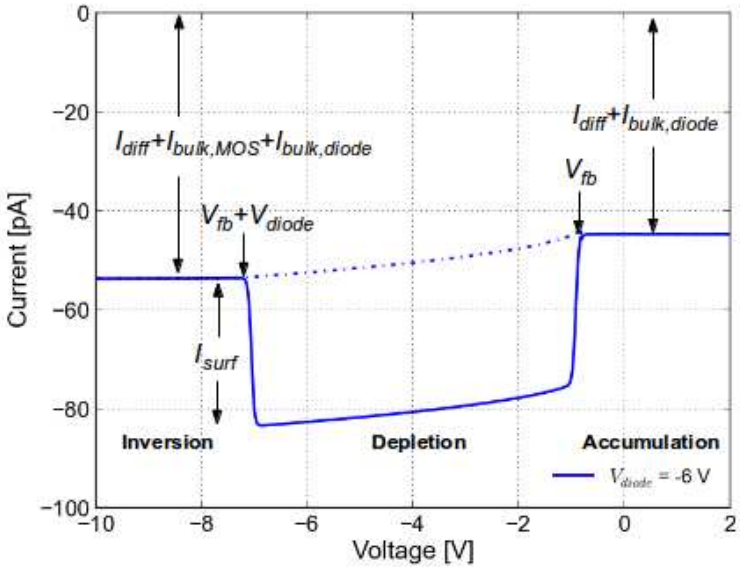


Figure 4.6: Ideal I-V curve of a gate-controlled diode built on n-doped silicon.

Thus, the surface current from the interface traps can be obtained from the difference of the peak current measured in depletion and the current measured in inversion: $I_{surf} = |I_{dep} - I_{inv}|$. However, the method to extract the surface current is limited for highly irradiated GCD. The problems and limitations will be discussed in chapter 8.

4.4. MOS Field Effect Transistor (MOSFET)

The metal-oxide-semiconductor field effect transistor (MOSFET) is an important device for high-density integrated circuits such as microprocessors and semiconductor

memories [8]. It is also an important power device. The MOSFET is usually used to characterize the mobility of minority carriers at the Si-SiO_2 interface.

A MOSFET consists of source, drain and gate, built either on n-doped or p-doped silicon. The MOSFET can be classified as p-channel MOSFET or n-channel MOSFET. For p-channel or n-channel MOSFETs, the carriers below the gate are holes or electrons when the gate is biased to inversion. The gate in a MOSFET is used to control the concentration of minority carriers below the interface: When an inversion layer with minority carriers forms, a voltage difference between source and drain results in a current flow in the channel. The current, however, increases with the gate voltage in case the channel is formed.

Figure 4.7 shows the basic operating principle of a p-channel MOSFET. The voltage on the gate biases the central part of the pMOSFET to either accumulation, depletion or inversion, similar to the MOS and GCD cases. However, the source-to-drain current I_{sd} is the main interest for general studies, which increases sharply when an inversion layer below the gate forms. The right bottom of figure 4.7 is the $I_{sd} - V_{gs}$ characteristic, with V_{gs} the voltage difference between gate and source. The onset voltage of the increase of I_{sd} is defined as threshold voltage, V_{th}. When $V_{gs} < V_{th}$, the central part is biased to either accumulation or depletion. Because the concentration of minority carriers is very low below the Si-SiO_2 interface, no direct current flow is possible. When $V_{gs} \geq V_{th}$, the central part is biased to inversion. An inversion layer forms and the concentration of minority carriers increases with the gate voltage exponentially, as seen in figure 4.4(a). Hence I_{sd} increases quickly with V_{gs}. The source-to-drain current I_{sd} is a function of the mobility of minority carriers, which can be written as [7]

$$I_{sd} = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[\left(V_{gs} - V_{th} \right) \cdot V_{sd} - \frac{1}{2} V_{sd}^2 \right] \tag{4.13}$$

where W and L are the width and length of the channel below the Si-SiO_2 interface, and V_{sd} the voltage difference between source and drain. Right top and right middle of figure 4.7 are the source-to-drain current I_{sd} as function of the source-to-drain voltage V_{sd} of a MOSFET working at $V_{gs} \geq V_{th}$. If no bias voltage is applied to the rear side of the MOSFET, I_{sd} is always working in an ohmic region, which shows a linear dependence on V_{sd}. The channel behaves like a conductor. If a bias voltage applied to the rear side of the MOSFET, I_{sd} increases with V_{sd} in the beginning and saturates at higher V_{sd}. The saturation of I_{sd} is due to the pinch-off of the channel, which is a result of the modification of depletion layer at the corners close to the source and drain.

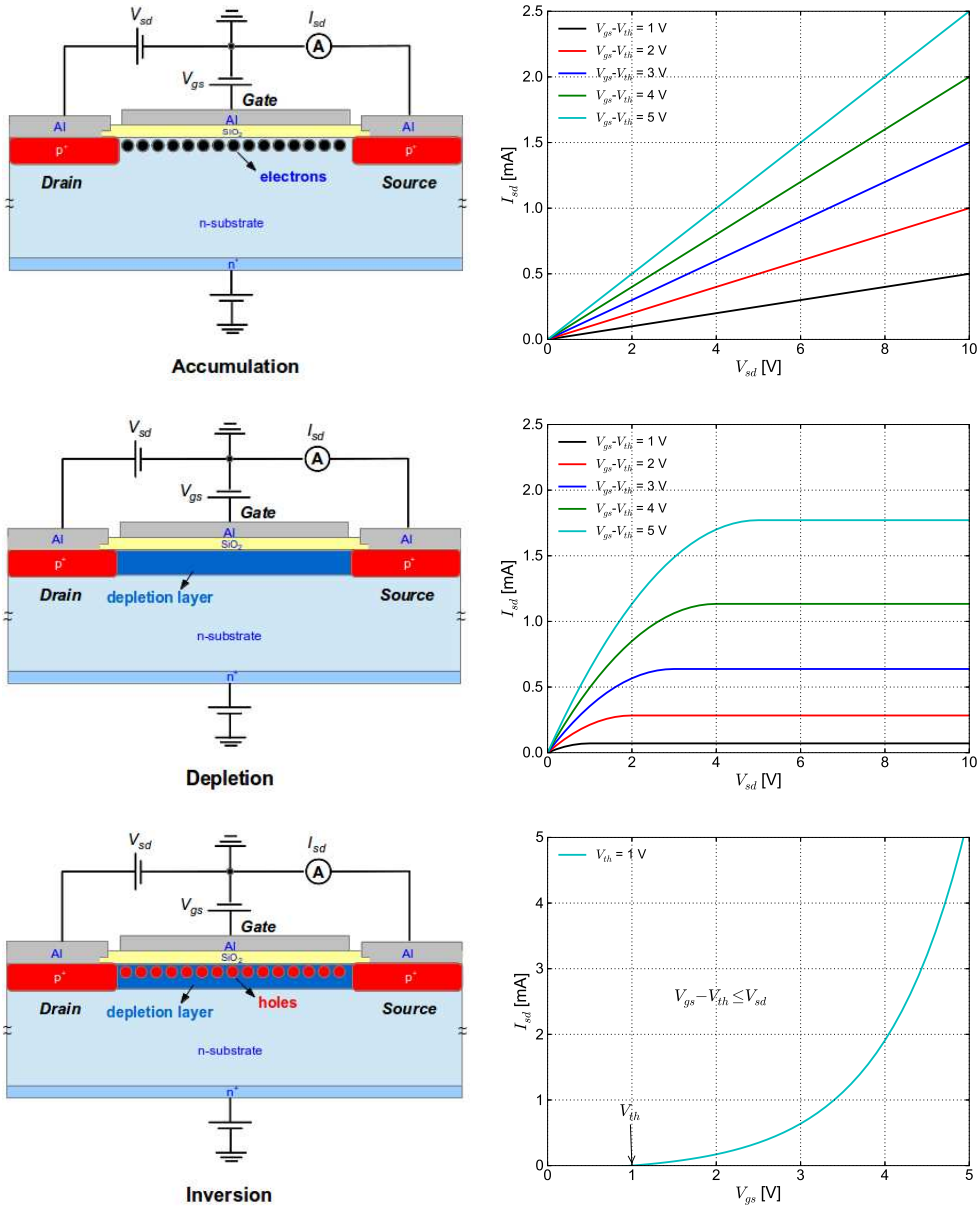


Figure 4.7: Left: a p-channel MOSFET operated in accumulation, depletion, and inversion. Right top: I_{sd} vs. V_{sd} in ohmic region. Right middle: I_{sd} vs. V_{sd} in saturation region. Right bottom: I_{sd} vs. V_{gs}.

5. Measurement set-ups and principles

Capacitance/conductance-voltage (C/G-V) and current-voltage (I-V) are the commonly used measurements to obtain the macroscopic properties, and for surface-radiation damage thermal dielectric relaxation current (TDRC) measurements are used to obtain the microscopic parameters such as the distribution of the interface-states density in the silicon band gap and their capture cross sections. This chapter introduces the set-ups for measuring the macroscopic and microscopic properties of silicon devices and their principles.

5.1. C/G-V and I-V measurements

The C/G-V and I-V set-ups consist of a cold chuck, a Keithley 6517A multimeter, a Keithley 6485 pico-ammeter, a Keithley 6487 power supply, an Agilent 4980A LCR meter and a temperature-control system. The device under test (DUT) is placed on the cold chuck, which is connected to a cooling system and whose temperature can be controlled in the range between ± 20 °C. The dry-air flow is used to reduce the humidity during measurements and avoid contamination. The electrodes of the device are contacted by needles and the needles are connected to either the Agilent 4980A LCR meter, or a Keithley 6517A multimeter, or a Keithley 6485 pico-ammeter, depending on the measurements.

For a C/G-V measurement, the Agilent 4980A LCR meter and the Keithley 6517A multimeter are used: the multimeter provides voltage to bias the device under test; the LCR meter measures the capacitance and conductance between any two electrodes under this biasing condition. The principle of the LCR meter for measuring capacitance and conductance is: The LCR meter applies an AC excitation voltage to the two electrodes and measures the AC current. Then, the admittance Y is calculated by using the AC current, $\widetilde{I}$, divided by the AC voltage, $\widetilde{V}$, which gives the capacitance C_p and conductance G_p in an equivalent parallel circuit.

$$Y = \frac{\widetilde{I}}{\widetilde{V}} = G_p + j\omega C_p \tag{5.1}$$

with $\omega = 2\pi f$ and f the frequency of the applied AC-voltage signal. The LCR meter is also able to calculate the capacitance C_s and resistance R_s in a series mode, which are given by the impedance Z according to

$$Z = \frac{1}{Y} = \frac{\widetilde{V}}{\widetilde{I}} = R_s + \frac{1}{j\omega C_s} \tag{5.2}$$

As seen in figure 5.1, given the fact that $Z = 1/Y$, C_s and R_s in an equivalent series circuit can be calculated from C_p and G_p by

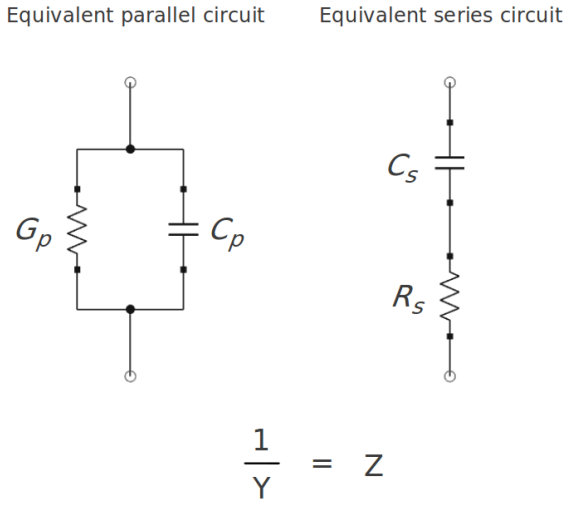


Figure 5.1: The equivalent parallel and series circuits: $Z = 1/Y$.

$$C_s = \frac{G_p^2 + \omega^2 C_p^2}{\omega^2 C_p} \tag{5.3}$$

$$R_s = \frac{G_p}{G_p^2 + \omega^2 C_p^2} \tag{5.4}$$

The amplitude and frequency of the AC voltage from the LCR meter can be chosen. In general, low frequencies (below several tens of Hz) causes large noise and result in unstable measurement values; high amplitudes of the AC voltage ($\sim$ V) added to the bias voltage change the steady-state situation. Therefore, medium frequencies and low AC voltages are preferred.

For an I-V measurement, the Keithley 6517A multimeter and the 6485 pico-ammeter are used: the multimeter biases the device and measures the current from one electrode of the device; the pico-ammeter, if needed, measures the current from another electrode of the device, for example the current from the current-collection ring (CCR) of a diode. For an I-V measurement on a gate-controlled diode (GCD), an additional power source Keithley 6487 is employed to supply a constant voltage on the diode of the GCD.

5.2. TDRC measurements

For determining the microscopic parameters related to the surface-radiation damage, for example the distribution of the interface-states density $D_{it}(E_{it})$ and their capture cross sections, the thermal dielectric relaxation current (TDRC) technique [27] is employed and measurements are performed on MOS capacitors.

5.2.1. TDRC principles

The TDRC technique is a non-steady-state current measurement technique, which involves filling the interface traps with charge carriers that are to be examined.

The basic principles of the TDRC technique can be understood with reference to the energy-band diagrams of an n-type MOS capacitor, as shown in figure 5.2. Figure 5.2(a) shows the MOS capacitor biased to the flatband condition, in which the traps whose levels are below the quasi Fermi level are filled by electrons.

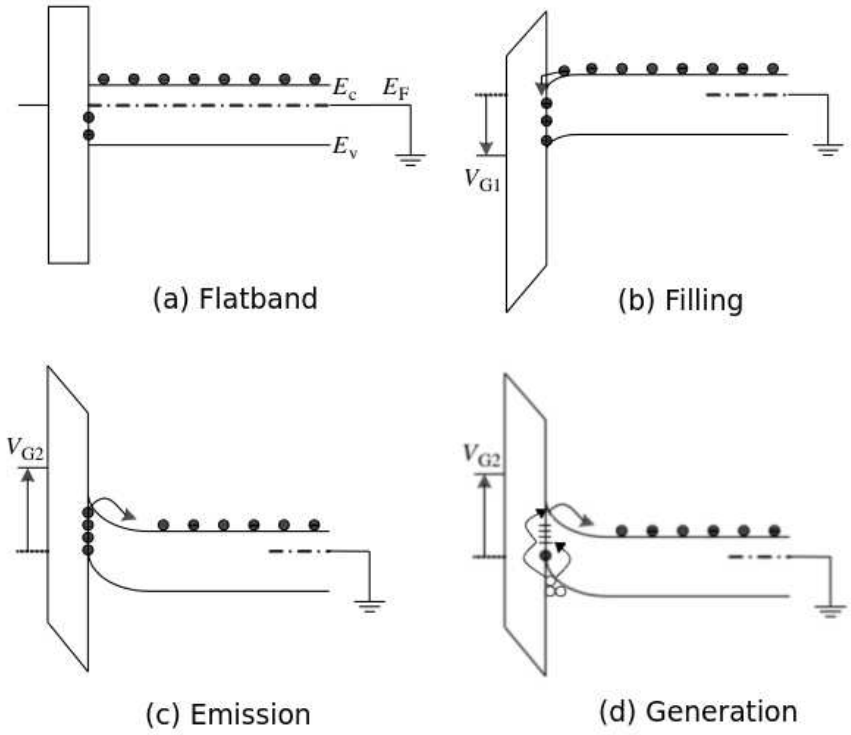


Figure 5.2: Energy diagram of an n-type MOS capacitor (a) in the flatband condition, (b) in accumulation showing the traps filled with electrons (c) in deep depletion showing the emission process, and (d) in deep depletion showing the generation process.

Filling The MOS capacitor is biased in accumulation (usually 0 V for irradiated MOS capacitors) at room temperature, as seen in figure 5.2(b). In this condition, all interface states below the quasi Fermi level are essentially filled by electrons, while those above are empty. Then the MOS capacitor is cooled down to a low temperature (< 30 K) and all trapped electrons are "frozen" in the interface traps.

Emission At the low temperature, the polarity of the gate voltage is reversed and the MOS capacitor is biased in deep depletion. Provided that the temperature is

low enough, the rate of released electrons from the filled interface traps is negligible. Furthermore, the MOS capacitor remains in this non-steady-state deep-depletion condition since the generation of electrons and holes can also be neglected at these temperatures. Then, increasing the temperature of the MOS capacitor with a constant rate β, the trapped electrons by interface states are released and drift in the electric field to the silicon substrate, as seen in figure 5.2(c). The flow of the electrons results in a current flow in the external circuit. The TDRC current I_{tdrc} as function of temperature T during heating up directly reflects the distribution of interface-states density $D_{it}(E_{it})$ in the silicon band gap where $e_n(E_{it}) \gg e_p(E_{it})$ [28]. $e_n(E_{it})$ and $e_p(E_{it})$ are the emission rates for electrons and holes from the defect level E_{it}. The determination of a trap level from the emission current of a TDRC measurement on a MOS capacitor built on n-doped silicon is limited in an energy range from the conduction band to the energy level crossing the quasi Fermi level at the strong inversion condition, namely $E_{it} \in [E_c, E_i + q_0\psi_B]$. $E_i + q_0\psi_B$ is the lowest limit of the energy level that can be determined from the emission current of a TDRC measurement. Typically, for a high resistivity n-type silicon with a doping concentration of 10^{12} cm^{-3}, the deepest level in the silicon band gap that can be determined from the emission current of a TDRC measurement is ~ 0.65 eV with respect to the conduction band. However, if the capture cross section of electrons is of the same order of the capture cross section of holes, the condition $e_n(E_{it}) \gg e_p(E_{it})$ can only be satisfied for the levels in the upper half of the band gap so that the deepest level can be determined is at E_i. For a continuous distribution, the energy level E_{it} of an interface state relative to the conduction band energy E_c is related to the temperature T by [29, 30],

$$E_c - E_{it} = 10^{-4} T \cdot \left[1.92 \cdot \log_{10}\left(\frac{v}{\beta}\right) + 3.2 \right] \frac{\text{eV}}{\text{K}} - 0.0155 \cdot \text{eV} \tag{5.5}$$

with the frequency factor $v = N_c v_{th} \sigma_n$. σ_n is the capture cross section for electrons, for which a T^{-2} dependence is usually assumed, v_{th} is the average thermal velocity of electrons and N_c is the density of states in the conduction band of silicon.

The interface-states density $D_{it}(E_{it})$ is obtained from $I_{tdrc}(T)$ according to [29, 30]

$$D_{it}(E_{it}) = \frac{I_{tdrc}(T)}{q_0 \cdot A_{gate} \cdot \beta \cdot 10^{-4} \cdot \left[1.92 \cdot \log_{10}\left(\frac{v}{\beta}\right) + 3.2 \right] \frac{\text{eV}}{\text{K}}} \tag{5.6}$$

with q_0 the elementary charge, and A_{gate} the gate area of the MOS capacitor.

Generation At sufficiently high temperatures, the surface-generation process dominates. This is illustrated in figure 5.2(d). Both the bulk-generation current and surface-generation current contribute to the measurement at high temperatures. The relations between E_{it} and T, and $D_{it}(E_{it})$ and $I_{tdrc}(T)$ are [31]

$$E_c - E_{it} = 10^{-4} T \cdot \left[1.98 \cdot \log_{10}\left(\frac{v}{\beta}\right) + 4.6 \right] \frac{\text{eV}}{\text{K}} + 0.025 \cdot \text{eV} \tag{5.7}$$

and

$$D_{it}(E_{it}) = \frac{I_{tdrc} \cdot T}{q_0 \cdot A_{gate} \cdot \beta \cdot E_g} \tag{5.8}$$

where E_g is the band gap of silicon, E_g = 1.12 eV at room temperature.

The formulae (5.5)-(5.8) are valid for $C_{ox} \gg C_d$, where C_{ox} and C_d are the oxide capacitance and the depletion capacitance of silicon, respectively.

In case the distribution of interface-states density $D_{it}(E_{it})$ is determined, the interface-trap density N_{it} is obtained by integrating $D_{it}(E_{it})$ throughout the silicon band gap:

$$N_{it} = \int_{E_v}^{E_c} D_{it}(E_{it}) \mathrm{d}E_{it} \tag{5.9}$$

More details on the TDRC technique, detailed derivation of the above formulae and associated constants in the formulae can be found in [29–32].

The assumptions used in the extraction of the distribution of the interface-states density will be discussed in detail in chapter 8.

5.2.2. TDRC set-up and measurement procedure

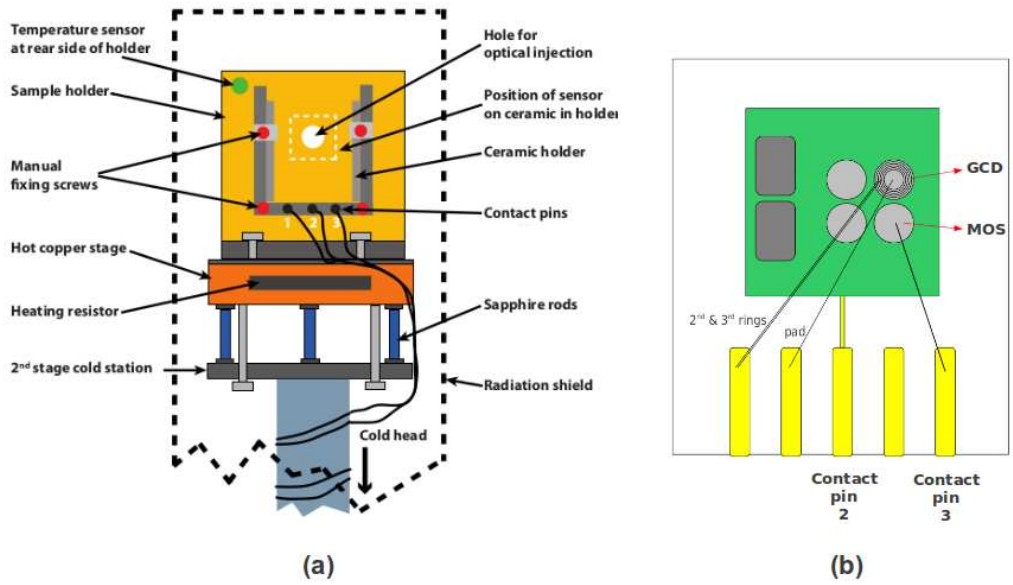


Figure 5.3: The cryostat of the TDRC setup (a) and the ceramic plate supporting the sample (b). The contact pins 2 and 3 are connected to the rear side and the gate of the MOS capacitor, respectively. The contact pin 1 is connected to ground.

The TDRC measurements are usually performed in a temperature range between < 30 K and 290 K. The MOS capacitor is cooled to a temperature < 30 K biased in accumulation to fill the interface traps with majority carriers. Then a negative voltage

to bias the structure in deep depletion is applied and the sample is heated to 290 K with a constant rate of β while measuring the current I_{tdrc} due to the emission of trapped charges.

Figure 5.3(a) and (b) show the cryostat (inner part) of the TDRC set-up and one test field consisting of a MOS capacitor glued onto a ceramic support. The contact pins 2 and 3, which contact the rear side and the gate of the MOS capacitor, are connected to the voltage-output and current-input terminals of a Keithley 487 pico-ammeter/voltage-source-meter. The contact pin 1 in the setup is connected to ground. The temperature is regulated via a Lakeshore 340 temperature controller associated with a helium cooling system. Details on the TDRC set-up can be found in [14].

6. Model calculation for MOS capacitors

The oxide charges and interface traps introduced by X-rays change the electrical properties of MOS capacitors. The former cause a shift in gate voltage of C/G-V curves; while the latter not only shift the entire curves (depending on the energy level of the interface states with respect to the quasi Fermi level of silicon) but also influence the slope and frequency dependence of the curves. The capacitance and conductance as function of the gate voltage is influenced by the oxide-charge density N_{ox}, the distribution of the interface-states density $D_{it}(E_{it})$ and the capture cross section of the interface trap. In this chapter, an equivalent circuit model of the MOS capacitor including contributions from oxide charges and interface traps will be described and analytic expressions of capacitances and conductances of elements in the RC circuit will be given. Comparisons of the C/G-V curves from the model calculation and the TCAD simulation have been made. Based on this model, the influence of interface traps on the C/G-V curves has been studied in detail.

6.1. Specification of the model

The concept of the equivalent circuit has proven to be very powerful to describe and analyse electrical properties of semiconductor devices. Several early papers from K. Lehovec [33, 34] and S. R. Hofstein [35] attempted to use an equivalent circuit to calculate the capacitance and conductance of the MOS capacitor as function of voltage and frequency. Later, details on the equivalent circuit for the MOS capacitor and explanations of the meaning of the RC elements in the band diagram of silicon have been discussed and summarized by Nicollian and Brews [16].

The MOS capacitor can be represented by a simplified equivalent circuit model, as shown in figure 6.1. The symbols of the RC elements in the circuit are described in table 6.1. The expressions of the RC elements in the following are given for the n-type MOS capacitor. Different from a complete model for the MOS capacitor, the charge exchange between interface traps and the valence band of silicon [16] has been omitted in this model. This process only influences the values of the capacitance and the conductance of the MOS capacitor biased approaching strong inversion.

6.1.1. The capacitance and conductance of the insulator

The capacitance of the insulator, C_{ox}, is related to the gate area A, relative dielectric constant ε_{ox} and thickness t_{ox} of the insulator:

$$C_{ox} = \varepsilon_0 \varepsilon_{ox} \frac{A}{t_{ox}} \tag{6.1}$$

with ε_0 the dielectric constant of the vacuum.

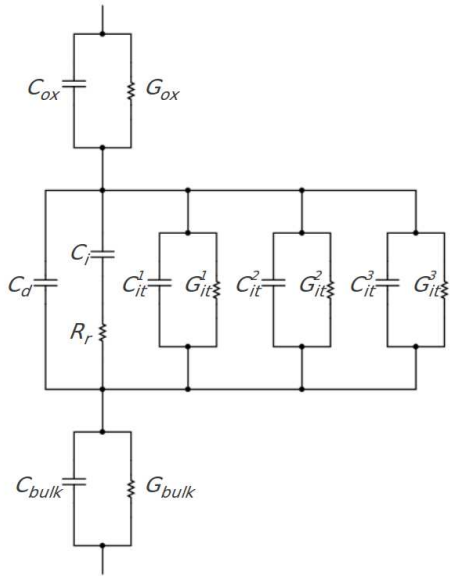


Figure 6.1: Equivalent circuit model of the MOS capacitor, shown with 3 interface traps included.

The conductance of the insulator G_{ox} is due to the leakage current and the AC-signal loss in the insulating layer. For a perfect insulator, $G_{ox} = 0$ S. In the present model, G_{ox} is considered as a free parameter. Its value can be determined from the frequency dependence of the series resistance of the MOS capacitor measured in accumulation.

6.1.2. The capacitance of the depletion layer and inversion capacitance

The capacitance of the depletion layer below the Si-SiO_2 interface, C_d, is approximated by the high frequency silicon surface capacitance, which can be calculated using the

Symbol	Explanation
C_{ox}	capacitance of the insulator
G_{ox}	conductance of the insulator
C_d	capacitance of the depletion layer
C_i	inversion capacitance
R_r	recombination/generation resistance
C_{it}^i	capacitance due to interface traps i
G_{it}^i	conductance due to interface traps i
C_{bulk}	capacitance of the non-depleted silicon bulk
G_{bulk}	conductance of the non-depleted silicon bulk

Table 6.1: Symbols in the equivalent circuit model of the MOS capacitor.

Lindner approximation [36, 37]:

$$C_d\left(\psi_s\right) = \begin{cases} \frac{C_{FBS}\cdot\frac{\psi_s}{|\psi_s|}\cdot\left[\exp\left(\frac{q_0\psi_s}{k_BT}\right)-1\right]}{\sqrt{2\left[-\frac{q_0\psi_s}{k_BT}-1+\exp\left(\frac{q_0\psi_s}{k_BT}\right)\right]}} & \frac{q_0\psi_s}{k_BT} > v_m \\ \frac{C_{FBS}\cdot\frac{v_m}{|v_m|}\cdot\left[\exp(v_m)-1\right]}{\sqrt{2\left[-v_m-1+\exp(v_m)\right]}} & \frac{q_0\psi_s}{k_BT} \leq v_m \end{cases} \tag{6.2}$$

where ψ_s is the band bending of the silicon at the Si-SiO_2 interface; v_m the optimal matching point which depends on the doping concentration, $v_m = -2.1 \cdot \ln(N_d/n_i) + 2.08 - 0.75$; n_i the intrinsic carrier density, $n_i = 3.87 \times 10^{16} T^{1.5} \exp\left(\frac{-0.605 \cdot eV}{k_BT}\right)$ cm^{-3} [38]; and C_{FBS} the flatband capacitance of silicon:

$$C_{FBS} = \varepsilon_0\varepsilon_{si}\frac{A}{L_D} = \varepsilon_0\varepsilon_{si}\frac{A}{\sqrt{\frac{k_BT\varepsilon_0\varepsilon_{si}}{q_0^2N_d}}} \tag{6.3}$$

with L_D the Debye length.

C_i is the inversion capacitance due to the minority carriers accumulating at the Si-SiO_2 interface:

$$C_i\left(\psi_s\right) = \frac{\partial Q_p}{\partial \psi_s} = \frac{\partial\left(Q_s - Q_d\right)}{\partial \psi_s} = \frac{\partial Q_s}{\partial \psi_s} - \frac{\partial Q_d}{\partial \psi_s} = C_s - C_d \tag{6.4}$$

with Q_p and Q_d the charges below the Si-SiO_2 interface due to minority carriers and depletion. Q_s is the total space charge below the interface, which can be calculated by solving the Poisson equation and applying Gauss's law [8], with the assumptions that the densities of free electrons and holes in the depletion layer equal to zero and charge neutrality prevails beyond the depletion layer edge:

$$Q_s\left(\psi_s\right) = \mp\frac{\sqrt{2}\epsilon_0\epsilon_{si}k_BTA}{q_0L_D}F\left(\frac{q_0\psi_s}{k_BT}, \frac{n_i^2}{N_d^2}\right) \tag{6.5}$$

with the negative sign for $\psi_s \geqslant 0$ and the positive sign for $\psi_s < 0$, and

$$F\left(\frac{q_0\psi_s}{k_BT}, \frac{n_i^2}{N_d^2}\right) = \sqrt{\left[\exp(\frac{q_0\psi_s}{k_BT}) - \frac{q_0\psi_s}{k_BT} - 1\right] + \frac{n_i^2}{N_d^2}\left[\exp(-\frac{q_0\psi_s}{k_BT}) + \frac{q_0\psi_s}{k_BT} - 1\right]} \tag{6.6}$$

The derivative of $Q_s(\psi_s)$ equals to C_s, which is the silicon surface capacitance due to total space charge below the Si-SiO_2 interface, as seen in formula (6.4).

Figure 6.2 shows C_d, C_i and C_s as function of the band bending for doping concentrations of 1×10^{11} cm^{-3}, 1×10^{12} cm^{-3} and 1×10^{13} cm^{-3}. In accumulation, C_s and C_d depend exponentially on ψ_s and C_i is negligible because of the low density of minority carriers below the Si-SiO_2 interface. In strong inversion, C_s and C_i depend exponentially on ψ_s and C_d is constant because the width of the depletion layer does not increase further with the decreasing band bending.

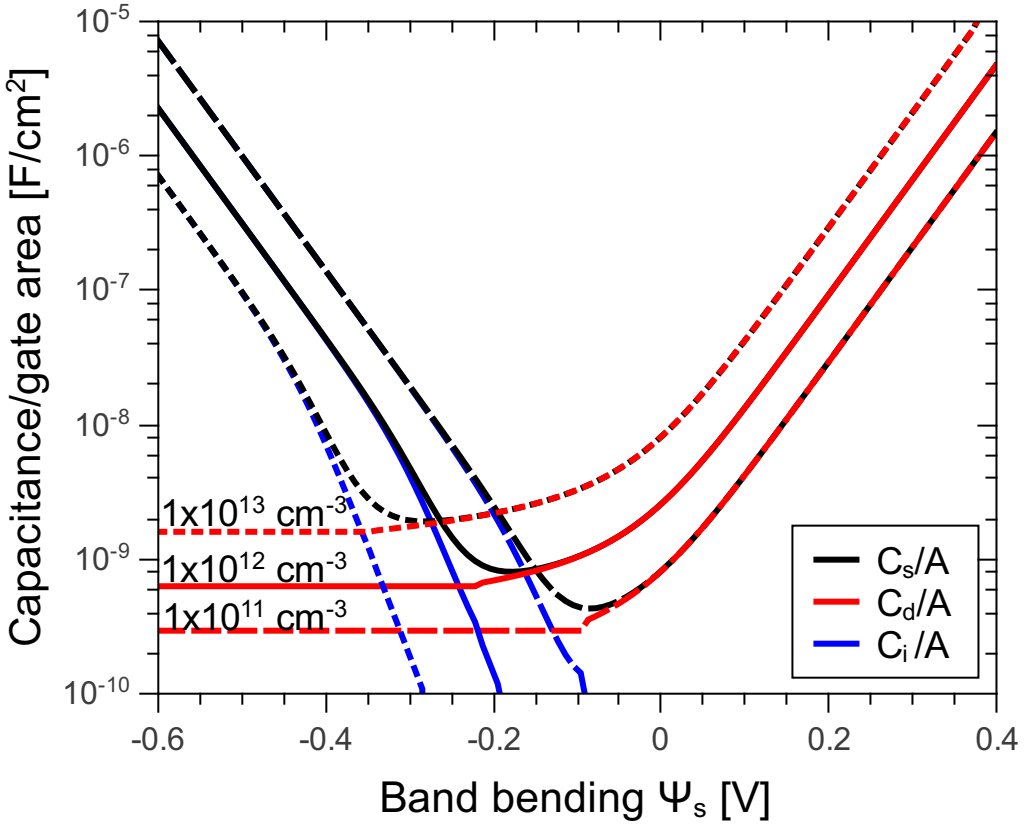


Figure 6.2: The capacitance of the depletion layer C_d, the inversion capacitance C_i and the surface capacitance C_s as a function of band bending ψ_s for $N_d = 1 \times 10^{11}$ cm^{-3}, 1×10^{12} cm^{-3} and 1×10^{13} cm^{-3}.

6.1.3. The recombination/generation resistance

The recombination/generation resistance R_r supplies minority carriers to the inversion layer at the Si-SiO_2 interface with two components [39]:

$$R_r(\psi_s, f) = \frac{1}{G_{qnr}(\psi_s, f) + G_{scr}(\psi_s, f)} \tag{6.7}$$

where $G_{qnr}(\psi_s, f)$ and $G_{scr}(\psi_s, f)$ are the recombination conductance due to the diffusion of minority carriers in the quasi neutral region of silicon and the generation conductance due to the traps in the space charge region of silicon, respectively.

The recombination conductance $G_{qnr}(\psi_s, f)$ is given by [39,40]:

$$G_{qnr}(\psi_s, f) = \frac{q_0 A \mu_p n_i^2}{N_d L_p^{eff}} \tag{6.8}$$

with μ_p the mobility of minority carriers. The effective diffusion length of minority carriers L_p^{eff} is [41,42]:

$$L_p^{eff}(f) = L_p \frac{cosh(\alpha) + \left(s_1 L_p / D_p\right) sinh(\alpha)}{\left(s_1 L_p / D_p\right) cosh(\alpha) + sinh(\alpha)} \tag{6.9}$$

with $\alpha = W_B / L_p$. W_B is the width of the quasi neutral region of the silicon bulk: $W_B(\psi_s) = t_{si} - W_d(\psi_s)$. t_{si} and W_d are the thickness of the silicon bulk and the width of the depletion layer. W_d can be approximated by $W_d(\psi_s) = \epsilon_0 \epsilon_{si} A / C_d(\psi_s)$[1]. s_1 is the surface-generation velocity at the rear contact of the MOS capacitor; D_p the diffusion coefficient. L_p is the diffusion length of minority carriers, $L_p = \sqrt{D_p \tau_p}$, where τ_p is the lifetime of minority carriers. In the presence of an external AC voltage, the lifetime of minority carriers is given by [39]:

$$\tau_p(f) = \frac{\tau_p^0}{1 + j\omega\tau_p^0} \tag{6.10}$$

where τ_p^0 is the lifetime of minority carriers without the external AC signal; ω the angular frequency, $\omega = 2\pi f$. The formula (6.10), can be derived from the AC continuity equation [43].

The generation conductance $G_{scr}(\psi_s, f)$ is given by [39]:

$$G_{scr}(\psi_s, f) = \frac{2\varepsilon_0 \varepsilon_{si} A n_i}{\tau_g N_d W_d} \tag{6.11}$$

where τ_g is related to the generation lifetime. It is given by [39]:

$$\tau_g(f) = \frac{\tau_g^0}{1 + j\omega\tau_g^0} \tag{6.12}$$

The generation lifetime τ_g^0 is given by [44]:

$$\tau_g^0 = \tau_p^0 \exp\left(\frac{E_t - E_i}{k_B T}\right) + \tau_n^0 \exp\left(-\frac{E_t - E_i}{k_B T}\right) \tag{6.13}$$

with τ_n^0 the lifetime of majority carriers, E_t the energy level of traps in the depletion region of silicon bulk and E_i the intrinsic Fermi level.

Figure 6.3 shows the recombination conductance G_{qnr} and generation conductance G_{scr} as function of band bending ψ_s for f = 1 kHz, 10 kHz, 100 kHz and 1 MHz according to formulae (6.8) and (6.11). In this calculation, both of the lifetimes of the majority and the minority carriers are assumed to be 600 μs; energy level of the traps in the depletion region of silicon $E_t = E_g/2$; the doping concentration $N_d = 1 \times 10^{12}$ cm^{-3}; the thickness of the silicon bulk $t_{si} = 285$ μm; surface-generation velocity at the rear contact of the MOS capacitor $s_1 = 8$ cm/s. It can be seen, for these parameters, the recombination conductance G_{qnr} dominates the recombination/generation resistance

[1] Another approximation for W_d is also commonly used, which can be written as $W_d(\psi_s) = \sqrt{\frac{2\epsilon_0 \epsilon_{si} |\psi_s|}{q_0 N_d}}$. The two approximations cause a difference in G_{scr} for $\psi_s \geqslant 0$. As the branch consisting of C_i and R_r in the RC-circuit model is open in this situation, the two approximations make no difference on the total capacitance and conductance of the entire circuit.

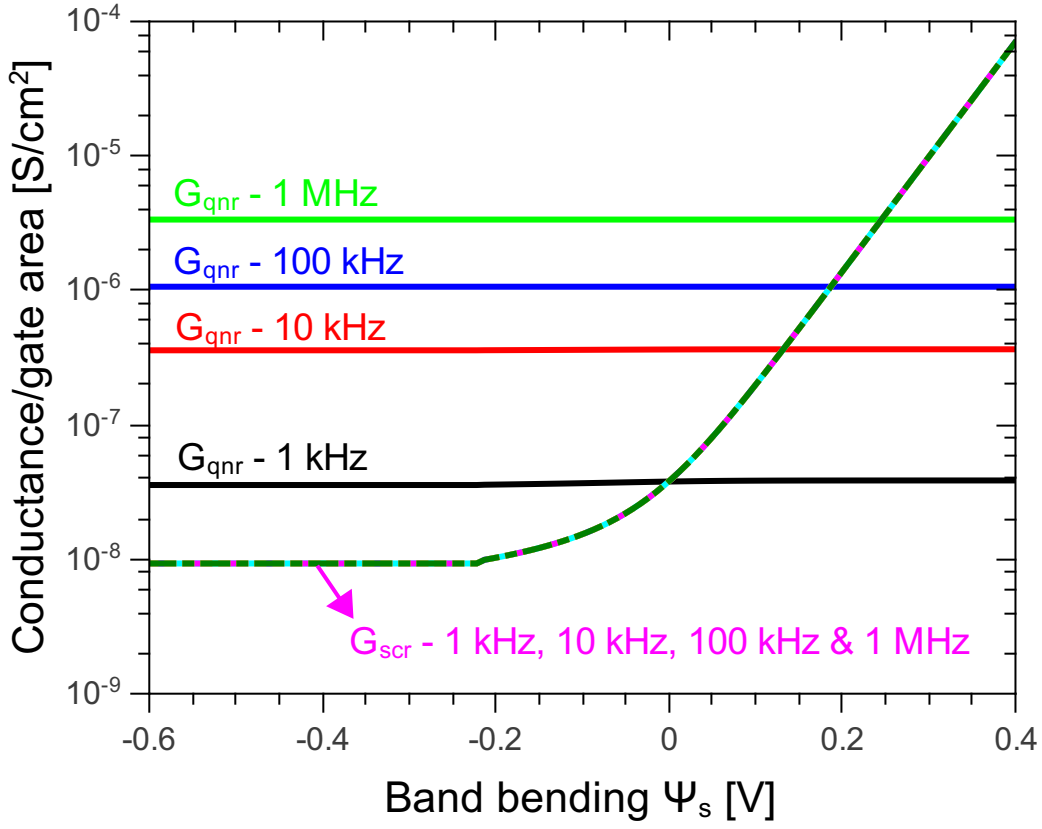


Figure 6.3: The recombination conductance G_{qnr} and generation conductance G_{scr} as a function of band bending ψ_s for $f = 1$ kHz, 10 kHz, 100 kHz and 1 MHz. The lifetimes of majority and minority carriers are assumed to be 600 μs; $E_t = E_g/2$; $N_d = 1 \times 10^{12}$ cm^{-3}; $t_{si} = 285$ μm; $s_1 = 8$ cm/s. It should be noted that the values of G_{scr} calculated in accumulation has no physics meaning as the width of the depletion layer in accumulation actually is zero. The result of G_{scr} in accumulation is only given under the approximation for W_d.

R_r and its frequency dependence in the inversion and depletion region ($\psi_s < 0$). In the accumulation region ($\psi_s > 0$), the branch consisting of the inversion capacitance C_i and the recombination/generation resistance R_r in the model are approximately open (disconnected) due to the value of C_i is extremely small.

The generation velocity at the rear contact of the MOS capacitor s_1 is important when the width of the quasi neutral region of the silicon bulk W_B is of the order of or less than the diffusion length of the minority carriers. For a silicon sensor without bulk damage, the lifetime of the minority carriers is typically of the order of $\sim$ ms. The diffusion length of the minority carriers is about several mm, which are larger than the width W_B. Hence, s_1 is important for high resistivity silicon sensor with a typical thickness of $\sim$ 300 μm. The value of s_1 is related to the doping concentration of n^+-implant at the rear side. The value of s_1 is obtained from a comparison of calculated conductance and simulated conductance by TCAD with the same parameters

as input.

6.1.4. The capacitance and conductance due to interface traps

As a function of ψ_s, assuming that charge carriers are only exchanged between interface traps and the conduction band of silicon, the capacitance $C_{it}(\psi_s, f)$ and conductance $G_{it}(\psi_s, f)$ due to interface traps are [45, 46]

$$C_{it}\left(\psi_s, f\right) = \frac{q_0^2 A}{k_B T} \int_0^{E_g} D_{it}\left(E_{it}\right) \frac{f_{it}^0\left(E_{it}, \psi_s\right)\left(1 - f_{it}^0\left(E_{it}, \psi_s\right)\right)}{1 + \omega^2 \tau\left(E_{it}, \psi_s\right)^2} dE_{it} \tag{6.14}$$

$$G_{it}\left(\psi_s, f\right) = \frac{q_0^2 A \omega^2}{k_B T} \int_0^{E_g} D_{it}\left(E_{it}\right) \tau\left(E_{it}, \psi_s\right) \frac{f_{it}^0\left(E_{it}, \psi_s\right)\left(1 - f_{it}^0\left(E_{it}, \psi_s\right)\right)}{1 + \omega^2 \tau\left(E_{it}, \psi_s\right)^2} dE_{it} \tag{6.15}$$

with the probability of a trap being occupied with an electron (occupation probability)

$$f_{it}^0\left(E_{it}, \psi_s\right) = \frac{1}{1 + \exp\left(\frac{-(E_c - E_{it}) - q_0\psi_s - E_F}{k_B T}\right)} \tag{6.16}$$

$$\tau\left(E_{it}, \psi_s\right) = \frac{1}{\sigma_{it}^e v_{th} N_d} \frac{1}{\exp\left(\frac{q_0\psi_s}{k_B T}\right) + \exp\left(\frac{-(E_c - E_{it}) - E_F}{k_B T}\right)} \tag{6.17}$$

where E_F is the quasi Fermi level, $E_F = k_B T \ln(N_d / N_c)$; σ_{it}^e the electron capture cross section of the interface trap.

6.1.5. The capacitance and conductance of the non-depleted silicon

The capacitance and conductance of the non-depleted silicon bulk $C_{bulk}(\psi_s)$ and $G_{bulk}(\psi_s)$ can be determined by

$$C_{bulk}(\psi_s) = \varepsilon_0 \varepsilon_{si} \frac{A}{t_{si} - W_d(\psi_s)} \tag{6.18}$$

$$G_{bulk}(\psi_s) = \frac{1}{R_{bulk}(\psi_s)} = q_0 \mu_n N_d \frac{A}{t_{si} - W_d(\psi_s)} \tag{6.19}$$

The $C_{bulk}R_{bulk}$ time constant, which is the dielectric relaxation time, is important when the lifetime is on the order of the relaxation time [39]. $C_{bulk}(\psi_s)$ only causes a reduction of the high frequency ($\sim$ 1 MHz) series capacitance of the entire circuit, which is only relevant for high resistivity material.

6.1.6. The admittance of the entire circuit

The total admittance of the entire equivalent circuit Y_{tot} is calculated by

$$Y_{tot}\left(\psi_s, f\right) = \frac{Y_{ox} Y_{sc} Y_{bulk}}{Y_{ox} Y_{sc} + Y_{sc} Y_{bulk} + Y_{bulk} Y_{ox}} \tag{6.20}$$

with $Y_{ox} = G_{ox} + j\omega C_{ox}$, $Y_{sc} = G_{it} + j\omega\left(C_{it} + C_d\right) + 1/\left(R_r + 1/j\omega C_i\right)$ and $Y_{bulk} = G_{bulk} + j\omega C_{bulk}$.

The total parallel capacitance C^p_{tot} and conductance G^p_{tot} are extracted from the imaginary and real parts of Y_{tot} respectively: $Y_{tot} = G^p_{tot} + j\omega C^p_{tot}$. The extracted values of C^p_{tot} and G^p_{tot} will be compared with the values from TCAD simulations in the next section and with the results from measurements in the following chapters.

6.1.7. Relation between gate voltage and band bending

The relation between the voltage V_g applied to the gate, and the band bending ψ_s in steady-state conditions is [16,45]

$$V_g\left(\psi_s\right) = \psi_s + \phi_{ms} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_s\left(\psi_s\right)}{C_{ox}} - \frac{Q_{it}\left(\psi_s\right)}{C_{ox}} \tag{6.21}$$

where ϕ_{ms} is the work function difference between the gate and silicon, Q_{ox} the oxide charges in the insulator and Q_{it} the charges stored in the interface traps. Q_{it} can be expressed as [16]

$$Q_{it}\left(\psi_s\right) = \begin{cases} -q_0 A \int_0^{E_g} D_{it}\left(E_{it}\right) f^0_{it}\left(E_{it}, \psi_s\right) dE_{it} & for\ acceptors \\ q_0 A \int_0^{E_g} D_{it}\left(E_{it}\right)\left(1 - f^0_{it}\left(E_{it}, \psi_s\right)\right) dE_{it} & for\ donors \end{cases} \tag{6.22}$$

with $D_{it}(E_{it})$ the energy distribution of the interface-states density in the silicon band gap.

6.2. Comparisons between the model calculation and TCAD simulation

Comparisons of C/G-V curves from the model and the calculations using the Finite Element Analysis software - Synopsys TCAD [6] have been made. The main parameters implemented in the model calculation and TCAD simulation are listed in table 6.2.

In the TCAD simulation, a Gaussian distributed profile of phosphorus doping with a peak concentration of 1×10^{19} cm^{-3} and a depth of 1 μm, which is defined as the distance from the peak position to the position where the concentration of the Gaussian-distributed phosphorus doping equals to the uniform doping concentration in the silicon substrate, is placed at the rear side of the MOS capacitor with the aim to reduce the influence of the surface-generation velocity s_1 at the rear contact on the recombination/generation resistance R_r. In the model calculation, the small value $s_1 = 8$ cm/s is used, which gives a good agreement for the frequency dependence of the total parallel conductances G^p_{tot} from the model calculation and the TCAD simulation when the MOS capacitor is biased in strong inversion.

The device simulations of Synopsys TCAD are performed using the Fermi statistics, the drift-diffusion model, the high field saturation and doping dependent mobility model, and the Shockley-Read-Hall (SRH) recombination model.

Parameter	Value
N_d	1×10^{12} cm^{-3}
t_{ox}	377 nm
G_{ox}	0 S
t_{si}	285 μm
T	295 °C
τ_n^0	1 ms
τ_p^0	1 ms
E_t	0.56 eV
N_{ox}	1×10^{12} cm^{-2}
σ_{it}^e	1×10^{-15} cm^2
σ_{it}^h	1×10^{-15} cm^2
E_{it}	-0.05, -0.15, ..., -1.05 eV
N_{it}	1×10^{12} cm^{-2}

Table 6.2: Parameters implemented in the model calculation and TCAD simulation for comparisons: N_{ox} is used for the case oxide charges present and assumed to be at the Si-SiO_2 interface in TCAD simulations. The calculations are done for single interface-trap levels with different energies E_{it} relative to the conduction band of silicon.

All calculated and simulated capacitances and conductances in the following comparisons refer to the total parallel capacitances C_{tot}^p and conductances G_{tot}^p of the equivalent circuit of the MOS capacitor normalised to a gate area of 1 cm^2.

6.2.1. C/G-V curves of MOS capacitors without/with oxide charges

Figure 6.4 shows the comparisons of C/G-V curves (shown in parallel capacitance and conductance) from the model calculation and the TCAD simulation for an ideal MOS capacitor (neither oxide charges nor interface traps included) and for $N_{ox} = 1 \times 10^{12}$ cm^{-2}. A good agreement is found.

As expected, in both calculation, reductions of the total parallel capacitance C_{tot}^p at 100 kHz and 1 MHz compared to the values at frequencies of 1 kHz and 10 kHz are observed in accumulation due to the low doping of the silicon substrate.

For the ideal MOS capacitor, the flatband voltage V_{fb}, defined as the gate voltage when the band bending equals to 0 ($\psi_s = 0$ V), is -0.49 V. For oxide charges $N_{ox} = 1 \times 10^{12}$ cm^{-2}, the flatband voltage V_{fb} shifts to -17.6 V in agreement with the formula (6.21) with $\psi_s = 0$ V.

6.2.2. C/G-V curves of MOS capacitors with a single interface-trap level

To understand the influence of interface traps on the electrical properties of MOS capacitors, the C/G-V curves of the MOS capacitor with a single interface-trap level are calculated and simulated with the following parameters: An oxide-charge density N_{ox} of 1×10^{12} cm^{-2}, an interface trap density N_{it} of 1×10^{12} cm^{-2} and electron and

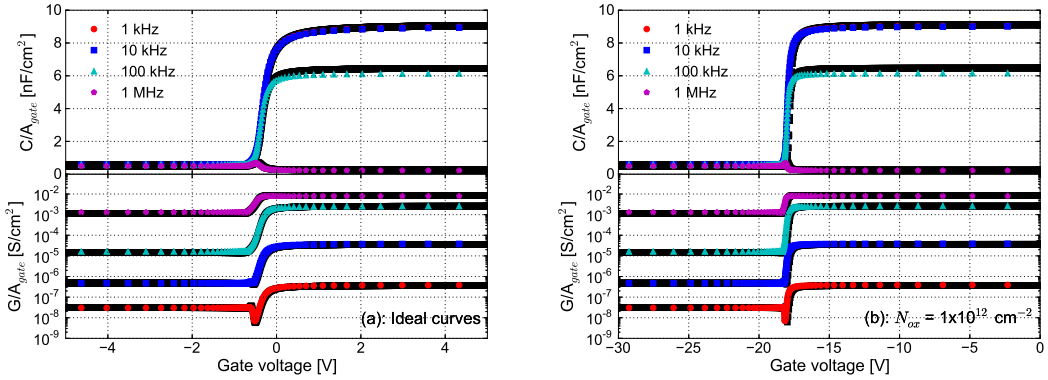


Figure 6.4: Comparisons of C/G-V curves (shown in parallel capacitance and conductance) from the model calculation and the TCAD simulation. Color dots: model calculation; Black lines: TCAD simulation. (a) Ideal C/G-V curves; (b) C/G-V curves for $N_{ox} = 1 \times 10^{12}$ cm^{-2}.

hole capture cross sections of interface traps of 1×10^{-15} cm^2. The energies of single interface-trap levels E_{it} with respect to the conduction band are investigated from -0.05 eV to -1.05 eV with an increment of 0.1 eV. A band gap of 1.12 eV at room temperature is assumed. As seen in figure 6.5, the first column are the results for acceptor traps and the second are the corresponding results for donor traps.

It is observed that the shapes of the C/G-V curves for acceptor traps and donor traps are practically identical. However the curves are shifted by $\triangle V = q_0 N_{it}/C_{ox} =$ 17.6 V. The reason is that, in both the model calculation and the TCAD simulation, the ground state degeneracies for acceptor (g_A) and donor (g_D) are assumed to be the same and equal to 1: $g_A = g_D = 1$. Under this assumption, there is no difference between the capacitances contributed by acceptor traps and donor traps and no difference between the shapes of $Q_{it}(\psi_s)$ for acceptor and donor traps as seen in formula (6.22). Hence, the shapes of the C/G-V curves for acceptor and donor traps are expected to be identical.

The calculated and simulated results in figure 6.5 show that interface traps with a single energy level E_{it} between -0.35 eV and -0.85 eV cause frequency shifts of the total parallel capacitances C^p_{tot} and increases of the total parallel conductances G^p_{tot} in the depletion and weak inversion regions. The C/G-V curves of the MOS capacitor with acceptor traps at the interface whose energy levels are close to the conduction band ($E_c - E_{it} < 0.35$ eV) and those with donor traps whose levels close to the valence band ($E_c - E_{it} > 0.85$ eV) are similar to those without interface trap, which indicates that the levels in such energy region do not affect the electrical properties of the MOS capacitor at room temperature. For acceptor traps with energies close to the valence band and donor traps with energies close to the conduction band, although no shifts of capacitance and increases of conductance are observed, the curves are shifted to a lower gate voltage and to a higher gate voltage by $\triangle V = q_0 N_{it}/C_{ox} = 17.6$ V with respect to those with oxide charges only.

6.2.3. C/G-V curves of MOS capacitors with distributed interface trap

A more realistic case is that the interface traps are distributed over the silicon band gap. Thus, the C/G-V curves of the MOS capacitor are also calculated and simulated with Gaussian distributed interface traps: An interface-states density D_{it}^0 at the location of the peak of 1×10^{13} cm^{-2}eV^{-1} is used; the mean energy $E_{it}^0 = -0.45$ eV and the standard deviation $\sigma_{it}^0 = 0.10$ eV. Results are shown in figure 6.6: The calculated and simulated C/G-V curves show good agreement.

The shift of the gate voltage between C/G-V curves for acceptors and donors is $\triangle V = q_0/C_{ox} \cdot \int_0^{E_g} D_{it}(E_{it})\mathrm{d}E_{it} = q_0/C_{ox} \cdot \int_0^{E_g} D_{it}^0 \exp\left[-\frac{1}{2}\left(\frac{E_{it}-E_{it}^0}{\sigma_{it}^0}\right)^2\right] \mathrm{d}E_{it} = 44.2$ V.

The large frequency shifts and increases of conductance for the Gaussian distributed interface traps with a mean energy of 0.45 eV confirm the previous conclusion that the interface traps located in the region near the centre of the band gap have a strong influence on the electrical properties of the MOS capacitor at room temperature.

6.3. Investigation of "invisible" electrical properties of MOS capacitors

The model calculation provides the possibility to directly investigate the "invisible" electrical properties of the MOS capacitor which cannot be measured: for example, the capacitances and conductances due to interface traps and the time constants of interface traps.

6.3.1. The charge stored in the interface trap

The charge stored in the interface trap as a function of band bending is shown in figure 6.7 for the density of a single interface-trap level $N_{it} = 1 \times 10^{12}$ cm^{-2} and the energies $E_c - E_{it} = 0.05, ..., 1.05$ eV. The acceptor traps are neutral when emptied and negatively charged when occupied by electrons; whereas the donor traps are neutral when occupied and positively charged when emptied. The occupation of the acceptor or donor traps at the interface is given by the Fermi-Dirac statistics.

As seen in figure 6.7, the difference of the charges stored in acceptor and donor traps at the same band bending is $q_0 N_{it}$ under the assumption that both degeneracies for acceptors and donors are the same. Therefore, the gate voltage shift between C/G-V curves of the MOS capacitor with acceptor and donor traps with the same N_{it} is $q_0 N_{it}/C_{ox}$ as observed during the above comparisons.

6.3.2. The interface-trap capacitance, conductance and time constant

The equivalent series capacitance (C_{it}^s) and resistance (R_{it}^s) of the branch consisting of the capacitance (C_{it}) and conductance (G_{it}) in the model (refer to figure 6.1) due to the interface traps give more information.

C_{it}^s and R_{it}^s can be calculated by a simple transformation from a parallel circuit to a series one:

$$C_{it}^s = \frac{G_{it}^2 + \omega^2 C_{it}^2}{\omega^2 C_{it}} \tag{6.23}$$

$$R_{it}^s = \frac{G_{it}}{G_{it}^2 + \omega^2 C_{it}^2} \tag{6.24}$$

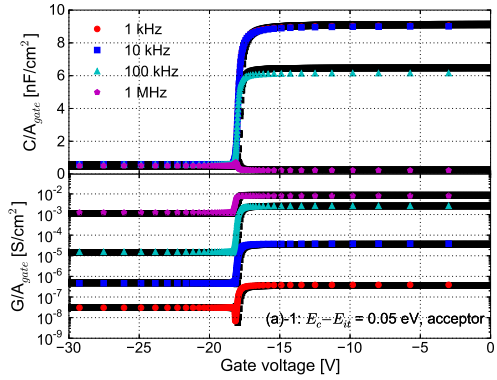
Figure 6.8 and 6.9 shows the band-bending dependence of C_{it}^s, R_{it}^s and $R_{it}^s C_{it}^s$ time constant for single interface-trap levels with a density of 1×10^{12} cm^{-2} and whose energy is varied from -0.05 eV to -1.05 eV. Both C_{it}^s and R_{it}^s do not depend on frequency but only on the band bending. It is seen that C_{it}^s, which is proportional to $N_{it} f_{it}^0 (1 - f_{it}^0)$ [16] reaches the maximum when the quasi Fermi level crosses the energy level of the interface trap, where the interface traps have the largest probability to communicate with both of the majority carriers in the conduction band and the minority carriers in the valence band.

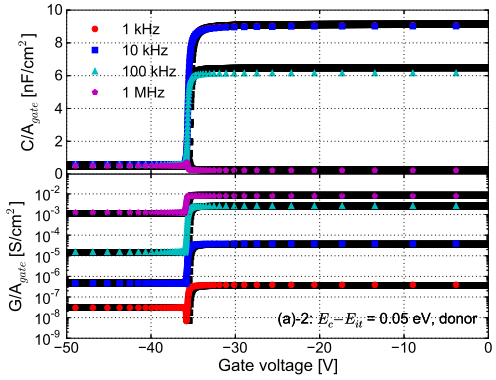
The series resistance of the interface traps $R_{it}^s \sim \left[N_{it} n_s (1 - f_{it}^0)\right]^{-1}$ [16], which reflects the charge exchange of the interface trap with the conduction band, is either almost constant ($\sim \exp\left(\frac{E_c - E_{it}}{k_0 T}\right)$) when the Fermi level is above the energy level of the interface trap, or depends exponentially on the band bending ($\sim \exp\left(-\frac{q_0 \psi_s}{k_0 T}\right)$) when the Fermi level is below. n_s is the density of majority carriers at the interface: $n_s = N_d \exp\left(\frac{q_0 \psi_s}{k_0 T}\right)$ and the time constant of the interface traps is $\tau_{it} = C_{it}^s R_{it}^s \sim f_{it}^0 / n_s$.

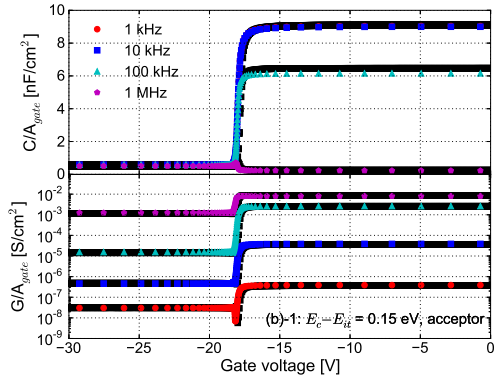
6.4. Summary

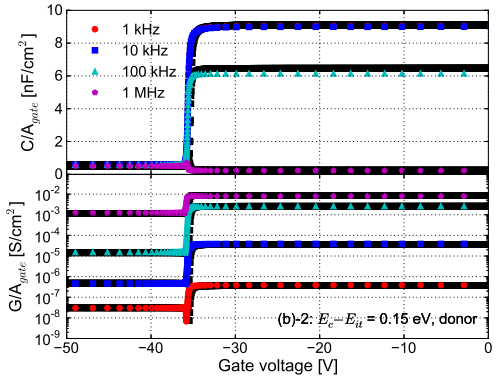
A model for C/G-V curves of the MOS capacitor assuming that the interface traps only exchange charge carriers with the conduction band has been developed. Based on the model, the C/G-V curves of the MOS capacitor with charges in the SiO_2 and traps at the Si-SiO_2 interface can be calculated. In addition, comparisons have been made between model calculations and TCAD simulations. A good agreement in all cases is found. Finally, the electrical properties, i.e. the capacitance, resistance and time constant, of the interface trap have been investigated in detail.

The model calculation will be used in the following to extract the parameters of radiation-induced interface traps and the densities of oxide charges.


1 kHz
10 kHz
100 kHz
1 MHz
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(a)-1: E_c−E_it = 0.05 eV, acceptor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
1 MHz
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(a)-2: E_c−E_it = 0.05 eV, donor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
1 MHz
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(b)-1: E_c−E_it = 0.15 eV, acceptor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
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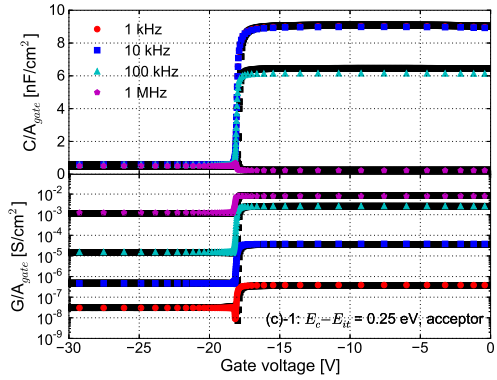
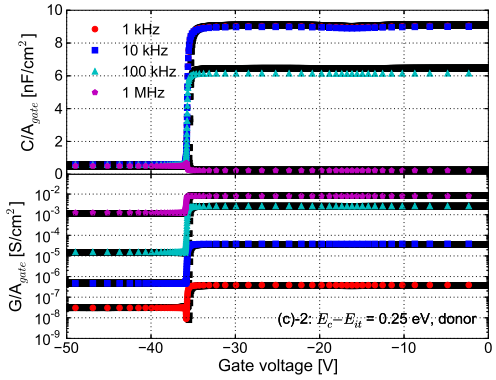
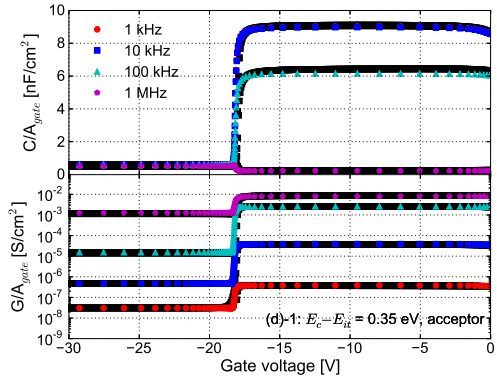
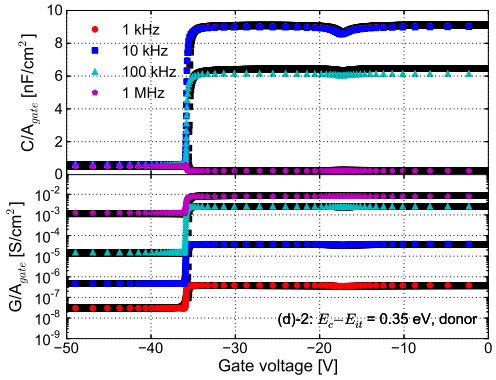
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(b)-2: E_c−E_it = 0.15 eV, donor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
1 MHz
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(c)-1: E_c−E_it = 0.25 eV, acceptor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
1 MHz
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(c)-2: E_c−E_it = 0.25 eV, donor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
1 MHz
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(d)-1: E_c−E_it = 0.35 eV, acceptor
Gate voltage [V]


1 kHz
10 kHz
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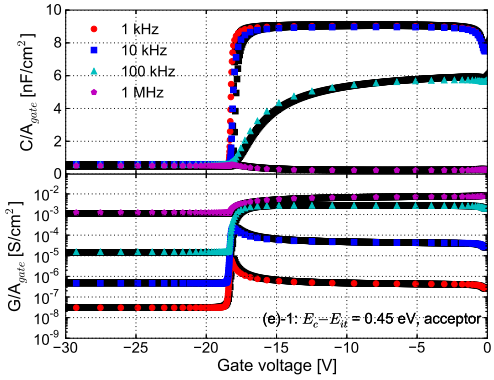
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(d)-2: E_c−E_it = 0.35 eV, donor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
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C/A_gate [nF/cm²]
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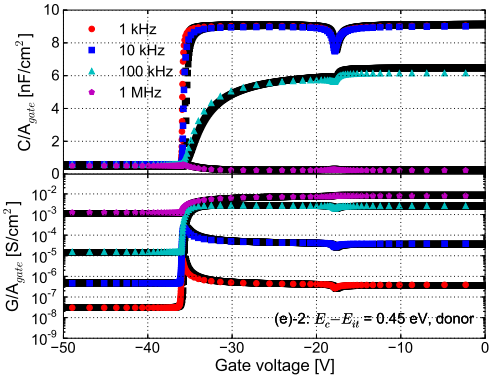
(e)-1: E_c−E_it = 0.45 eV, acceptor
Gate voltage [V]


1 kHz
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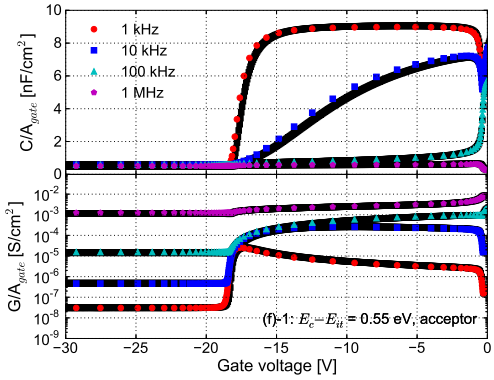
G/A_gate [S/cm²]
(e)-2: E_c−E_it = 0.45 eV, donor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
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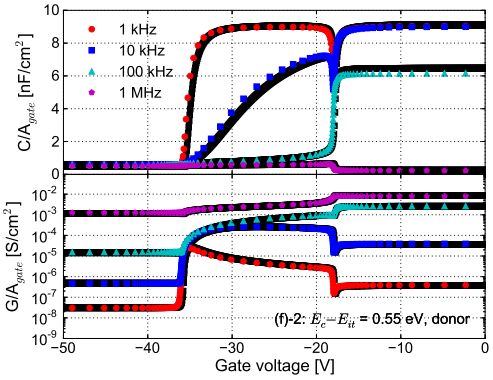
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(f)-1: E_c−E_it = 0.55 eV, acceptor
Gate voltage [V]


1 kHz
10 kHz
100 kHz
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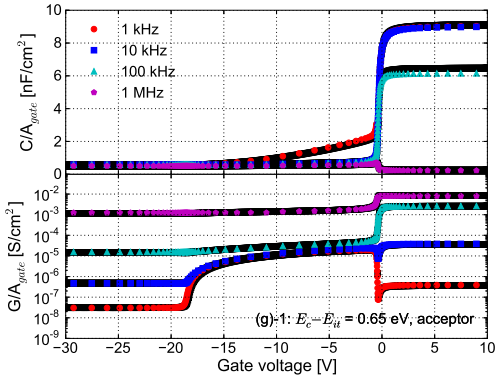
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(f)-2: E_c−E_it = 0.55 eV, donor
Gate voltage [V]


1 kHz
10 kHz
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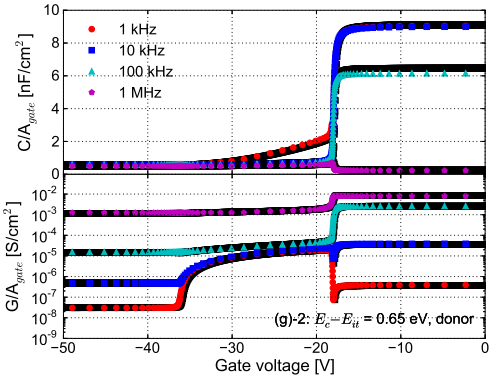
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(g)-1: E_c−E_it = 0.65 eV, acceptor
Gate voltage [V]


1 kHz
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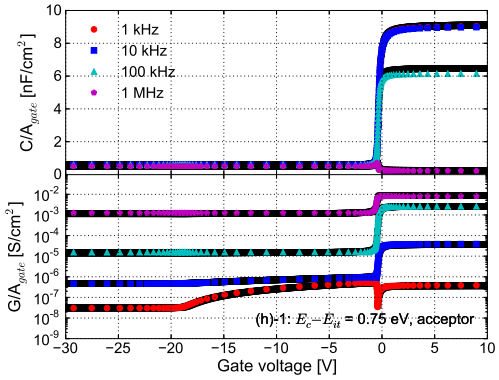
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(g)-2: E_c−E_it = 0.65 eV, donor
Gate voltage [V]


1 kHz
10 kHz
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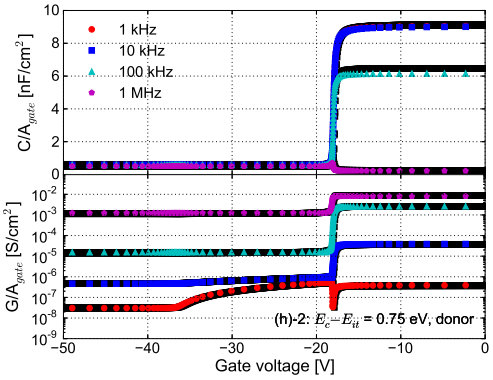
1 MHz
C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(h)-1: E_c−E_it = 0.75 eV, acceptor
Gate voltage [V]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C/A_gate [nF/cm²]
G/A_gate [S/cm²]
(h)-2: E_c−E_it = 0.75 eV, donor
Gate voltage [V]

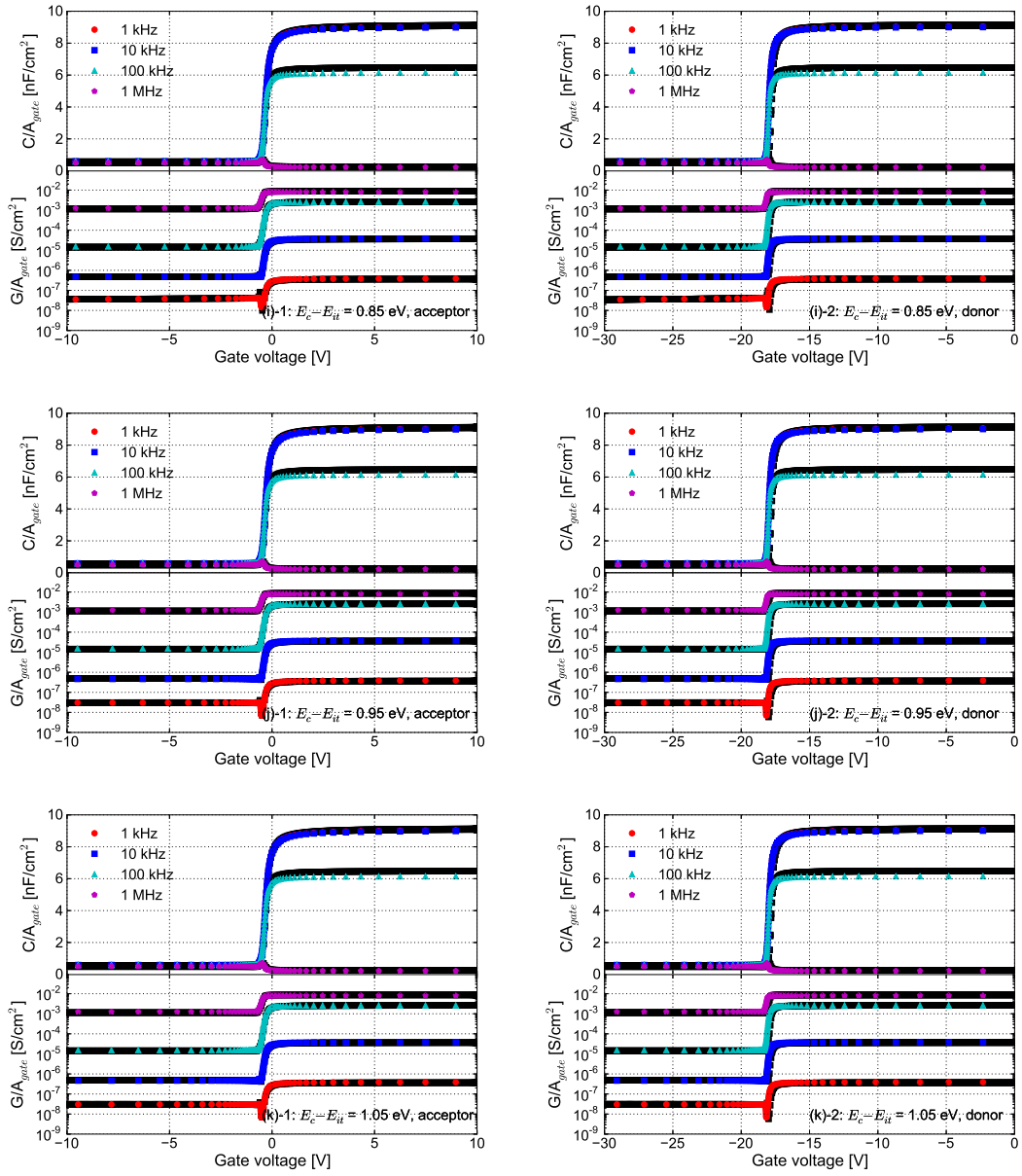

Figure 6.5: Comparisons of C/G-V curves of MOS capacitors with single interface-trap levels. Color dots: model calculation; Black lines: TCAD simulation. 1st column: acceptor traps; 2nd column: donor traps. $N_{ox} = 1 \times 10^{12}$ cm^{-2}, $N_{it} = 1 \times 10^{12}$ cm^{-2} and $E_c - E_{it} = 0.05, ..., 1.05$ eV.

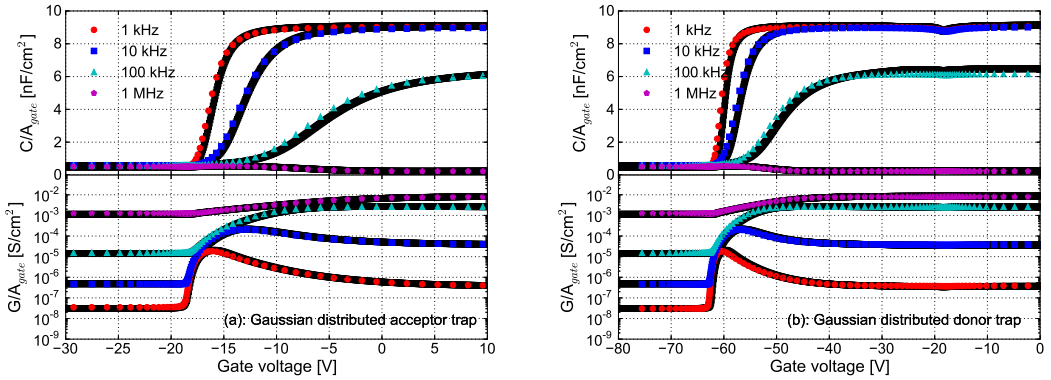

Figure 6.6: Comparisons of C/G-V curves of MOS capacitors with Gaussian distributed interface trap. Color dots: model calculation; Black lines: TCAD simulation. (a) Acceptor trap; (b) Donor trap. $N_{ox} = 1 \times 10^{12}$ cm^{-3}, $D_{it}^{0} = 1 \times 10^{13}$ cm^{-2}eV^{-1}, $E_{it}^{0} = -0.45$ eV and $\sigma_{it}^{0} = 0.10$ eV.

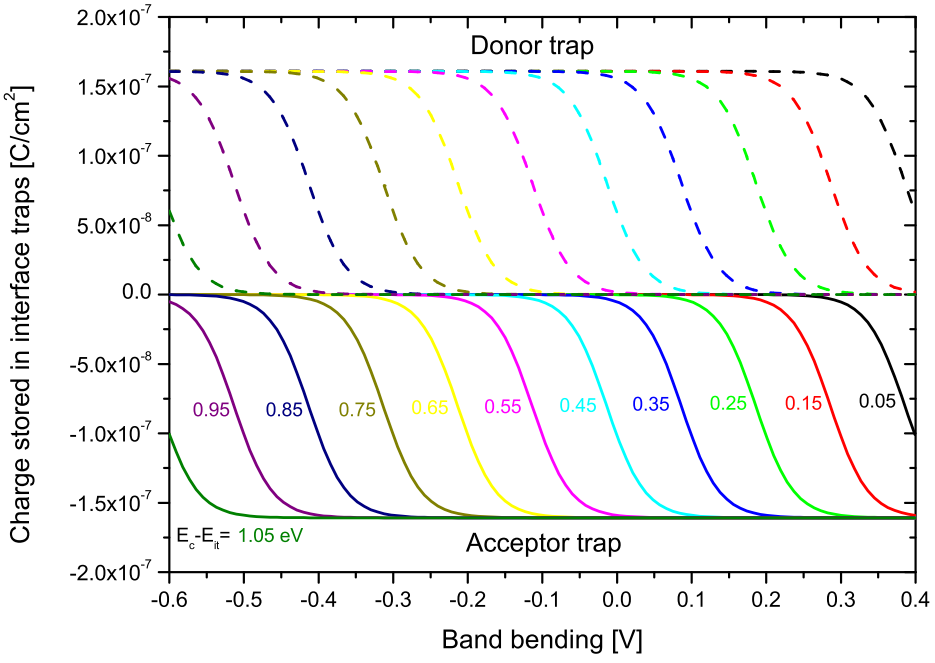

Figure 6.7: The charge stored in the interface trap: $N_{it} = 1 \times 10^{12}$ cm^{-2} and $E_c - E_{it} = 0.05, ..., 1.05$ eV. Lines: acceptor traps; Dashes: donor traps.

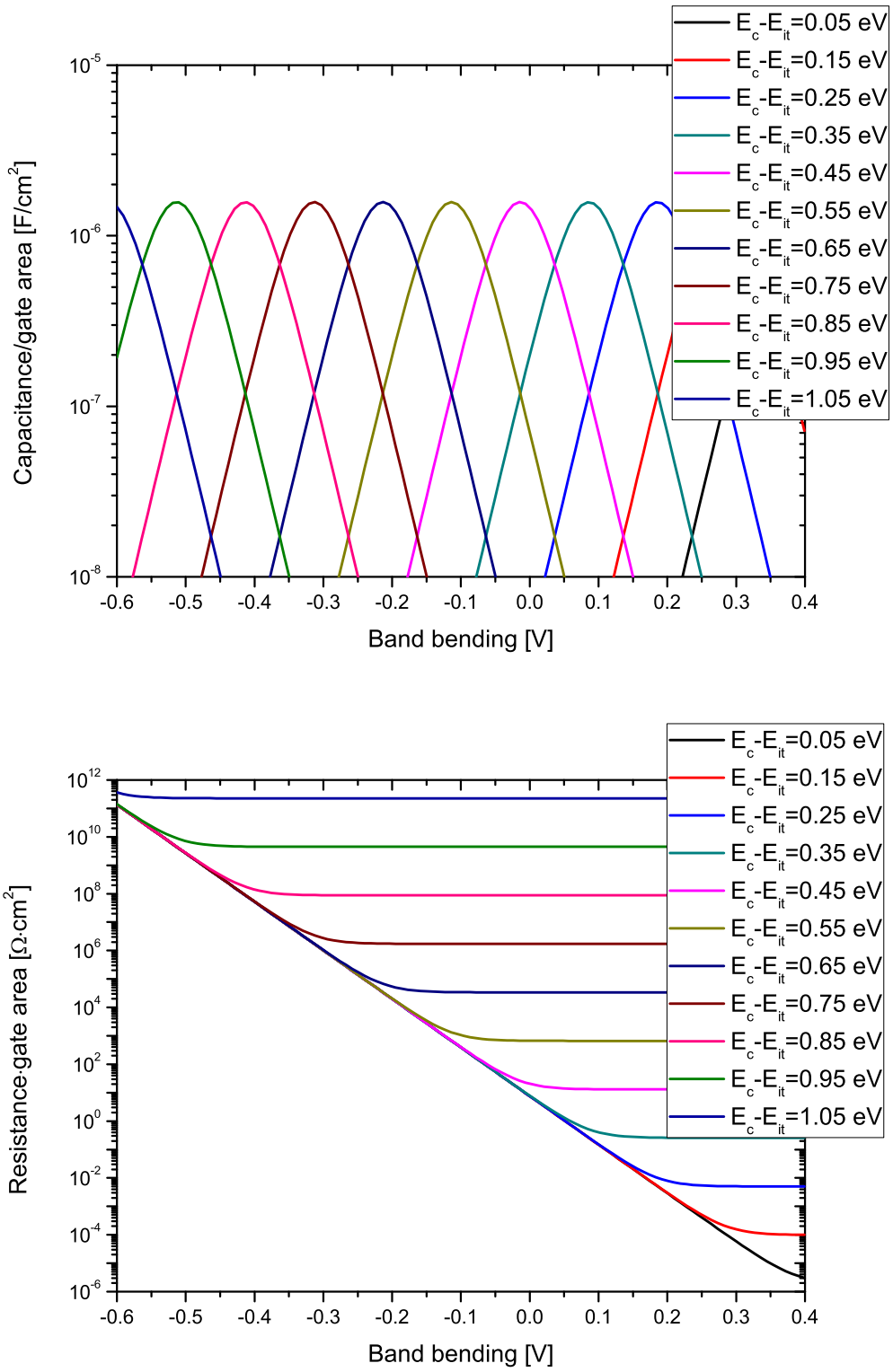

Figure 6.8: The capacitances and resistances of a single interface-trap level: $N_d = 1 \times 10^{12}$ cm^{-3}, $N_{it} = 1 \times 10^{12}$ cm^{-2}, $\sigma_{it}^e = \sigma_{it}^h = 1 \times 10^{-15}$ cm^2 and $E_c - E_{it} = 0.05, ..., 1.05$ eV.

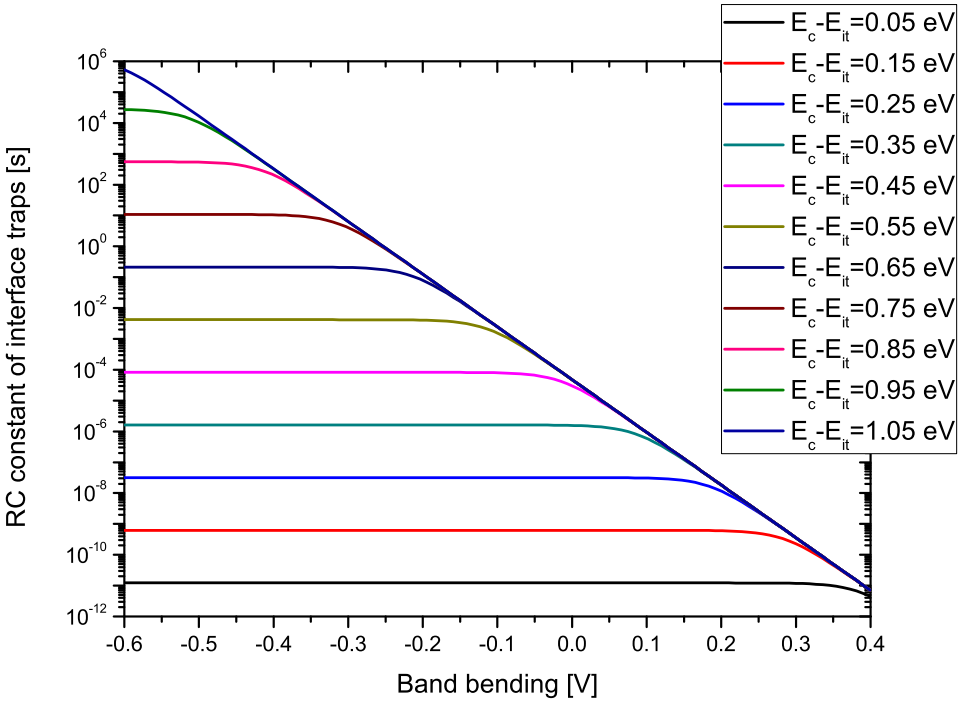

Figure 6.9: The time constants of a single interface-trap level: $N_d = 1 \times 10^{12}$ cm^{-3}, $N_{it} = 1 \times 10^{12}$ cm^{-2}, $\sigma_{it}^e = \sigma_{it}^h = 1 \times 10^{-15}$ cm^2 and $E_c - E_{it} = 0.05, ..., 1.05$ eV.

7. Irradiation procedure

In this chapter, the X-ray irradiation set-up in the F4 beamline at the DORIS III synchrotron light source of DESY is introduced. The beam profile and the detailed procedures to calibrate the dose for silicon devices, i.e. MOS capacitors, gate-controlled diodes and silicon microstrip sensors, are presented.

7.1. Irradiation facility

DORIS III [47] was a dedicated synchrotron radiation source located at the DESY premise. Its circumference and bending radius are 289 m and 12.2 m, respectively. The positron energy in the storage ring and the magnetic field of the bending magnets are 4.45 GeV and 1.2182 T, which results in a radiated power of 420 kW for a positron beam current of 140 mA.

For the irradiations with X-rays, a facility has been set up [26, 48] and used at the beamline F4 of DORIS III. The set-up is shown in figure 7.1. It consists of an adjustable Ta chopper, which permits the reduction of the full dose rate (180 kGy/s) down to 0.5%, an adjustable collimator to precisely define the region of irradiation, and a sample holder made of a ceramic substrate with 5 biasing lines, which is connected to a liquid cooling system to control the temperature in the range of 10 to 30 °C.

The test structures and sensors were glued and wire-bonded to the ceramic substrate, shown at the top left of figure 1. This holder makes the exchange and test of the structures easy and safe.

The set-up is mounted on a table, which permits computer control of both the horizontal and vertical movement of the sample enabling larger areas than the beam spot to be irradiated uniformly. A pneumatic beam shutter, for a precise determination of the exposure time to the beam, was installed close to the exit window of the beam pipe, as seen in figure 7.2. The time needed to open and close the beam shutter is less than 0.1 s. For all irradiations, the shortest exposure time was $\sim$ 5 s, thus the accuracy of exposure time is better than 98%.

7.2. Beam profile

The beamline F4 at DORIS III provides a "white" photon beam from a bending magnet. The energy spectrum was calculated taking into account the X-ray absorption by the materials in the beam line (see figure 7.2 for the materials and their thicknesses). As shown in figure 7.3(a) the typical photon energy at the detector was 12 keV with the full width at half maximum of about 13 keV.

The intensity profile of the X-ray beam was measured by the photocurrent in a silicon pad diode biased to 6 V. The bias voltage applied to the pad diode is determined

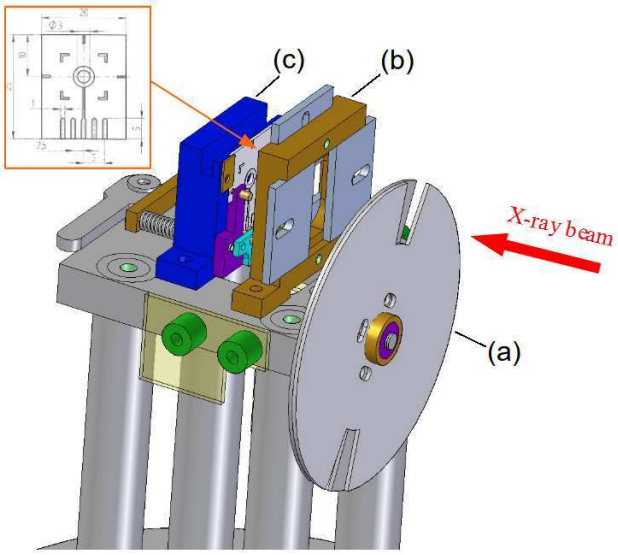

Figure 7.1: Set-up of the irradiation facility: Chopper (a), collimator (b), and sample holder (c) with cooling and spring mechanism. The ceramic substrate which is mounted into the sample holder carries test structures and sensors (shown at the top left). The entire set-up can be moved in all three dimensions by computer control.

from a measurement of the photocurrent as function of the bias voltage. It is found the photocurrent saturates at a very small bias voltage, which is below the full depletion voltage of 35 V. The reason why the full photocurrent can be measured even with a bias voltage below the full depletion voltage is that the minority carriers produced in the non-depleted silicon substrate diffuse to the depletion boundary because their diffusion length is much larger than the thickness of silicon. During the measurement of the photocurrent, the DORIS current was monitored in real time. The pad diode, glued onto a ceramic substrate as shown in figure 7.1, was placed onto the sample holder. The collimator was opened to a window of 0.2 mm $\times$ 0.2 mm. The sample was moved in steps of 0.1 mm to scan the beam. The photon flux entering the sensor as a function of position was calculated from the measured current, the average energy of 3.6 eV to produce one electron-hole pair in silicon and the energy deposited by the photons. The fraction of interacting photons was derived from the energy spectrum and the absorption length of X-rays as a function of energy. The energy spectrum of X-rays is calculated according to the primary energy spectrum of a synchrotron radiation source and the absorption of photons in the materials before reaching the sensor. Figure 7.3(b) shows the measured two dimensional beam profile.

The horizontal and vertical profiles at the center of the beam are shown in figure 7.3(c) and figure 7.3(d). The width of the horizontal profile is about 5 mm and uniform; whereas the full width of half maximum of the vertical profile is 4 mm and Gaussian-like. The distributions are as expected for the synchrotron radiation of the positrons of DORIS III in the bending magnet and the width of the horizontal collimator before the set-up.

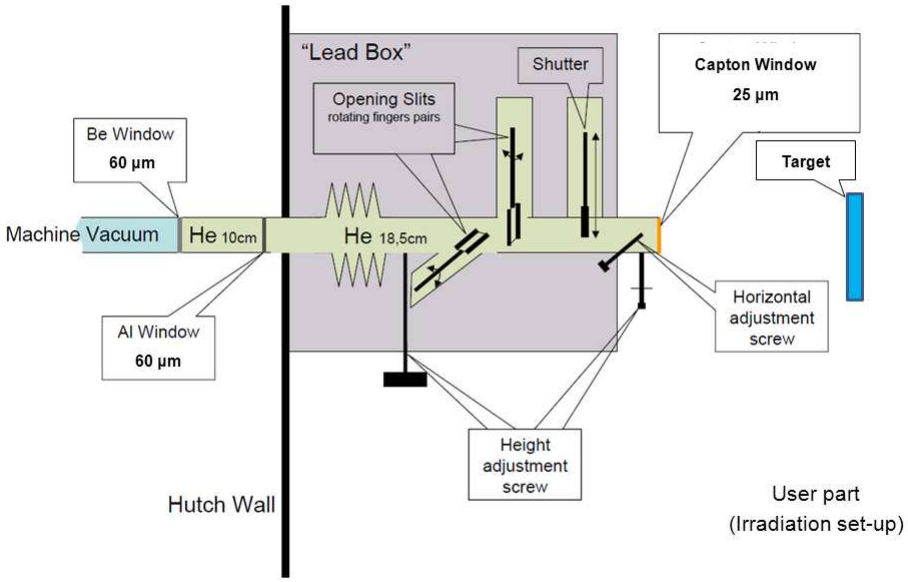

Figure 7.2: Front-end of the beamline F4 of DORIS III. The opening of the two slits in the lead box are adjustable. The user part (irradiation set-up) is exposed to normal air. Private communication by G. Potdevin [49].

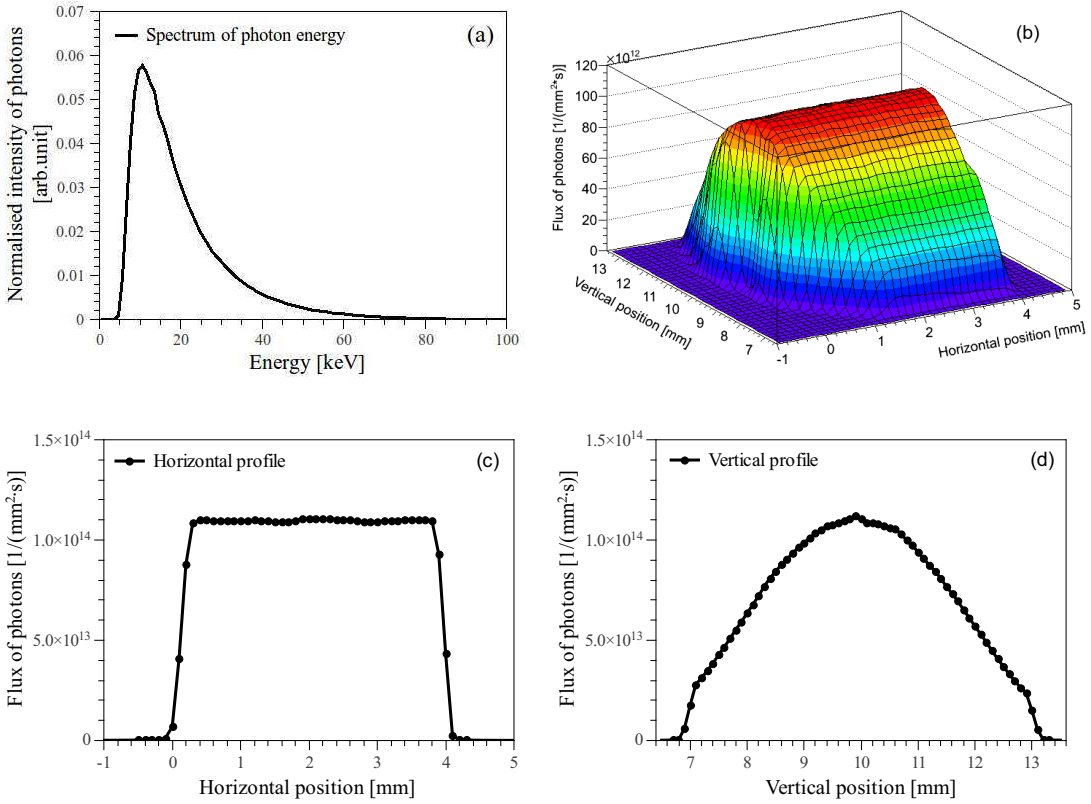

Figure 7.3: (a) Normalised spectrum of photon energy at the entrance of the sensor. (b) Two dimensional beam profile. (c) Horizontal profile. (d) Vertical profile. The beam profile is normalised to a positron beam current of DORIS III $\sim$ 100 mA. The flux of photons in the figure refers to the flux at the entrance of the sensor.

7.3. Calibration of the dose

The dose mentioned throughout this thesis refers to the dose in the SiO_2. The formulae given below are for irradiations of the SiO_2 layer facing to the X-ray beam.

Irradiation with fixed sample

For structures, whose dimensions are much smaller than the beam spot, they can be irradiated simply by centering them on the beam. Using the data shown in figure 7.3(a) the normalised photon spectrum and figure 7.3(b) the two dimensional beam profile, the dose in the SiO_2 insulator of a structure smaller than the dimension of the beam spot can be calculated according to:

$$Dose = \frac{3.6\text{eV} \cdot R \cdot t_{irra}}{q_0 \rho_{Si} d_{Si} \Delta x \Delta y} \iint_{\Delta x, \Delta y} J_{diode}(x, y) \cdot \mathrm{d}x\mathrm{d}y \tag{7.1}$$

with $J_{diode}(x, y)$ the current density (A/mm^2) measured by the silicon diode, t_{irra} the duration of irradiation, ρ_{Si} and d_{Si} the density and thickness of the silicon diode. Δx and Δy are the horizontal and vertical opening of the collimator (equal to the horizontal and vertical extensions of the structure under irradiation) in the plane perpendicular to the X-ray beam and q_0 is the elementary charge. R is the ratio of energy deposited per unit mass in the SiO_2 (E_{SiO_2}) to the energy deposited in the silicon (E_{Si}) for the given photon spectrum:

$$R = \frac{\frac{E_{SiO_2}}{\rho_{SiO_2} \cdot d_{SiO_2}}}{\frac{E_{Si}}{\rho_{Si} \cdot d_{Si}}} \tag{7.2}$$

ρ_{SiO_2} and d_{SiO_2} are the density and thickness of the SiO_2 insulator. The energies deposited in the SiO_2 (E_{SiO_2}) and in the silicon (E_{Si}) are calculated from the energy spectrum of photons at the entrance of the sensor, the absorption lengths of photons in SiO_2 and in Si, and the thicknesses of the SiO_2 layer and the silicon sensor. The values of the absorption lengths of photons in SiO_2 and Si as function of energy are taken from [50, 51] and shown in figure 7.4.

For the given energy spectrum, and d_{SiO_2} = 300 nm and d_{Si} = 300 μm, the value of R is 1.30, which is essentially independent of d_{SiO_2} for the typical oxide thickness of sensors. Without the chopper the typical dose rates in SiO_2 are 180 kGy/s, which corresponds to a flux of approximately 1.1×10^{14} photons/(mm^2 ·s).

It can be seen from figure 7.3(d), the uniformity gets worse when the vertical size of the structure is comparable to the vertical beam profile. For a structure with a height of > 4 mm, the irradiation dose at the edges of the structure are smaller than the dose in the centre by 50%. For a MOS capacitor with a diameter of 1.5 mm, the uniformity of the irradiation with this method is better than 90%. Nevertheless, in order to obtain a more uniform irradiation of the structure, 1-dimensional scan along the vertical direction is always performed for MOS capacitors and gate-controlled diodes.

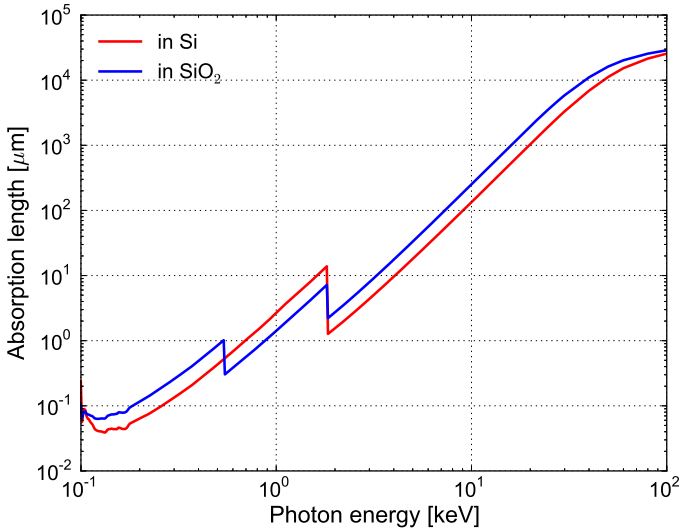

Figure 7.4: The absorption lengths of photons as function of energy in Si and SiO_2. Figure reproduced according to data from [50, 51].

1-dimensional vertical scan

For the structure with a dimension comparable to the beam spot, in order to obtain a homogeneous dose in the SiO_2, the irradiation needs to be done by scanning the beam along the vertical direction. Assuming the irradiation set-up moves vertically with a constant speed v_y, the dose in the insulator can be calculated by:

$$Dose = \frac{3.6\text{eV} \cdot R}{q_0 \rho_{Si} d_{Si} \Delta x \cdot v_y} \iint_{\Delta x, \Delta Y} J_{diode}(x, y) \cdot \mathrm{d}x\mathrm{d}y \tag{7.3}$$

with ΔY the full range of the vertical beam profile.

2-dimensional scan

Larger area sensors, e.g. microstrip sensors with an area of $\sim$ 1 cm^2 larger than the area of the beam spot, need to be irradiated by scanning in both horizontal and vertical directions. The procedure is to move the irradiation set-up horizontally with a constant speed v_x to scan the beam, then to change the vertical position with a small step y_{step} and repeat the scan. By repeating the procedure until the entire sample is scanned, the larger area sensors can be irradiated uniformly. The dose is determined according to

$$Dose = \frac{3.6\text{eV} \cdot R}{q_0 \rho_{Si} d_{Si} y_{step} v_x} \iint_{\Delta X, \Delta Y} J_{diode}(x, y) \cdot \mathrm{d}x\mathrm{d}y \tag{7.4}$$

where ΔX is the full range of the horizontal beam profile.

As a short summary, for the studies of surface-radiation damage, the MOS capacitors with a diameter of 1.5 mm and the gate-controlled diodes produced by CiS,

Hamamatsu and Canberra were irradiated by scanning the beam in vertical direction. The "large" area MOS capacitor (3.5 mm $\times$ 1 mm) and gate-controlled diode produced by Sintef, and the microstrip sensors ($\sim$ 1 cm^2) were irradiated by scanning the beam along both the horizontal and vertical directions.

The results from the measurement of the dose agree within 20% with the calculations using the current of the DORIS III beam, the field of the bending magnet and the geometry of the set-up. All references to dose in the text refer to the surface dose in SiO_2. The dose enhancement effect in SiO_2 has not been taken into account in this study [52].

8. Methods to extract N_{ox}, N_{it} and J_{surf}

The methods to extract the oxide-charge density, N_{ox}, the interface-trap density, N_{it}, and the surface-current density, J_{surf}, have been studied extensively for the non-irradiated and low-dose irradiated test structures (dose less than 500 kGy) by different groups [15, 24, 53–55]. In this chapter, the methods used in the current work to extract N_{ox}, N_{it} and J_{surf}, especially for highly irradiated test structures, will be introduced and the limitation of the methods discussed.

8.1. Extraction of N_{it} and N_{ox}

The capacitance/conductance-voltage (C/G-V) and thermal dielectric relaxation current (TDRC) measurements have been performed on the MOS capacitors, in order to extract the oxide-charge density, N_{ox}, the distribution of interface-states density in the silicon band gap, $D_{it}(E_{it})$, and the interface-trap density, N_{it}. For the measurements, the voltage is applied to the gate of the MOS capacitor while the backside is grounded. The measurement scheme is shown in figure 8.1.

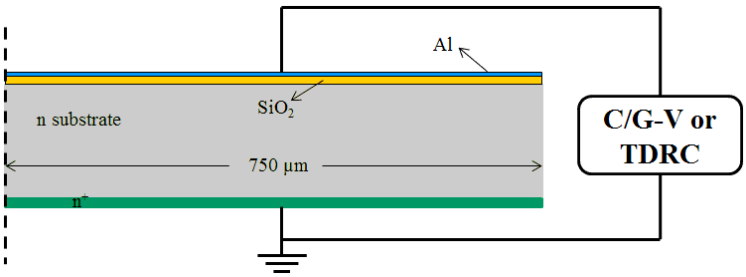

Figure 8.1: Cross section and measurement scheme of a MOS capacitor.

When performing the C/G-V measurements it has been observed that, for irradiated MOS capacitors biased in strong inversion, holes are injected into border traps in the SiO_2 close to the Si-SiO_2 interface [15, 56]. They cause further shifts of the C/G-V curves. The effect is illustrated by the C-V curves shown in figure 8.2(a) for a MOS capacitor irradiated to 5 MGy and annealed at 80 °C for 30 minutes. The gate voltage is cycled four times from 0 V to the maximum voltage V_{max} and back to 0 V, with V_{max} values of -40, -60, -80 and -80 V. The shapes of the four curves (and their frequency dependences, not shown) are identical, but the voltages at which the flatband capacitance is reached change. They are -36, -36, -40 and -44 V, which is an evidence for additional positive charges in the SiO_2. Hence, for all C/G-V measurements in the following studies, the voltage scans are stopped before the strong inversion is reached, to avoid the injection of holes into border traps.

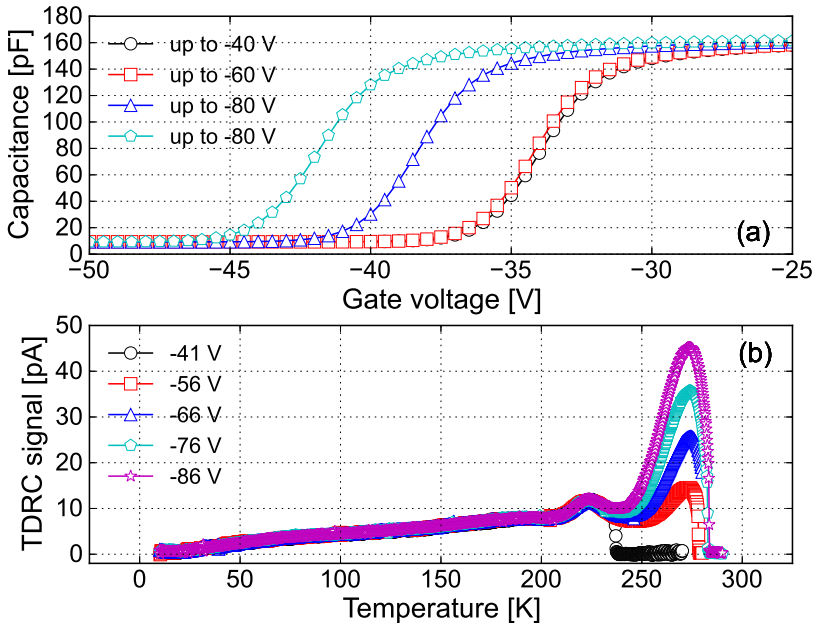

Figure 8.2: (a) C-V curves for 1 kHz of the MOS capacitor irradiated to 5 MGy after annealing at 80 °C for 30 minutes biased from 0 V to different maximum voltages: The shift of the C-V curves indicates the injection of holes into SiO_2. (b) The corresponding TDRC spectra: The increase of the TDRC signal at $\sim$ 270 K is due to the generation current in the silicon bulk. In the legend, the voltages applied to the gate of the MOS capacitor during heating up are shown.

The measured TDRC signal, I_{tdrc}, as function of temperature, T, allows to determine the distribution of the interface-states density, $D_{it}(E_{it})$, in the silicon band gap [27,29–32,57]. The measurement procedures have been introduced in chapter 5. Figure 8.2(b) shows the TDRC spectra for the same fore-mentioned MOS capacitor with different gate voltages applied during heating up in a temperature range between 10 K and 290 K. The TDRC signal around 270 K increases with higher negative gate voltages. The peaks close to room temperature are due to the generation current of defects in the depleted silicon bulk [27, 30, 58], and the values of the peaks depend on the gate voltage. The TDRC signal due to the generation current of bulk defects overlaps the signal produced by the emission of majority carriers stored in interface traps, thus the gate voltage should be limited in order to avoid the overlap. According to extensive measurements, it is found that if the gate voltage applied during heating up of the TDRC measurement equals to the voltage V_{merge}, at which the capacitance measured with frequencies of 1 kHz and 10 kHz merge in inversion, the generation current due to the defects in silicon bulk whose peak is located at $\sim$ 270 K in the TDRC spectra disappears. Therefore, the TDRC measurements for irradiated MOS capacitors were measured with gate voltages of 0 V (accumulation) for filling during cooling down and with V_{merge} during heating up.

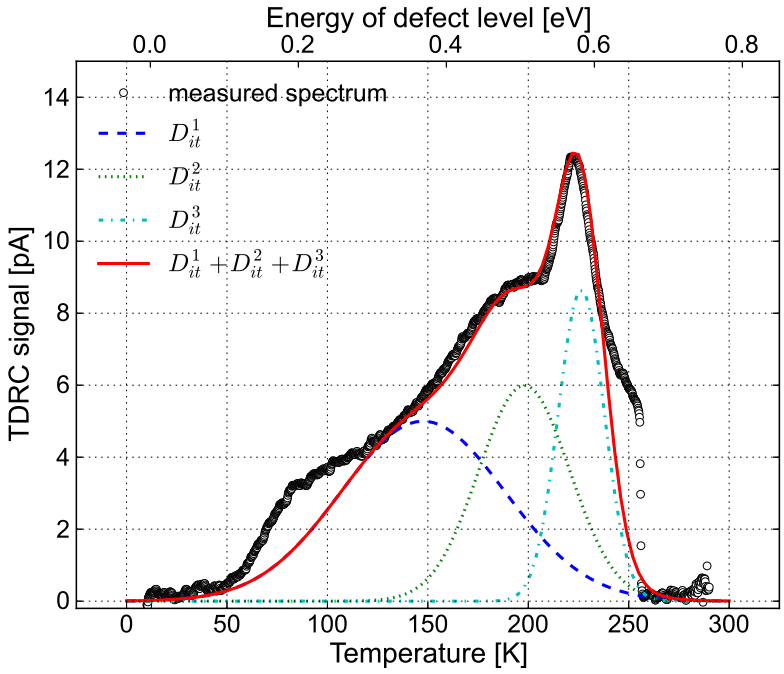

Figure 8.3: TDRC spectrum of a MOS capacitor fabricated on <100> silicon irradiated to 5 MGy after annealing at 80 °C for 10 minutes.

Figure 8.3 shows the TDRC signal for a MOS capacitor irradiated to 5 MGy and annealed for 10 minutes at 80 °C. For quantitative analysis, the following assumptions are made:

- The TDRC signal is caused only by the emission of majority carriers (electrons for n-doped silicon) stored in interface traps.
- The TDRC signal is described by three dominant interface traps with Gaussian energy distribution in the silicon band gap.
- The three dominant interface traps contributing to the measured TDRC signal are acceptors in the upper part of the silicon band gap.

The first assumption is made as the TDRC signal around 225 K cannot be simply distinguished whether it is due to the emission- or the generation-current of the interface trap. Typically, the integrated interface-trap density responsible for the TDRC signal that appears around 225 K under this assumption (caused by the emission current) is $\sim$ 50% larger than the value obtained under the assumption that the TDRC signal is caused by the generation current. The second one is based on an annealing study on an <111> MOS capacitor, which will be discussed later in detail in this chapter. The third is made as the TDRC technique is not able to give the information on the type of an interface trap. However, the assumptions made above gives the maximal estimate for the oxide-charge density.

Using equations (5.5) and (5.6) the $D_{it}(E_{it})$ spectrum is extracted. As seen in figure 8.3, its main features can be described by three states with Gaussian energy distribu-

tions D_{it}^1, D_{it}^2 and D_{it}^3 as given in table 8.1. There is also a peak around 100 K which, however, as acceptor close to the conduction band, has no influence at room temperature. It should be noted here that the fit to the TDRC spectrum does not allow an unambiguous determination of the energies and widths of the different trap levels. However, deconvolution of several TDRC spectra measured after different annealing times and/or different irradiation doses allow to fix the number and the trapping parameters of the interface states to the values given in table 8.1. In addition, the spectra at low temperatures change in a way which cannot be described with a single level and its strength is different for MOS capacitors fabricated by different vendors. Thus this analysis should not be considered as an unambiguous determination of the radiation-induced interface traps but as a consistent phenomenological description of the measurements.

	D_{it}^1	D_{it}^2	D_{it}^3
Capture cross section σ [cm^2]	1.2×10^{-15}	5.0×10^{-17}	1.0×10^{-15}
Peak energy [eV]	0.39	0.48	0.60
FWHM [eV]	0.26	0.13	0.071

Table 8.1: The properties of the three dominant interface-trap levels. The peak energy of D_{it}^3 is 0.60 eV under the assumption that the TDRC signal at 225 K is caused by the emission current; however, if assuming the TDRC signal is caused by the generation current of interface traps, its peak energy is 0.69 eV.

For the calculation of the energy distribution and of the densities of interface traps the frequency factors in equations (5.5) and (5.6) have to be known for each state. In principle, they can be determined from the TDRC spectra measured with different heating rates (i.e. β_1 and β_2) following the procedure described by Uranwala *et al.* [30]. The frequency factor for each of the trapping centres is estimated by

$$v = 10^y, \text{ with } y = \frac{T_2 \log\beta_2 - T_1 \log\beta_1}{T_2 - T_1} \tag{8.1}$$

where T_1 and T_2 are the TDRC peak temperatures for the heating rates β_1 and β_2.

This method is only reliable if the trap levels do not overlap. However, they do, as seen in figure 8.3. In the annealing study of MOS capacitors fabricated on <111> silicon it has been observed that after annealing for 32 hours at 80 °C the signal from D_{it}^2 is significantly reduced and the signals from D_{it}^1 and D_{it}^3 are separated (figure 8.4). Thus the frequency factors for these two interface states could be determined [using equation (8.1)] by performing TDRC measurements with different heating rates β (between 0.1 K/s and 0.5 K/s). The estimated ranges for the frequency factors are $10^{11.6} - 10^{12}$ s^{-1} and $10^{11.5} - 10^{12.5}$ s^{-1} for D_{it}^1 and D_{it}^3, respectively. These frequency factors in turn are used to calculate the capture cross sections for the majority carriers at different temperatures according to $\sigma = v/(N_c v_{th})$. The values for 295 K, where the C/G-V curves have been measured, are given in table 8.1. In the estimation the frequency shifts of the C/G-V curves have been taken into account. With these values the capture cross section of D_{it}^2 has been obtained by comparing the calculated C/G-

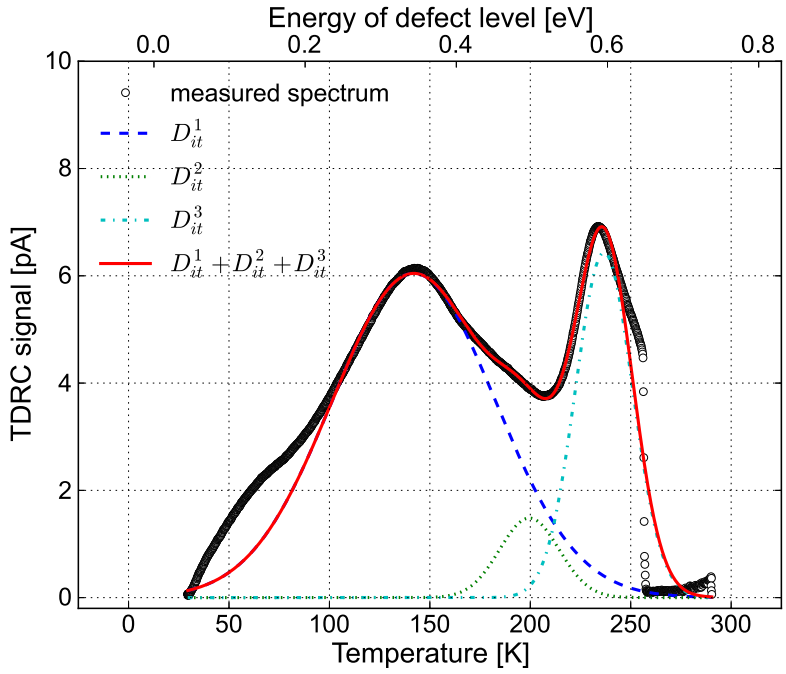

Figure 8.4: TDRC spectrum of a MOS capacitor fabricated on <111> silicon irradiated to 4.8 MGy after annealing at 80 °C for 32 hours. The signal owing to the D_{it}^2 state is significantly reduced due to fast annealing.

V curves based on the model described in chapter 6 with the measured ones for the investigated samples after annealing for 10 minutes at 80 °C. Table 8.1 summarizes the values estimated for the cross sections, the peak activation energies and the full widths at half-maximum (FWHM). When performing the annealing studies on the <100> crystals it has been noticed that after annealing for 72 hours at 80 °C a strong D_{it}^2 signal remains. Thus the method for determining the cross sections described above cannot be used here and for that reason the <111> values have been used in the analysis.

Once the distributions of interface-states density $D_{it}^{1,2,3}$ were known, the integrated interface-trap densities can be obtained by

$$N_{it}^{1,2,3} = \int_{E_v}^{E_c} D_{it}^{1,2,3}(E_{it}) \mathrm{d}E_{it} \tag{8.2}$$

Hence, the density of overall interface traps, which contributes to the TDRC signal, is obtained by $N_{it} = \Sigma N_{it}^{1,2,3}$. The value obtained equals to the one calculated by equation (5.9) directly from the integration of the TDRC signal $I_{tdrc}(T)$. It should be stressed that the calculated density of interface traps does not include those trap levels located in the lower part of the silicon band gap.

To extract the oxide-charge density N_{ox}, the model describing the irradiated MOS capacitor by an RC-network introduced in chapter 6 is employed. The model allows to calculate the capacitance and conductance of a MOS capacitor as function of gate

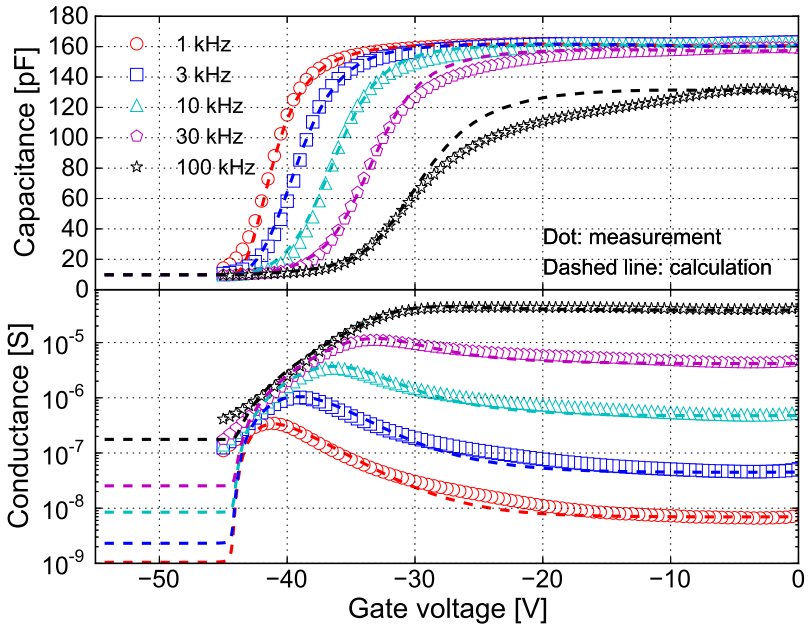

Figure 8.5: The C/G-V curves of a MOS capacitor irradiated to 10 MGy after annealing at 80 °C for 10 minutes and comparison to the calculated ones for frequencies between 1 kHz and 100 kHz using the model described in chapter 6.

voltage for different frequencies using the measured TDRC signal, the capture cross section of each single trap and N_{ox} as input. As the TDRC signal can be obtained from measurements and the capture cross section of each single trap has been determined, the oxide-charge density N_{ox}, which just shifts the C/G-V curves along the voltage-axis, is obtained by adjusting its value till the calculated C/G-V curves describe the measurements. Figure 8.5 shows the comparison of the measured to the calculated C/G-V curves (in parallel mode) of a MOS capacitor irradiated to 5 MGy after annealing for 10 minutes at 80 °C for frequencies between 1 kHz and 100 kHz. In the model calculation, the assumption is made that all the interface traps observed in the TDRC measurements are acceptors, which gives the maximal estimate for the density of oxide charges introduced by X-rays.

8.2. Extraction of J_{surf}

To determine the surface-current density, J_{surf}, current-voltage (I-V) measurements have been done at room temperature for the gate-controlled diode (GCD). Figure 8.6 shows the I-V measurement scheme for a gate-controlled diode consisting of a central diode and 5 surrounding gate rings. Such kind of gate-controlled diode is used for the studies regarding the dependence of irradiation dose, gate voltage and annealing time and temperature of the surface-current density. However, for the studies of dose dependence of J_{surf}, some other kinds of GCD fabricated by different vendors are

used, however the measurement schemes are similar.

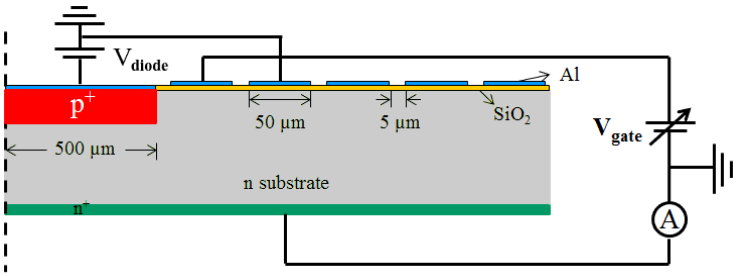

Figure 8.6: Cross section and measurement scheme of a gate-controlled diode consisting of a central diode and 5 gate rings.

For the I-V measurement performed on the gate-controlled diode, a constant DC voltage (-6 V for non-irradiated GCD; -12 V for irradiated GCD) is applied to the p^+ electrode through a voltage source to partially deplete the central diode, and the current flow from the rear side n^+ electrode is recorded as function of voltage on the 1^{st} gate ring while keeping the 2^{nd} gate ring grounded. The DC voltage applied to the p^+ electrode should be sufficient so that the depletion regions below the diode and the 1^{st} gate merge when the 1^{st} gate is biased to depletion. To determine the voltage applied to the diode V_{diode}, a set of I-V measurements with different V_{diode} has been done: It is found that the surface currents saturate at voltages of -6 V for non-irradiated GCD and -12 V for irradiated GCD (not shown), respectively.

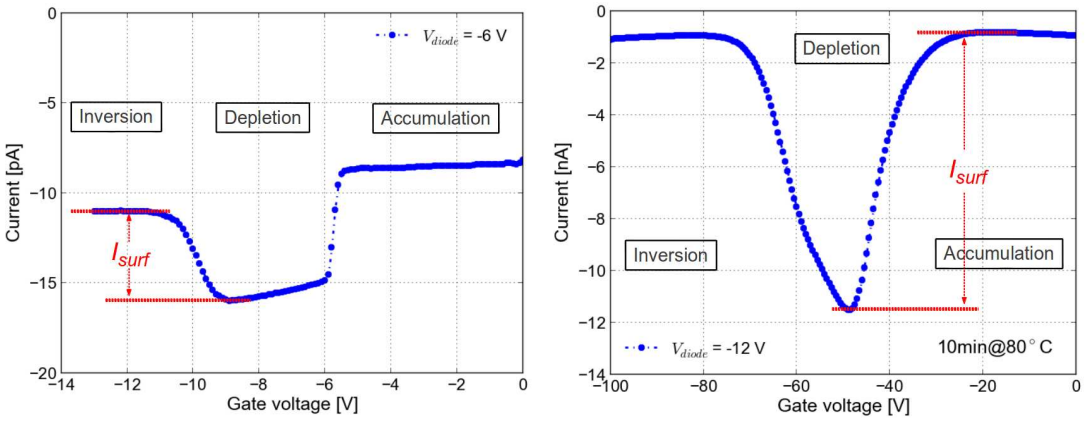

Figure 8.7: Left: Extraction of the surface current I_{surf} from the non-irradiated gate-controlled diode. Right: Extraction of the surface current I_{surf} from the irradiated gate-controlled diode. The result from a gate-controlled diode irradiated to 5 MGy after 10 minutes annealing at 80 °C is shown. The current measured in accumulation for the irradiated gate-controlled diode is higher than the value before irradiation, which is due to the surface current caused by the interface traps located at the depleted Si-SiO_2 interface close to the p^+ implant.

Figure 8.7 shows the I-V curves of gate-controlled diodes before and after irradiation to 5 MGy. For the non-irradiated GCD, the surface current, I_{surf}, is extracted

from the "maximum" current measured in depletion of the 1^{st} gate ring and the average value of the currents obtained in inversion. For the irradiated GCD, I_{surf} is extracted from the "maximum" current and the average currents in accumulation. In principle, for irradiated GCD, the surface current is sufficiently high compared to the bulk-generation current, thus the average currents in accumulation and in inversion are not expected to be very different. However, for highly irradiated GCD, an electron-accumulation layer is formed below the Si-SiO_2 interface in-between the p^+ electrode and the 1^{st} gate, whose width decreases with gate voltage. Hence, a gate-voltage dependence of the current in inversion can be observed. To avoid an incorrect extraction of the average current, the mean value of the currents in accumulation is used for irradiated GCD.

It can be seen that the shape of the I-V curve for an irradiated GCD is different from the ideal shape for the non-irradiated one. For an ideal I-V curve, the surface currents are expected to be identical for different gate voltages biasing the region below the gate to depletion. However, for the irradiated GCD, the surface currents change dramatically with gate voltage and decrease when a maximum is reached. The reduction of the surface currents at "higher" gate voltages (in depletion) is due to the decrease of the critical channel length below the gate with gate voltage. At "higher" gate voltages, part of the Si-SiO_2 interface below the gate is in depletion, whereas part of the interface is already in inversion. The length of the depleted interface is characterized by the critical channel length. Only interface traps in this region are able to contribute to the surface current. Pierret [59,60] has shown that the extraction of the surface current I_{surf} and subsequently the surface-generation velocity S_0 from a depleted interface is only correct if the length of the gate L_{gate} is shorter than the critical length L_{cri}, otherwise the extracted I_{surf} and S_0 are reduced from their actual values and decrease as L_{cri} decreases. The critical length L_{cri} is a function of the depth of the depletion layer below the gate, W_d, and the surface-generation velocity, S_0:

$$L_{cri} = \left[\frac{\overline{\mu}_p (k_B T/q_0)^2 \varepsilon_0 \varepsilon_{si}}{q_0 N_d S_0 W_d \sqrt{\sigma_p/\sigma_n}} \right]^{1/2} \tag{8.3}$$

with $\overline{\mu}_p$ the effective mobility of minority carriers below the Si-SiO_2 interface, N_d the doping concentration of the silicon substrate and σ_p/σ_n the ratio of hole-to-electron capture cross section of interface states at the silicon midgap. The depth of the depletion layer below the gate W_d depends on the band bending ψ_s,

$$W_d = \sqrt{\frac{2\varepsilon_0 \varepsilon_{si} |\psi_s|}{q_0 N_d}} \tag{8.4}$$

Figure 8.8 shows the critical length L_{cri} as function of the depth of the depletion layer below the gate for surface-generation velocities S_0 of 1.0, 10.0, 100.0 and 1000.0 cm/s and a doping concentration of 1.0×10^{12} cm^{-3} typical for high-resistivity silicon material. The dashed yellow line in the figure indicates the length of a gate of 50 μm. It can be seen, for the non-irradiated and low-dose irradiated GCD with smaller surface-generation velocities, the critical length L_{cri} is always larger than the

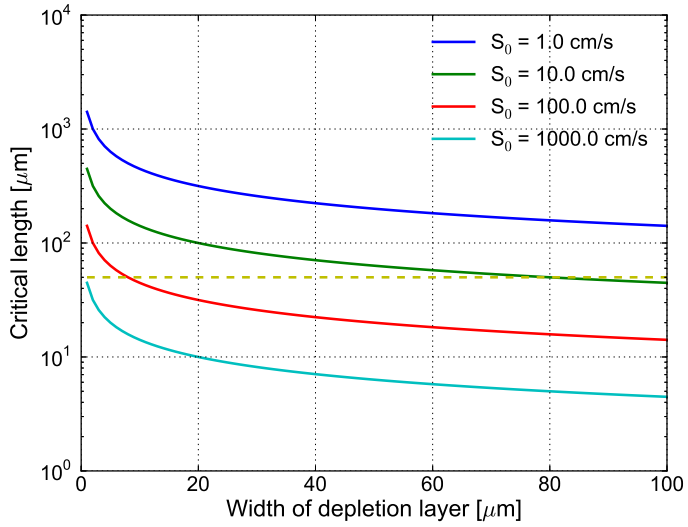

Figure 8.8: The critical length L_{cri} as function of the width of depletion layer below the gate for different surface-generation velocities S_0. The doping concentration is assumed to be 1.0×10^{12} cm^{-3}, and $\sigma_p/\sigma_n = 1$.

actual length of the gate L_{gate}. However, for the irradiated GCD with large surface-generation velocities, L_{cri} is smaller than L_{gate} and L_{cri} decreases with the depth of the depletion layer. Thus, the measured current decreases with gate voltage once it reaches the maximum in depletion. According to the procedure proposed by Pierret [59, 60] and Dugas [61], a calculation shows that the extracted surface-generation velocities (and surface-current densities) using this method for a gate length of 50 μm are reduced by $\sim$ 10%, $\sim$ 50% and $\sim$ 70% for $S_0 = 10^2$, 10^3 and 10^4 cm/s, assuming a doping concentration of 1.0×10^{12} cm^{-3}, $\sigma_p/\sigma_n = 1$ and a band bending of $-\phi_B$.

It should be noted that the measured surface current $I_{surf}(T_{meas})$ is very sensitive to the temperature T_{meas} during the measurement, i.e. at room temperature its value changes by $\sim$ 8% if the temperature changes by 1 °C. In figure 8.9(left), the temperature dependence of the I-V curves of an irradiated gate-controlled diode measured at different temperatures from 213 K to 295 K is shown. The following scaling formula, which is derived from the temperature dependence of Shockley-Read-Hall statistics, allows to describe the data

$$I_{surf}(T) = I_{surf}(T_{meas}) \cdot \left(\frac{T}{T_{meas}}\right)^2 \cdot \exp\left[\frac{0.605\text{eV}}{k_B} \cdot \left(\frac{1}{T_{meas}} - \frac{1}{T}\right)\right] \tag{8.5}$$

Figure 8.9 shows the I-V curves of a gate-controlled diode in the temperature range from 213 K to 295 K and the comparison between the measured surface currents and the calculated ones according to the scaling formula (8.5), which shows a good agreement. Thus, all surface currents extracted from the measurements in this study have been scaled to the values at 20 °C. The surface-current density at 20 °C, $J_{surf}(T = 293\text{ K})$, is calculated from the surface current scaled to 20 °C and the area of the 1^{st}

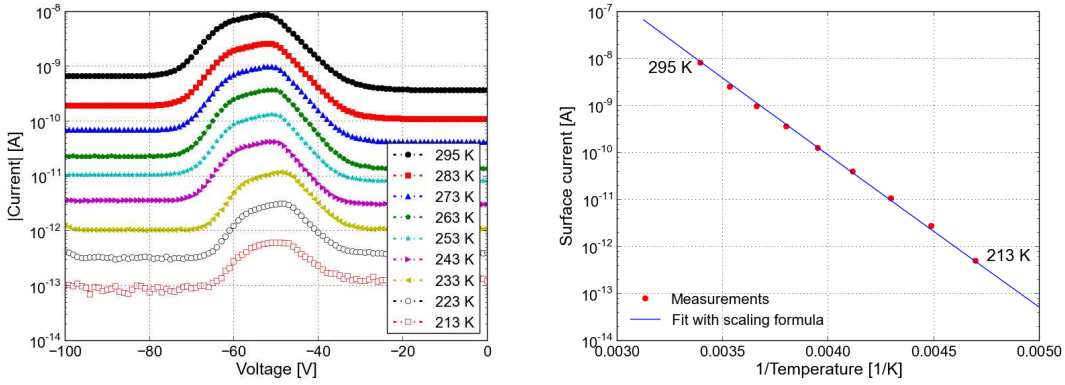

Figure 8.9: Left: I-V curves of a gate-controlled diode irradiated to $\sim$ 100 kGy after annealing at 80 °C for 60 minutes, measured in the temperature range from 213 K to 295 K. Right: Comparison of the measured values of surface currents at different temperatures with the scaling formula (8.5).

gate ring:

$$J_{surf}(T = 293\ \mathrm{K}) = I_{surf}(T = 293\ \mathrm{K})/A_{gate}^{1st} \tag{8.6}$$

8.3. Summary and discussion

In this chapter, the methods to extract the oxide-charge density, N_{ox}, the interface-trap density, N_{it}, and the surface-current density, J_{surf}, have been introduced. In addition, the parameters of the three dominant interface traps have been determined, which are the main inputs in the model calculation.

However, the extraction of separated traps at the Si-SiO_2 interface using the TDRC spectra needs certain assumptions. Assumptions have to be made on the cause of the current (emission/generation) contributing to the TDRC signal, on the type of the interface trap and on the way how to separate individual traps. It should be noted that the extraction of the oxide-charge density, N_{ox}, and interface-trap density, N_{it}, are obtained under these assumptions, which give maximal estimate for N_{ox}. A donor trap at the Si-SiO_2 interface located in the lower part of the silicon band gap is well known [15]. The trap is supposed not to significantly influence the C/G-V curves and the extracted N_{ox}, because the trap is not able to be filled with holes (not charged) in the voltage range of the C/G-V measurement. However, the influence depends on how much the energy distribution of the trap level extends to the midgap of silicon.

In addition, the extraction of the surface current is introduced and the shape of the I-V curve of an irradiated gate-controlled diode explained. However, for irradiated GCD, part of the Si-SiO_2 interface will be weakly inverted even if the gate voltages are far below the voltage required to strongly invert the region below the interface. Thus, the surface-current density and the surface-generation velocity deduced from the method used for GCD are less than the real values.

9. Dose dependence of N_{ox}, N_{it} and J_{surf}

Imaging experiments at the European X-ray Free Electron Laser require silicon pixel sensors which can withstand X-ray doses up to 1 GGy. To address this challenge, the properties of the SiO_2 layer and of the Si-SiO_2 interface, using MOS capacitors and gate-controlled diodes manufactured on high-resistivity n-type silicon irradiated to X-ray doses between 1 kGy and 1 GGy, have been studied in this chapter. Using capacitance/conductance-voltage (C/G-V), current-voltage (I-V) and thermal dielectric relaxation current (TDRC) measurements, together with the model described in chapter 6, the oxide-charge density (N_{ox}), the surface-current density (J_{surf}) and the integrated interface-trap density (N_{it}) have been determined as function of dose. The results indicate that the dose dependence of N_{ox}, J_{surf} and N_{it} depend on the producer of the sample and the crystal orientation at higher dose values.

9.1. Investigated structures and their electrical properties before irradiation

To study the total ionizing dose (TID) effects, test fields, each including a MOS capacitor and a gate-controlled diode, built on high resistivity n-type silicon with crystal orientations <100> and <111> produced by four vendors, CiS, Hamamatsu, Canberra and Sintef, have been investigated. The test fields used in this study and their properties are given in table 9.1. The geometries and gate areas are different for different producers: For CiS and Hamamatsu, the MOS capacitor has a circular shape with a diameter of 1.5 mm, and the gate-controlled diode consists of a circular diode with a diameter of 1.0 mm and 5 concentric gate rings surrounding the central diode. The width of the gate rings is 50 μm and neighbouring gate rings are separated by 5 μm. For Canberra, the geometry and dimensions of the MOS capacitor are the same as for CiS and Hamamatsu, whereas the geometry of the gate-controlled diode is a finger-like structure with 6 vertical and 1 horizontal fingers of gates embedded by a diode. The width of the 7 fingers in total is 100 μm and the lengths for the 6 vertical and 1 horizontal figures are 1000 and 1100 μm. For Sintef, the MOS capacitor is rectangular and the lengths along two edges are 3.5 and 1.0 mm. The gate-controlled diode of Sintef consists of a circular diode in the centre, whose diameter is 400 μm, and 1 concentric gate ring of a gate length of 210 μm. Figure 9.1(a)-(c) shows the top view of the investigated gate-controlled diodes produced by different vendors.

The oxide-charge density N_{ox}, the interface-trap density N_{it} and the surface-current density J_{surf} given in table 9.1 are obtained directly from the C/G-V, TDRC and I-V measurements. The measurements on a test field (labeled CE2250) produced by CiS with an orientation <100> is shown in figure 9.2; the others are given in appendix (A.1, A.2, A.3, A.4, A.5, A.6).

Label	CE2250	CB0450
Producer	CiS	CiS
Material	FZ	DOFZ
Orientation	<100>	<111>
Doping	7.6×10^{11} cm^{-3}	1.1×10^{12} cm^{-3}
Insulator	330 nm SiO_2 + 50 nm Si_3N_4	360 nm SiO_2 + 50 nm Si_3N_4
N_{ox}	1.2×10^{11} cm^{-2}	5.7×10^{11} cm^{-2}
N_{it}	1.6×10^{11} cm^{-2}	8.0×10^{11} cm^{-2}
J_{surf}	0.78 nA/cm^2	3.0 nA/cm^2
Label	6336-01-03	HAMA-04
Producer	CiS	Hamamatsu
Material	Epi	FZ
Orientation	<111>	<100>
Doping	7.8×10^{13} cm^{-3}	9.0×10^{11} cm^{-3}
Insulator	335 nm SiO_2	700 nm SiO_2
N_{ox}	6.3×10^{11} cm^{-2}	1.3×10^{11} cm^{-2}
N_{it}	8.8×10^{11} cm^{-2}	3.0×10^{10} cm^{-2}
J_{surf}	0.81 nA/cm^2	8.1 nA/cm^2
Label	Canberra-145/7	Sintef-1/2/3
Producer	Canberra	Sintef
Material	FZ	FZ
Orientation	<111>	<100>
Doping	6.2×10^{11} cm^{-3}	3.0×10^{11} cm^{-3}
Insulator	250 nm SiO_2	750 nm SiO_2
N_{ox}	2.2×10^{11} cm^{-2}	2.8×10^{10} cm^{-2}
N_{it}	1.4×10^{11} cm^{-2}	3.8×10^{10} cm^{-2}
J_{surf}	46 nA/cm^2	8.7 nA/cm^2

Table 9.1: List of investigated test fields in the study of dose dependence before irradiation. Each contains a MOS capacitor and a gate-controlled diode. FZ - float zone; DOFZ - diffusion oxygenated float zone; Epi - epitaxial silicon. J_{surf} has been scaled to a value at 20 °C.

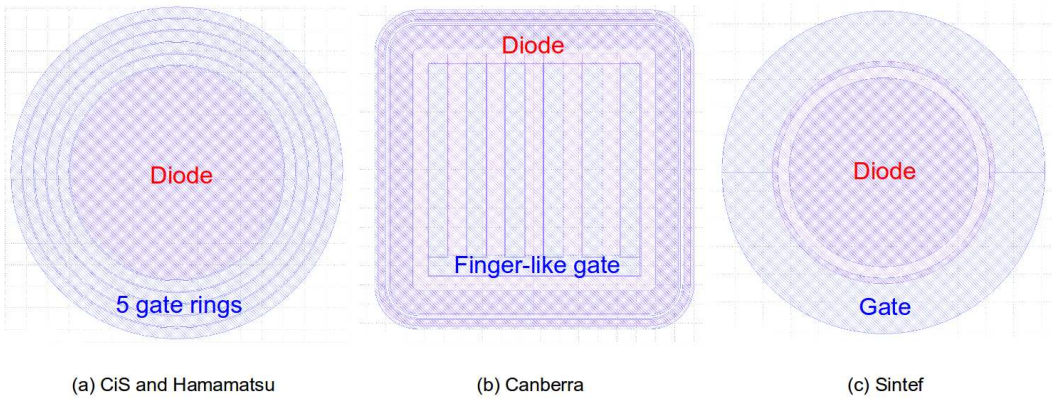

Figure 9.1: The top view of the investigated gate-controlled diodes: (a) CiS and Hamamatsu; (b) Canberra; (c) Sintef.

As expected, it is observed that N_{ox} and N_{it} of <100> silicon are lower than that of <111>: The maximal N_{ox} and N_{it} for <100> orientation are 1.3×10^{11} cm^{-2} from HAMA-04 and 1.6×10^{11} cm^{-2} from CE2250 respectively, however the minimal ones for <111> orientation are at least 2.2×10^{11} cm^{-2} and 1.4×10^{11} cm^{-2} from Canberra-145/7. The lower values of N_{ox} and N_{it} of <100> silicon is due to the good passivation of dangling silicon bonds at the Si-SiO_2 interface compared to <111>.

The minimal J_{surf} is as low as 0.78 nA/cm^2 from CE2250 (<100>), however the maximal one is as high as 46 nA/cm^2 from Canberra-145/7 (<111>). The values of J_{surf} before irradiation are different by a factor of $\sim$ 60, however the differences are smaller after irradiation.

9.2. Measurements after irradiation

The test fields were irradiated with 12 keV X-rays at the DESY DORIS III beamline F4 to doses of from 1 kGy to 1 GGy using the irradiation set-up discussed in chapter 7. The following procedures were used in this study:

- The test fields, each consisting of a MOS capacitor and a gate-controlled diode, were irradiated to a specific dose (the first irradiation doses are different for the different vendors: CiS and Hamamatsu start from 10 kGy, Canberra from 2.2 kGy and Sintef from 1 kGy).
- After irradiation, solid-state measurements, C/G-V, I-V and TDRC, were performed on MOS capacitors and gate-controlled diodes before and after annealing at 80 °C for 10 minutes.
- The previously irradiated test fields were irradiated to higher doses and measured afterwards.
- The above steps were repeated till reaching the last expected doses. The last irradiation doses are 1 GGy for test fields of CiS and Hamamatsu, and 100 MGy for test fields of Canberra and Sintef.

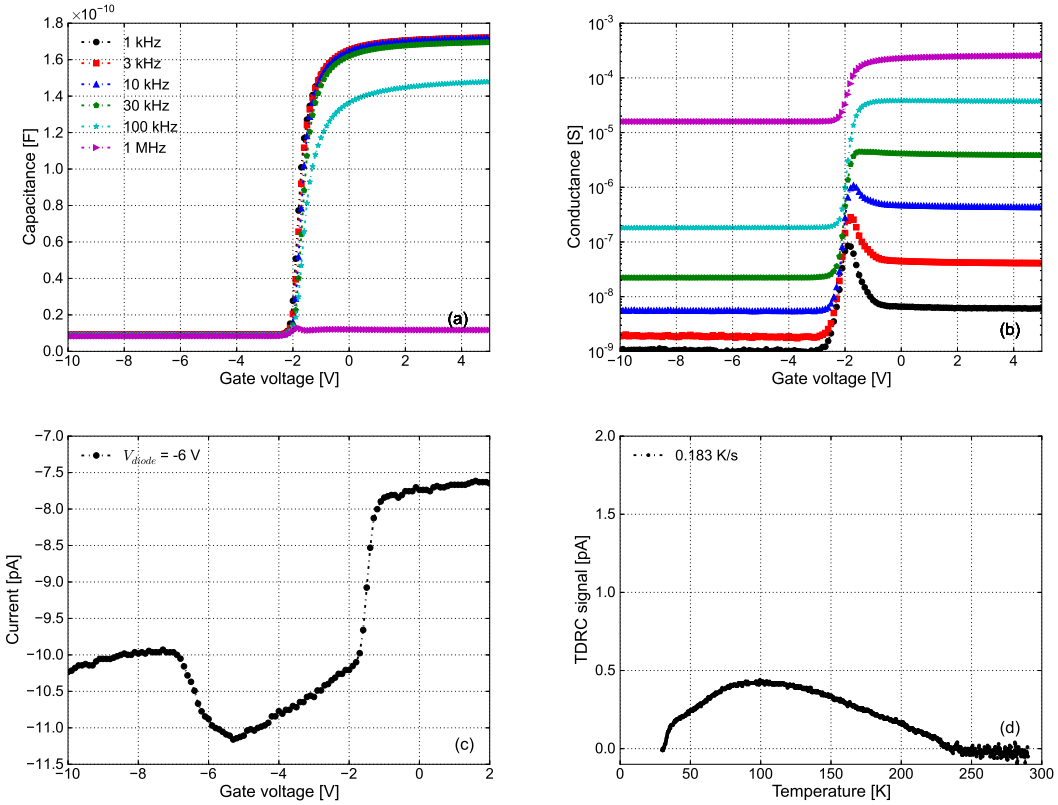

Figure 9.2: Measurements on the non-irradiated CE2250 fabricated by CiS: (a) C-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of gate-controlled diode for V_{diode} = -6 V scaled to 20 °C. (d) TDRC spectrum of MOS capacitor.

The C/G-V measurements on MOS capacitors were performed from 0 V down to a gate voltage (V_{merge}) at which the capacitance of 1 kHz and 10 kHz merge in inversion. The gate voltages of I-V measurements on gate-controlled diodes were scanned from 0 V to voltages which are at least 20 V "lager" than the gate voltages corresponding to the strong inversion condition. The TDRC measurements on MOS capacitors were performed with a gate voltage of 0 V applied during cooling down and with the gate voltage V_{merge} during heating up. During heating up the MOS capacitor, a constant heating rate $\beta = 0.183$ K was used.

Here only the C/G-V, I-V and TDRC curves from CE2250 are shown. The others can be referred to appendix A.7, A.9 and A.8. However, the results from all of them are discussed together.

9.2.1. C/G-V curves of MOS capacitors

In figure 9.3 (as well those in the appendix A.7), C/G-V curves of 1 kHz and 10 kHz are shown for different doses after annealing for 10 minutes at 80 °C. Results for

before annealing (0 minutes at 80 °C) not shown here however have similar features as for 10 minutes annealing. The features can be summarized as follow:

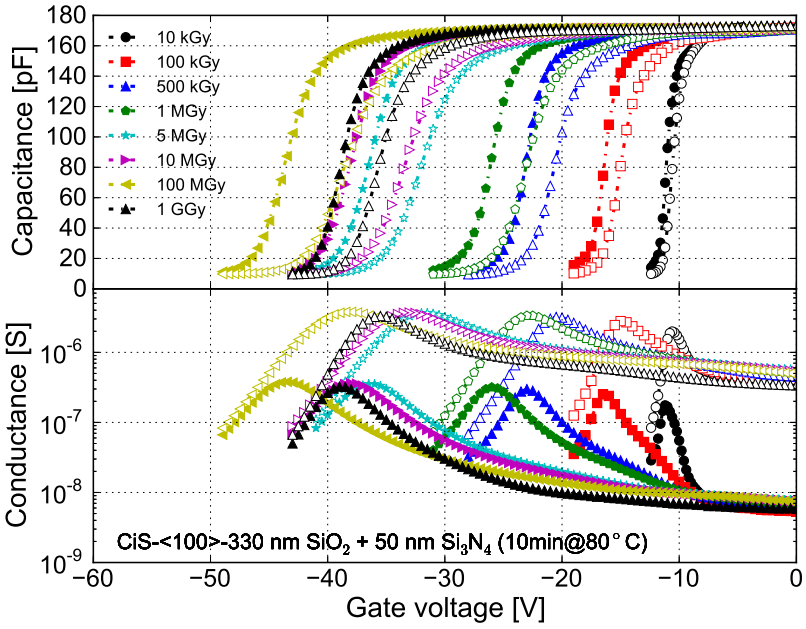

Figure 9.3: Measurements of C/G-V curves on irradiated MOS capacitors of CE2250 with orientation <100> produced by CiS. Frequencies of 1 kHz and 10 kHz are shown.

- Shift in gate voltage of C/G-V curves
- Frequency shift of C-V curves and change of the slope of the transition from accumulation to inversion
- Increase of the peak value of conductance

The shift in gate voltage of C/G-V curves can be explained by the increase of oxide charges introduced by irradiations and the effect of charged interface traps: The number of positive charges in the SiO_2 increases with accumulated dose in the oxide, which causes shifts of C/G-V curves to negative gate voltages. The shift in gate voltage of C/G-V curves caused by oxide charges is given by $\triangle V_{gate} = q_0 N_{ox}/C_{ox}$, with the oxide-charge density N_{ox} and the oxide capacitance C_{ox}. The shift in gate voltage reaches a "maximum" for a dose of 100 MGy and then decreases by $\sim$ 5 V for a dose of 1 GGy. In order to reduce the irradiation time, the dose rate during irradiation was increased to 180 kGy/s for 1 GGy, which is 10 times higher than the dose rates for the other irradiations. The increase of dose rate results in less oxide charges and interface traps (as discussed in chapter 3). According to the investigation of Perrey [26], the differences in voltage shift of C/G-V curves for different dose rates are within $\sim$ 30%.

The frequency shift of C-V curves is the result of an increase of interface traps. From figure 9.3, it is seen the frequency shift increases till 100 MGy and then decreases for 1 GGy, which indicates the interface-trap density reaches its maximum at 100 MGy.

The peak value of conductance in depletion is also a direct reflection of the density of interface traps. The peak value of conductance reaches the maximum at 100 MGy. However, using the conductance to judge the interface-trap density is not as obvious as using the frequency shift of C-V curves.

9.2.2. TDRC spectra of MOS capacitors

The TDRC spectra of the MOS capacitor (CE2250) after irradiations are shown in figure 9.4. The other TDRC curves are given in appendix A.8.

For 10 kGy, 100 kGy and 500 kGy, the TDRC signals around 245 K is dominated by the generation current of defects in the depleted silicon. For low-dose irradiated (and non-irradiated) MOS capacitors, the generation current of defects in depleted silicon is sensitive to the gate voltage during the TDRC measurement. A voltage slightly higher than V_{merge} causes large generation currents. However, for highly irradiated MOS capacitors, the generation current is hardly seen. This is due to the significant increase of TDRC signals at around 225 K, which corresponds to D_{it}^{3} indicated in figure 8.3. The D_{it}^{3} is located at $\sim$ 0.6 eV from the conduction band, which stretches out the $V_{gate} - \psi_s$ curve so that the V_{gate} is not sensitive to ψ_s. Hence, to observe the generation current for highly irradiated MOS capacitors much higher gate voltages are needed during the TDRC measurements. As the defects in silicon are not the topic of the study, this will not be discussed further.

From the TDRC measurements shown in figure 9.4, one can observe that:

- Increase of TDRC signal with irradiation
- Change of TDRC spectra at low temperatures
- Shift of the peak located around 225 K

The TDRC signal increases with dose up to 100 MGy and then decreases at 1 GGy. The the TDRC signal, caused by the emission current of interface traps, is proportional to the interface-states density. Hence, the densities of the three dominant interface traps, $D_{it}^{1,2,3}$, increases and reaches its maximum at 100 MGy. The decrease of the TDRC signal at 1 GGy can be understood as a process that the passivation of dangling silicon bonds (interface traps) is enhanced. Hence, the difference of reaction rates of the depassivation and passivation processes changes. The trend of the TDRC signal changes with irradiation confirms the observation of the frequency shift of C-V curves mentioned above.

In addition, the shape of the TDRC spectra changes with irradiation, especially for the TDRC signals below $\sim$ 100 K. The change of the TDRC spectra either with irradiation or with time has also been observed by the others [17, 62–66]. However, due to the energy level of the interface traps, which contribute to the TDRC signals at low temperature (< 100 K), is located close to the conduction band, the acceptor-like traps are hardly filled by electrons at the operating temperature of the sensors so that

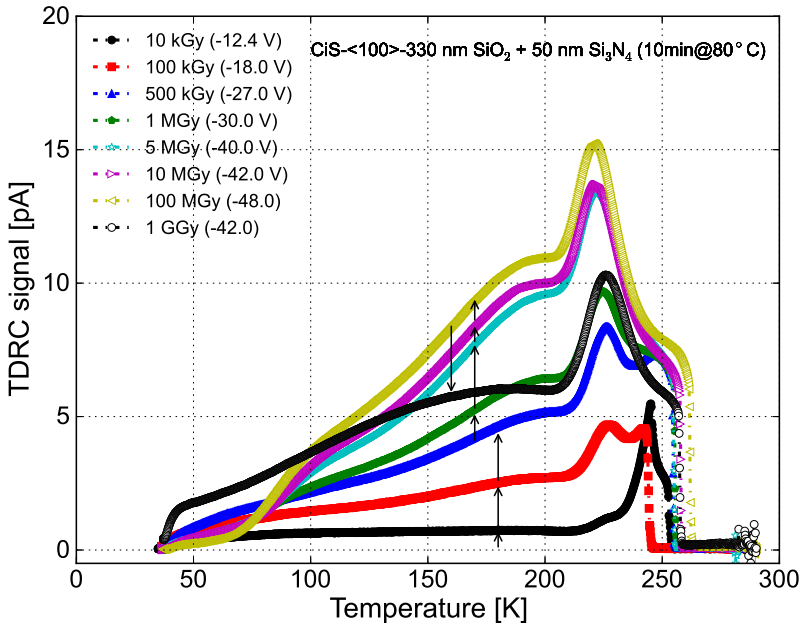

Figure 9.4: Measurements of TDRC spectra on the irradiated MOS capacitors of CE2250 with orientation <100> produced by CiS. The gate voltages used in the TDRC measurements during heating up are shown for each dose.

they do not influence the electrical properties. This is also the reason why it was not included in the fit as shown in figure 8.3.

Similar features are also found for the other test fields, whose results are shown in appendix A.8. It should be noticed that, with the same irradiation dose, the shapes of the TDRC spectra of MOS capacitors produced by different vendors are different, which indicates different dose dependence of $D_{it}^{1,2,3}$ for test fields from different vendors. However, all of them can be described by the three dominant traps described in chapter 8.

9.2.3. I-V curves of gate-controlled diodes

The I-V curves of the gate-controlled diode on CE2250 are shown in figure 9.5 (the others are given in appendix A.9). The currents have been scaled to their values at 20 °C using the scaling formula (8.5).

The shapes of the I-V curves change with irradiation: "Plateaus" can be observed in depletion for low irradiation dose (i.e. 10 kGy), which is similar to the ideal I-V curve of a non-irradiated gate-controlled diode. However, the "plateaus" disappear for higher irradiation doses. This has been explained in chapter 8: The critical length L_{cri} for higher surface-generation velocities is smaller than the gate length of the investigated gate-controlled diode. Hence, the surface current contributing to the I-V measurement depends on L_{cri}. L_{cri} is a function of the depth of the depletion layer below the gate W_d, which increases with the gate voltage (in depletion). Thus, a gate-voltage

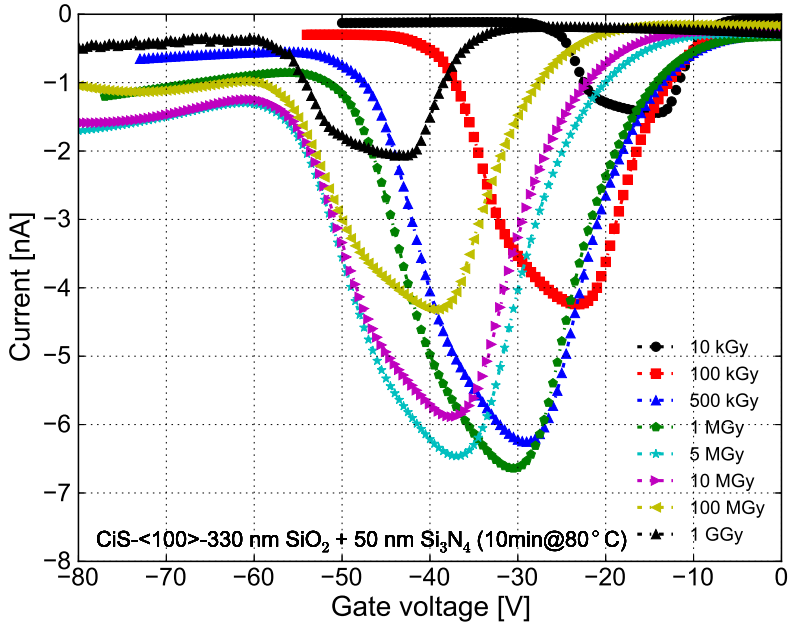

Figure 9.5: Measurements of I-V curves on irradiated gate-controlled diodes of CE2250 with orientation <100> produced by CiS. The bias voltage applied to the diode during the I-V measurements is -12 V. The currents have been scaled to their values at 20 °C.

dependence of the surface current for a highly irradiated gate-controlled diode biased to depletion is observed in this study.

The peak value of the measured current increases with irradiation dose till it reaches a maximum at 1 $\sim$ 5 MGy, then the peak value decreases. This results in a reduction of the extracted surface-generation current for doses above 5 MGy.

The current values measured in strong inversion ("high" gate voltages) are about 10%-20% of the peak values for higher irradiation doses. The currents in strong inversion are from the depleted interface outside the 1^{st} gate ring and the depleted interface in the 5 μm spacing between the p^+ implant and the 1^{st} gate ring.

9.3. Results: N_{ox}, N_{it} and J_{surf} vs. dose

According to the C/G-V, I-V and TDRC measurements, together with the model calculation, the oxide-charge density N_{ox}, the integrated density of interface traps N_{it} and the surface-current density J_{surf} from different test fields are determined as function dose. Figures 9.6, 9.7 and 9.8 show the results after annealing at 80 °C for 10 minutes. The results obtained before annealing are not shown here but given in appendix A.10.

In the figures 9.6 and 9.7, the data, labelled "CiS-<100>-350 nm SiO_2 + 50 nm Si_3N_4 (JSR)", which have been published in [46], are also shown for comparison.

First of all, a comparison of the measurements shown as yellow stars (YS: CiS-

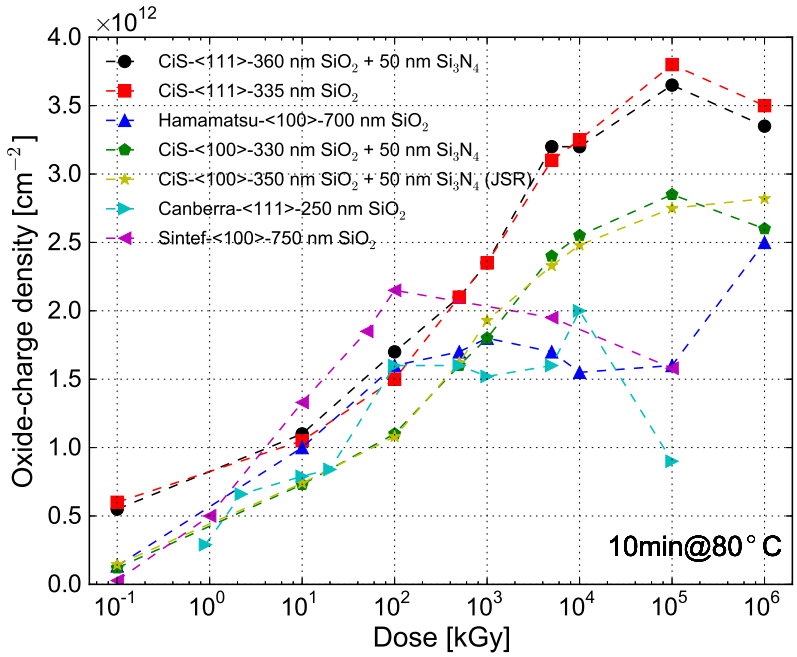

Figure 9.6: Dose dependence of N_{ox} after annealing at 80 °C for 10 minutes. Results of N_{ox} before irradiation are plotted at a dose of 10^{-1} kGy in the figure. Given the fact that the extraction of N_{ox} is based on the assumptions made in chapter 8, the results in the figure are maximal estimate for N_{ox}.

<100>-350 nm SiO_2 + 50 nm Si_3N_4 (JSR)) and as green dots (GD: CiS-<100>-330 nm SiO_2 + 50 nm Si_3N_4) demonstrates that the results for structures with the same technology and crystal orientation are compatible[1] and reproducible. The results for YS, measured in 2011 and published in [46], are obtained from eight different MOS capacitors each one directly irradiated to the dose shown in figure 9.6 and figure 9.7. For GD, measured in 2012, the results are from one MOS capacitor irradiated in steps to the doses given in the figure and annealed for 10 minutes at 80 °C after each step. Thus, it can be concluded that, under the same irradiation environment and annealing condition, the densities of defects introduced by X-ray ionizing radiation are independent of the way the irradiation is performed but just depend on the "accumulated dose" (TID effect).

From the dose dependence of the oxide-charge density N_{ox}, the interface-trap density N_{it} and the surface-current density J_{surf}, it is found that:

- N_{ox}, N_{it} and J_{surf} for <100> silicon before irradiation are lower than for <111> silicon produced by the same vendor, for example CiS. This difference remains even after irradiation to high doses. It should be noted that N_{ox}, N_{it} and J_{surf} for <100> and <111> silicon produced by CiS are different before irradiation: Both

[1]The thickness of the SiO_2 has been estimated from the capacitance of the MOS capacitor biased to accumulation assuming a Si_3N_4 thickness of 50 nm.

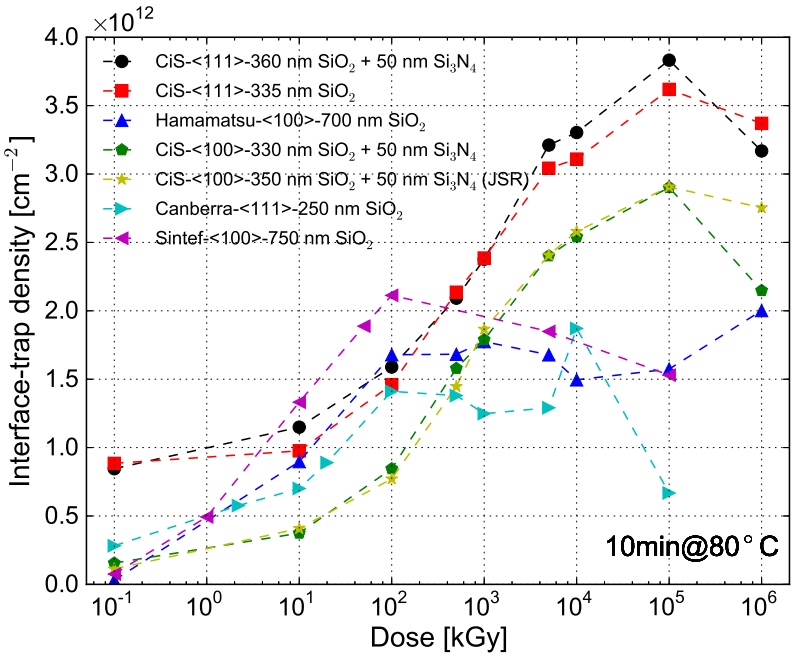

Figure 9.7: Dose dependence of N_{it} after annealing at 80 °C for 10 minutes. Results of N_{it} before irradiation are plotted at a dose of 10^{-1} kGy in the figure. The high values of N_{it} before irradiation are due to D^1_{it}, which is located at $\sim$ 0.39 eV with respect to the conduction band of silicon and is far away from the mid-gap of silicon. Therefore, it is not the main source of surface current.

N_{ox}, N_{it} and J_{surf} for <111> are higher than for <100>. To make sure the difference in N_{ox}, N_{it} and J_{surf} for <111> silicon and <100> silicon at high doses is not caused by their different values before irradiation, a <111> test field produced by CiS was annealed at 350 °C before irradiation to remove the large number of oxide charges and interface traps in the oxide and at the Si-SiO_2 interface. After annealing, the densities of oxide charges and interface traps are similar to those of non-irradiated <100> test fields. Then, the pre-annealed <111> test field and another one with orientation <100> were irradiated in one step to 5 MGy. Figure 9.9 shows the C/G-V curves of 1 kHz and 10 kHz on the left, and the TDRC spectra on the right for the two test fields. It is seen that the C/G-V curves for <111> silicon are shifted further than for <100> silicon to negative voltage, and the TDRC signal from <111> silicon is higher than the TDRC signal from <100> silicon. The extracted values of N_{ox} and N_{it} for <111> silicon are both 2.9×10^{12} cm^{-2}, which are higher than the values for <100> silicon (2.3×10^{12} cm^{-2} and 2.2×10^{12} cm^{-2}).

- There is no obvious dependence on the SiO_2 thickness. We interpret this that a thin layer of oxygen vacancies is present close to the Si-SiO_2 interface. In this case, independent of the thickness of the SiO_2 (but the thickness of the SiO_2 should be much larger than the characteristic depth of the distribution of oxygen vacancies), only holes produced in this thin layer of oxygen vacancies

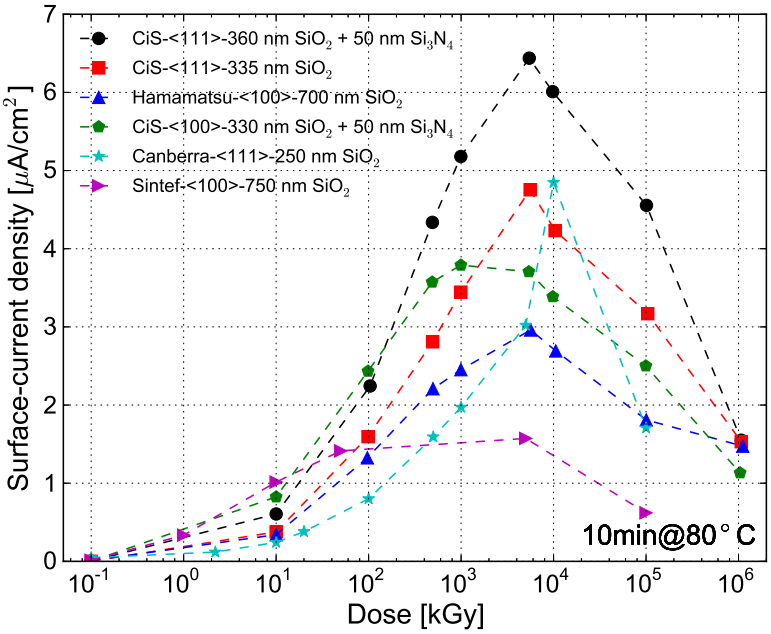

Figure 9.8: Dose dependence of J_{surf} after annealing at 80 °C for 10 minutes. Results of J_{surf} before irradiation are plotted at a dose of 10^{-1} kGy in the figure. Results give the minimal estimate for J_{surf}.

are captured and form oxide charges. However, the situation may change in case the characteristic depth of the distribution of oxygen vacancies is comparable to or larger than the thickness of the SiO_2. Then the dose dependence of defect densities depends on the SiO_2 thickness.

- Little difference in N_{ox} is observed for the MOS capacitors with an insulating layer made of SiO_2 and an insulating layer made of SiO_2 and Si_3N_4. For irradiations without any voltage applied to the gate, the electric field in the oxide during irradiation points from the Si-SiO_2 interface to the gate due to the build-up of oxide charges close to the Si-SiO_2 interface with irradiation. Hence, the interface between SiO_2 and Si_3N_4 for the MOS capacitor with an additional insulating layer of Si_3N_4 is able to capture electrons when they are produced in the Si_3N_4 and drift to the SiO_2. As a barrier exists at the SiO_2-Si_3N_4 interface[2], electrons hardly cross the barrier. The electrons thus can not drift into the SiO_2 from the Si_3N_4 and accumulate at the interface region. They are either captured by the defects at the SiO_2-Si_3N_4 interface or recombine with holes drifting to the Si_3N_4 from the SiO_2 due to the electric field. In the case the recombination effect is dominant, a negligible number of negative charges can be formed at the SiO_2-Si_3N_4 interface.
- The values found for samples fabricated by the four vendors differ by a factor

[2]The band gaps of Si_3N_4 and SiO_2 are 5.1 eV and 8.8 eV, respectively. And the conduction and valence bands of Si_3N_4 are within the band gap of SiO_2.

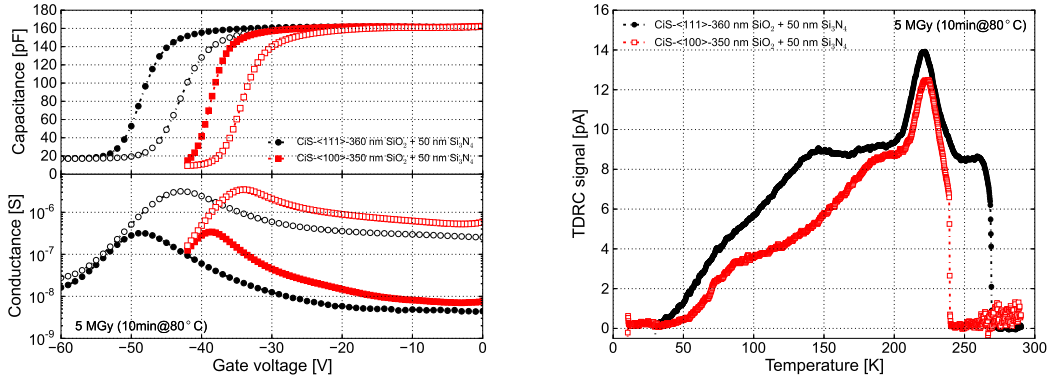

Figure 9.9: Crystal orientation dependence of C/G-V and TDRC measurements after irradiation to 5 MGy and annealing at 80 °C for 10 minutes. Left: C/G-V curves of 1 kHz and 10 kHz. Right: TDRC spectra. The extracted N_{ox} are 2.9×10^{12} cm^{-2} for <111> and 2.3×10^{12} cm^{-2} for <100>, respectively. The integrated N_{it} are 2.9×10^{12} cm^{-2} for <111> and 2.2×10^{12} cm^{-2} for <100>.

of 2 or 3, which indicates some dependence of radiation-induced defects on technology. For different technologies used in the fabrication of the oxide layer, the distribution of the oxygen vacancies in the SiO_2 is different, which results in a different dose dependence of radiation-induced defects. The distribution is known being related to the highest temperature and the time of the thermal oxidation [67]. The higher the temperature and "annealing" time, the larger the concentration of oxygen vacancies and the broader the distribution. As the technology-related parameters from different vendors are confidential, the issue related to technologies cannot be discussed further.

- N_{ox} and N_{it} saturate at high X-ray doses. The doses at which radiation-induced defects saturate are different for test fields produced by different vendors: For CiS, N_{ox} and N_{it} saturate at a dose between 10 MGy and 100 MGy; for Hamamatsu, Canberra and Sintef, N_{ox} and N_{it} saturate at $\sim$ 100 kGy. The saturation values of N_{ox} and N_{it} for all investigated test fields are in the range from 1.5×10^{12} to 3.8×10^{12} cm^{-2}. The saturation mechanism of N_{ox} can be explained in the following way: In the beginning of an irradiation, the hole-capture rate of oxygen vacancies is larger than the recombination rate of captured holes with electrons. Hence, the density of oxide charges increases with irradiation dose. At high doses, the electric field in the SiO_2 points from the Si-SiO_2 interface to the gate, which repels the holes produced in the SiO_2 away from the interface. Hence, the hole-capture rate of remaining oxygen vacancies at some moment equals to the recombination rate of captured holes with electrons. Thus, a saturation of the oxide charges is reached. An illustration of the saturation mechanism of the oxide charges is shown in figure 9.10. Due to the correlation between the formation of oxide charges and interface traps, the saturation of the interface traps is also expected.
- J_{surf} saturates (reaches the maximum) at doses between 1 MGy and 10 MGy and

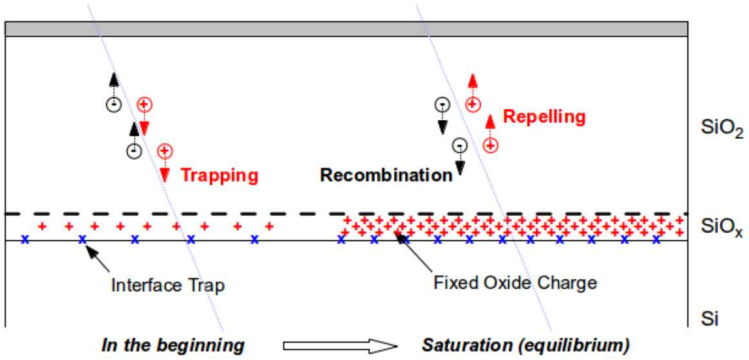

Figure 9.10: An explanation of the saturation mechanism of the oxide-charge density N_{ox} at high doses. The arrow indicates the direction of electrons or holes drift.

then decreases with irradiation dose. On one hand, the surface current increases with irradiation, which results in the increase of J_{surf}. On the other hand, the mobility of minority carriers below the Si-SiO_2 interface decreases with irradiation [68, 69]. The decrease of J_{surf} can be understood as a result of the reduction of the critical gate length L_{cri}. The radiation-induced oxide charges and interface traps at the Si-SiO_2 interface result in a non-uniform distribution of surface potential below the interface: When the interface region close to the p^+ implant (inner part below the gate) is in depletion, the interface region away (outer part below the gate) can be already in inversion. The critical gate length L_{cri} is a function of the surface-generation velocity and the effective mobility of minority carriers below the Si-SiO_2 interface (also see formula (8.3)). Therefore, the increase of the surface-generation velocity (interface traps) and the reduction of the mobility of minority carriers cause a reduction of the critical length L_{cri} and thus reduces the surface-current density J_{surf} being measured. Hence, the method to extract J_{surf} for highly irradiated gate-controlled diodes gives a value which is too small. According to the measurements and simulation results reported by G.-F. Dalla Betta [70], the relative accuracy of the J_{surf} extracted with this method is about $< 1\%$ for a gate length of 50 μm and about 50% for a gate length of 210 μm with a low surface-generation velocity (~ 10 cm/s). However, the error increases quickly with irradiation: A calculation based on the formulae derived by Pierret [59, 60] and Dugas [61] shows that the extracted surface-current densities can be as low as 30% of the expected values for a gate length of 50 μm at a high dose corresponding to a surface-generation velocity of 10^4 cm/s.

Results on the dose dependence of N_{ox}, N_{it} and J_{surf} are given in appendix A.2, A.3, A.5, A.6, A.7, and A.4.

Figure 9.11(left) shows the dose dependence of N_{it}-to-N_{ox} ratio. It is found that the values of N_{it}/N_{ox} for overall investigated test fields saturate at ~ 1 at high doses. This indicates a strong correlation between the formations of oxide charges and interface traps.

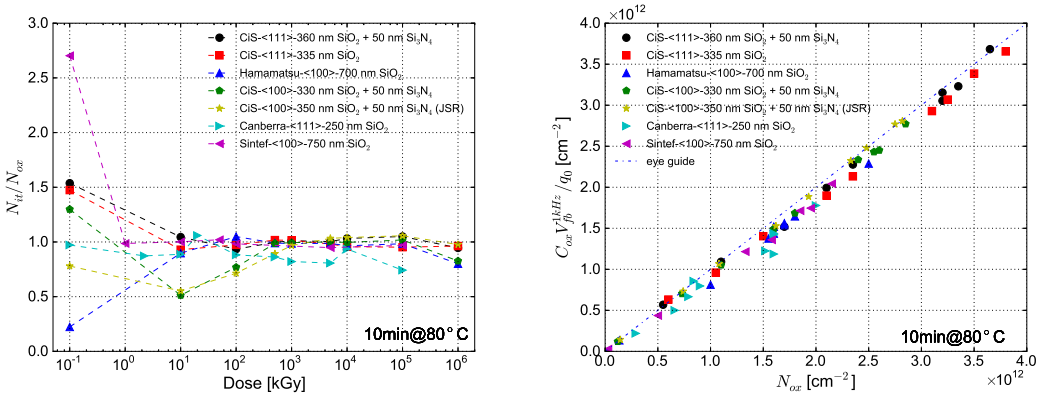

Figure 9.11: Left: The N_{it}-to-N_{ox} ratio. Right: The empirical relation between the N_{ox} extracted from the model calculation and the value calculated from $C_{ox}V_{fb}^{1\,\mathrm{kHz}}/q_0$.

An empirical formula is found for the extraction of N_{ox}. As seen in figure 9.11(right), the charge densities calculated by $C_{ox}V_{fb}^{1\,\mathrm{kHz}}/q_0$ for all investigated MOS capacitors are able to fairly describe the oxide-charge density N_{ox} extracted from the model calculation. $V_{fb}^{1\,\mathrm{kHz}}$ is the voltage of the C-V curve measured at 1 kHz at which the capacitance equals to the flatband capacitance of a non-irradiated MOS capacitor. The empirical formula provides a fast method to extract the N_{ox}. For the extraction of N_{ox} for the MOS capacitors after irradiation but before annealing, this method was used due to the lack of available TDRC measurements. However, it should be stressed that the values are obtained only under the assumptions made in chapter 8.

9.4. Summary

Results on the oxide-charge densities, the interface-trap densities and the surface-current densities from MOS capacitors and gate-controlled diodes built on high resistivity n-type silicon with orientations of <100> and <111> produced by four vendors, CiS, Hamamatsu, Canberra and Sintef, as function of 12 keV X-ray doses up to 1 GGy have been presented. The oxide-charge densities, the interface-trap densities and the measured surface-current densities either saturate or decrease at high doses, which can be explained either by a mechanism of saturation between hole-capture and electron-recombination or by a reduction of critical length of the gate. The extracted oxide-charge densities in this study give the maximal estimate of their values based on the assumptions made in chapter 8, however the surface-current densities give the minimal estimate. The extracted surface-current densities are expected to be about 10% to 70% smaller than their real values.

The results obtained in this study provide inputs in TCAD simulations for the sensor optimization for the AGIPD.

10. Gate-voltage dependence of N_{ox}, N_{it} and J_{surf}

The presence of an electric field in the SiO_2 during the X-ray irradiation plays an important role in the formation of oxide charges and interface traps: It determines not only the fraction of electrons and holes escaping from the initial recombination, but also the direction that the electrons and holes drift, which impacts on the amount of oxide charges and interface traps that form in the Si-SiO_2 interface region.

In order to investigate the formation of oxide charges and interface traps as function of the electric field, a number of test fields have been irradiated to doses of 100 kGy and 100 MGy with different gate voltages applied during irradiation. Measurement results on the C/G-V curves, I-V curves and TDRC spectra are shown in this chapter, and the gate-voltage dependence of the oxide-charge density, interface-trap density and surface-current density presented. Finally, the relevance of the results to the sensors for the XFEL is discussed.

10.1. Investigated structures and their electrical properties before irradiation

Two groups of test fields, labelled CE20xx[1] and CG10xx[2], are used in this study. Every group includes 5 test fields. Each test field consists of a MOS capacitor and a gate-controlled diode. The shapes and geometrical parameters[3] of the CiS test structures have been described in chapter 9.

The investigated test fields are fabricated on high resistivity n-type silicon with an orientation of <100> by CiS. Table 10.1 is a list of the general properties of the test fields used in this study.

Figure 10.1(a)-(d) are the C-V, G-V, I-V curves and the TDRC spectrum from the non-irradiated test fields. The total density of interface traps N_{it} before irradiation, is calculated by integrating the TDRC signal I_{tdrc} divided by the heating rate β used in the measurement and the elementary charge q_0: $N_{it} = 1/(\beta \cdot q_0) \cdot \int I_{tdrc} \mathrm{d}T$ = 1.1 $\times$ 10^{11} cm^{-2} for CE20xx and 2.3 $\times$ 10^{11} cm^{-2} for CG10xx. The oxide-charge density, N_{ox}, is calculated according to the model introduced in chapter 6 by inputting the measured TDRC spectra, which gives a value of 1.2 $\times$ 10^{11} cm^{-2} for CE20xx and 2.5 $\times$ 10^{11} cm^{-2} for CG10xx. The surface-current density at 20 °C, $J_{surf}(T = 20°C)$, is

[1] CE20xx: CE2016, CE2023, CE2039, CE2050 and CE2350.

[2] CG10xx: CG1016, CG1023, CG1039, CG1050 and CG1223.

[3] The MOS capacitor has a circular shape with a diameter of 1.5 mm. The gate-controlled diode contains a circular diode (diameter $\sim$ 1.0 mm) in the center and 5 concentric surrounding gate rings. The width of the gate rings is 50 μm and neighbouring gate rings are separated by 5 μm spacing.

Label	CE20xx	CG10xx
Material	FZ	DOFZ
Orientation	<100>	<100>
Doping	6.3×10^{11} cm^{-3}	8.2×10^{11} cm^{-3}
Insulator	330 nm SiO_2 + 50 nm Si_3N_4	360 nm SiO_2 + 50 nm Si_3N_4
N_{ox}	1.2×10^{11} cm^{-2}	2.5×10^{11} cm^{-2}
N_{it}	1.1×10^{11} cm^{-2}	2.3×10^{11} cm^{-2}
J_{surf}	$\sim$ 1.3 nA/cm^2	$\sim$ 1.3 nA/cm^2

Table 10.1: Properties of the test fields used for the gate-voltage dependence of N_{ox}, N_{it} and J_{surf}.

determined from the surface current I_{surf} scaled to 20 °C and the area of the 1^{st} gate ring of the gate-controlled diode A^{1st}_{gate}: $J_{surf}(T = 20°C) = I_{surf}(T = 20°C)/A^{1st}_{gate} = 1.3$ nA/cm^2, which is similar for both group of test fields.

Differences in N_{ox} and N_{it} are found for CE20xx and CG10xx. The values of N_{ox} and N_{it} for CE20xx are about 50% lower than the one for CG10xx. The differences are assumed to be caused by different processes for the two groups of test fields: Compared to the standard process for CE20xx, CG10xx underwent an additional oxygen-enrichment process at 1150 °C for 48 hours. The mechanism leading to the increase of N_{ox} and N_{it} due to additional/different process step is not clear so far. As the interest in this study is the gate-voltage dependence of N_{ox} and N_{it} of test fields in each group with irradiation, the differences will not be a concern after irradiation.

The two groups of test fields were irradiated to 100 kGy (CE20xx) and 100 MGy (CG10xx). During irradiation, gate voltages of -25 V, -10 V, 0 V, 10 V and 25 V were applied to the five test fields in each group, respectively. The maximum applied gate voltage, 25 V, corresponds to an electric field of $\sim$ 0.7 MV/cm in the SiO_2, which is far below the electric field of $\sim$ 10 MV/cm causing oxide breakdown.

10.2. Measurements after irradiation

C/G-V, I-V and TDRC measurements were performed for CE20xx and CG10xx after irradiation. For the C/G-V measurements on the MOS capacitors, the gate voltage was scanned from a value corresponding to accumulation to a value corresponding to weak inversion, in order to avoid injecting holes into the border traps in the SiO_2. The I-V curves were measured on the gate-controlled diodes from 0 V (accumulation) to a voltage when surface current disappears (strong inversion). For the TDRC measurement, the gate voltage applied to the MOS capacitors was 0 V (accumulation) during cooling down. During heating up, the gate voltage at which the C/G-V measurements stopped was applied. The heating rate β of the TDRC measurement was 0.183 K/s.

Same measurements were performed on the test fields of each group.

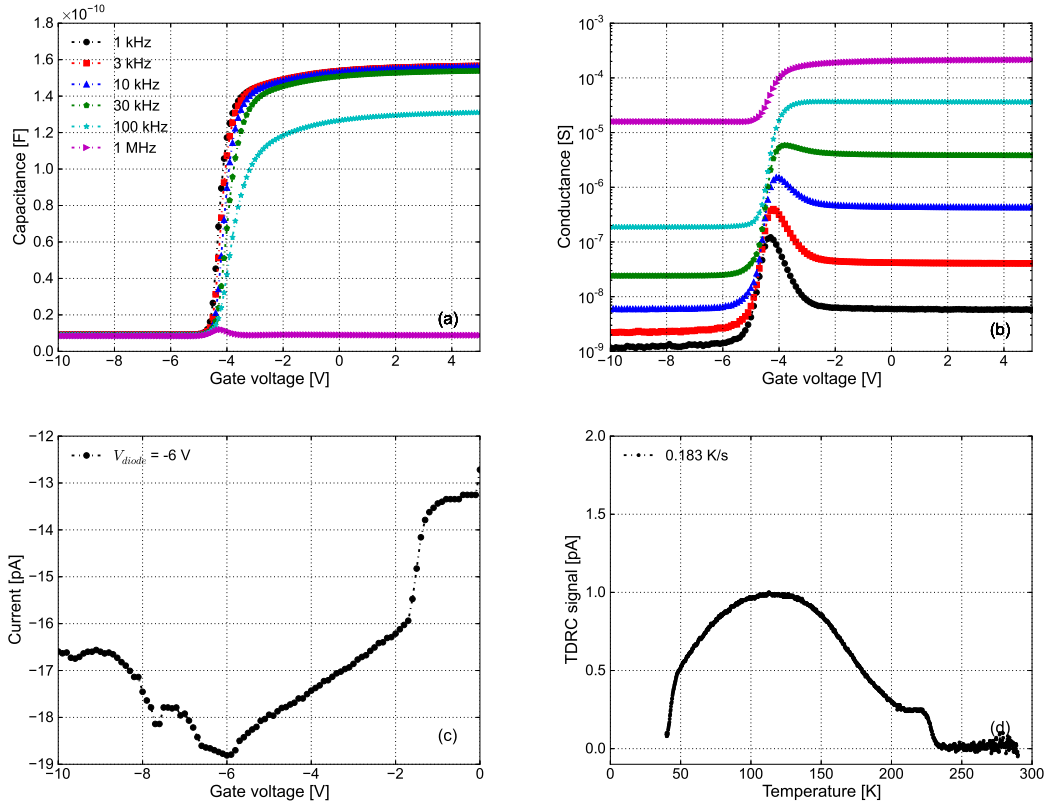

Figure 10.1: Measurements on the non-irradiated test fields: (a) C-V curves of the MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of the MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of the gate-controlled diode for V_{diode} = -6 V. (d) TDRC spectrum of the MOS capacitor. Results for CG10xx are shown.

10.2.1. C/G-V curves of MOS capacitors

Figure 10.2(a)-(d) show the C/G-V curves of the two group of test fields with different gate voltages applied (V_{irrad}) during irradiation. Curves of 1 kHz and 10 kHz are shown in the figure.

Compared to the C/G-V curves before irradiation, the X-ray irradiation causes shifts in gate voltage of at least 10 V for 100 kGy and 30 V for 100 MGy. Increases of the peak values of the conductance are caused by the increase of the interface traps at the Si-SiO_2 interface.

For 100 kGy, gate voltages of -25 V, 10 V and 25 V applied during irradiation result in larger shifts in the C/G-V curves than the gate voltage of 0 V, which indicates more positive charges are created in the SiO_2. For 100 MGy, compared to the gate voltage of 0 V, gate voltages of 10 V and 25 V cause larger shifts in C/G-V curves and however -10 V and -25 V cause less. This behaviour will be discussed in detail in the following section when summarizing the results on the oxide-charge density, interface-trap density and surface-current density.

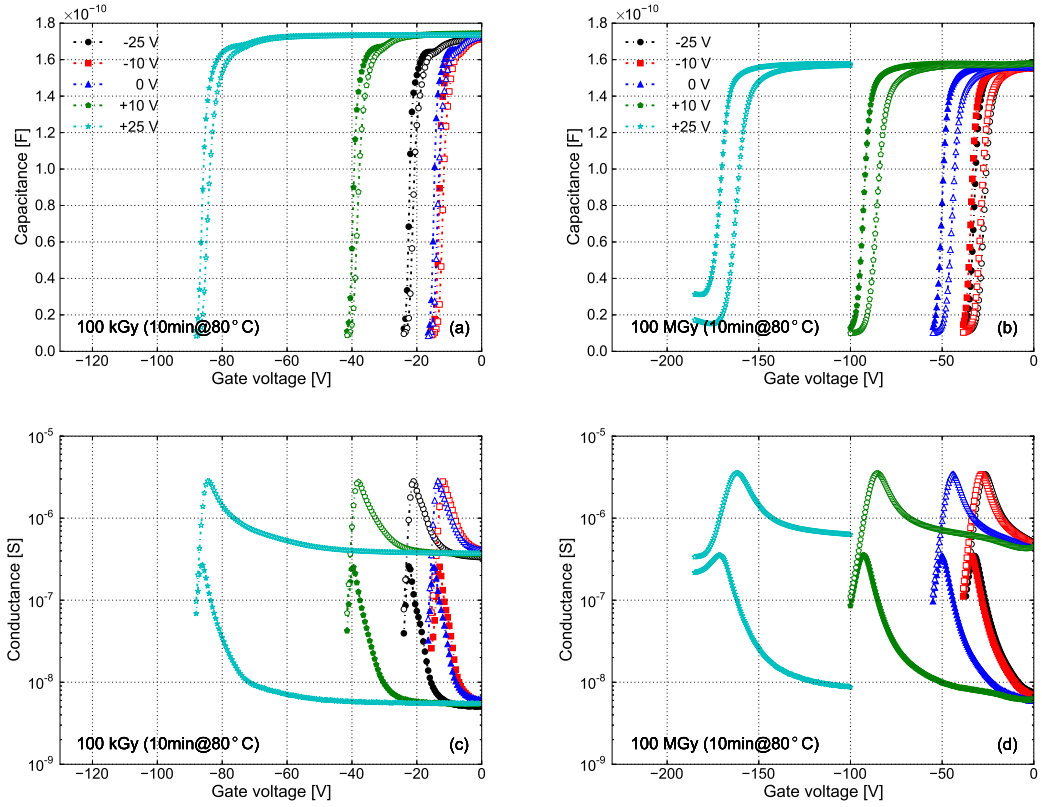

Figure 10.2: Measurements on the MOS capacitors: (a) C-V curves of the MOS capacitor irradiated to 100 kGy, annealed at 80 °C for 10 minutes. (b) C-V curves of the MOS capacitor irradiated to 100 MGy, annealed at 80 °C for 10 minutes. (c) G-V curves of the MOS capacitor irradiated to 100 kGy, annealed at 80 °C for 10 minutes. (d) G-V curves of the MOS capacitor irradiated to 100 MGy, annealed at 80 °C for 10 minutes. Frequencies of 1 and 10 kHz are shown: Filled symbols - 1 kHz; open symbols - 10 kHz. The values of V_{irrad} are shown in the legend.

10.2.2. TDRC spectra of MOS capacitors

Figure 10.3 show the TDRC signals for different gate voltages applied to the MOS capacitors during irradiation to 100 kGy and 100 MGy. The distributions of the TDRC signal as function of temperature for 100 kGy are similar to a standard TDRC signal measured from a CiS MOS capacitor with an orientation of <100>. However for 100 MGy, the TDRC signals for V_{irrad} of 10 V and 25 V show a pronounced peak around 180 K in addition to the one at $\sim$ 220 K, which indicates different gate-voltage dependence of individual traps in the TDRC spectra. Another interesting feature is that, for V_{irrad} of -10 V and -25 V, the TDRC signals are very small below 90 K, which may indicate a deformation or change of the configuration of the interface traps. This is still an issue to be understood in a future study.

The dependence of TDRC signals on V_{irrad} is, as expected, similar to that of the C/G-V shifts. This confirms the correlation between the formation of interface traps

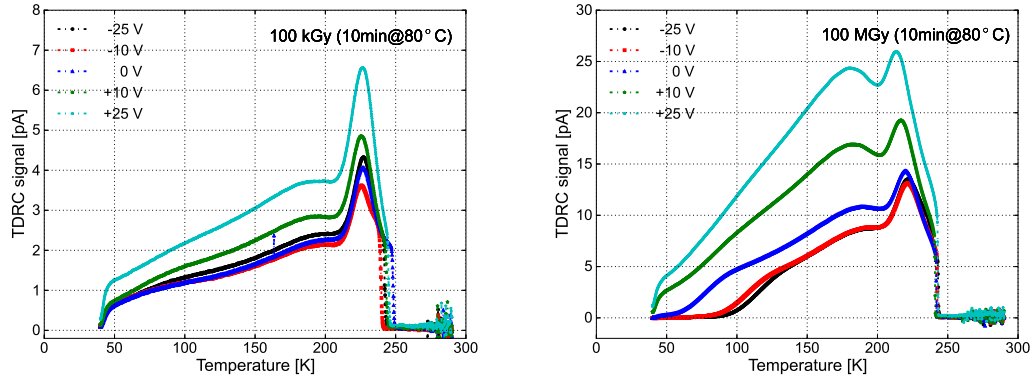

Figure 10.3: Measurements on the MOS capacitors. Left: TDRC spectra of the MOS capacitor irradiated to 100 kGy, annealed at 80 °C for 10 minutes. Right: TDRC spectra of the MOS capacitor irradiated to 100 MGy, annealed at 80 °C for 10 minutes. The values of V_{irrad} are shown in the legend. The TDRC spectra were always measured under the gate voltages of V_{merge}.

and the formation of oxide charges: The former is due to the reaction between protons and passivated dangling silicon bonds, in which the protons are released after holes reacting with hydrogenated oxygen vacancies; the latter however is due to the holes trapped by the oxygen vacancies.

10.2.3. I-V curves of gate-controlled diodes

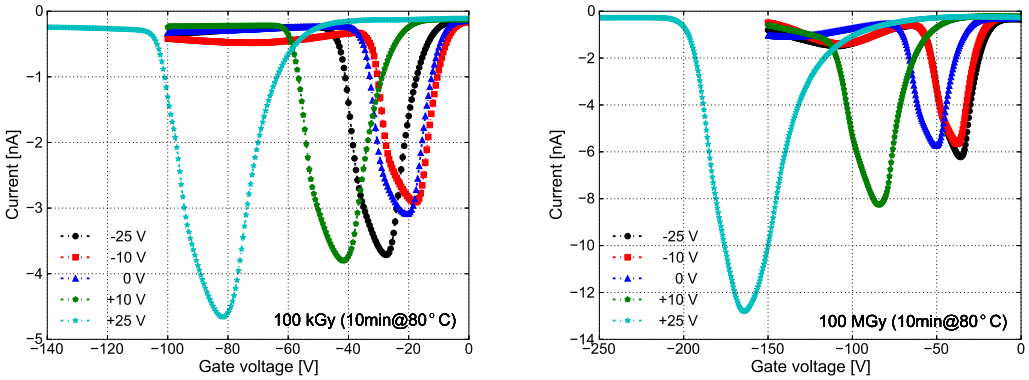

Figure 10.4: Measurements on the gate-controlled diodes. Left: I-V curves of the gate-controlled diode irradiated to 100 kGy, annealed at 80 °C for 10 minutes. Right: I-V curves of the gate-controlled diode annealed irradiated to 100 MGy, annealed at 80 °C for 10 minutes.

The gate-voltage dependence of the I-V curves measured from the gate-controlled diodes are shown in figure 10.4. At 100 kGy and 100 MGy, the surface current for -10 V are in the same level as the surface current for 0 V ($\sim$ 3.0 nA for 100 kGy and

$\sim$ 5.5 nA for 100 MGy). At -25 V, 10 V and 25 V the surface current is larger than at -10 V and 0 V. The behaviour will be discussed in the following.

10.3. Results: N_{ox}, N_{it} and J_{surf} vs. V_{irrad}

Figure 10.5 shows the gate-voltage dependence of the oxide-charge density, N_{ox}, the interface-trap density, N_{it}, and the surface-current density, J_{surf}, for doses of 100 kGy and 100 MGy. The maximum applied gate voltage, 25 V, corresponds to an electric field of $\sim$ 0.7 MV/cm in the SiO_2. The results will be discussed for three cases:

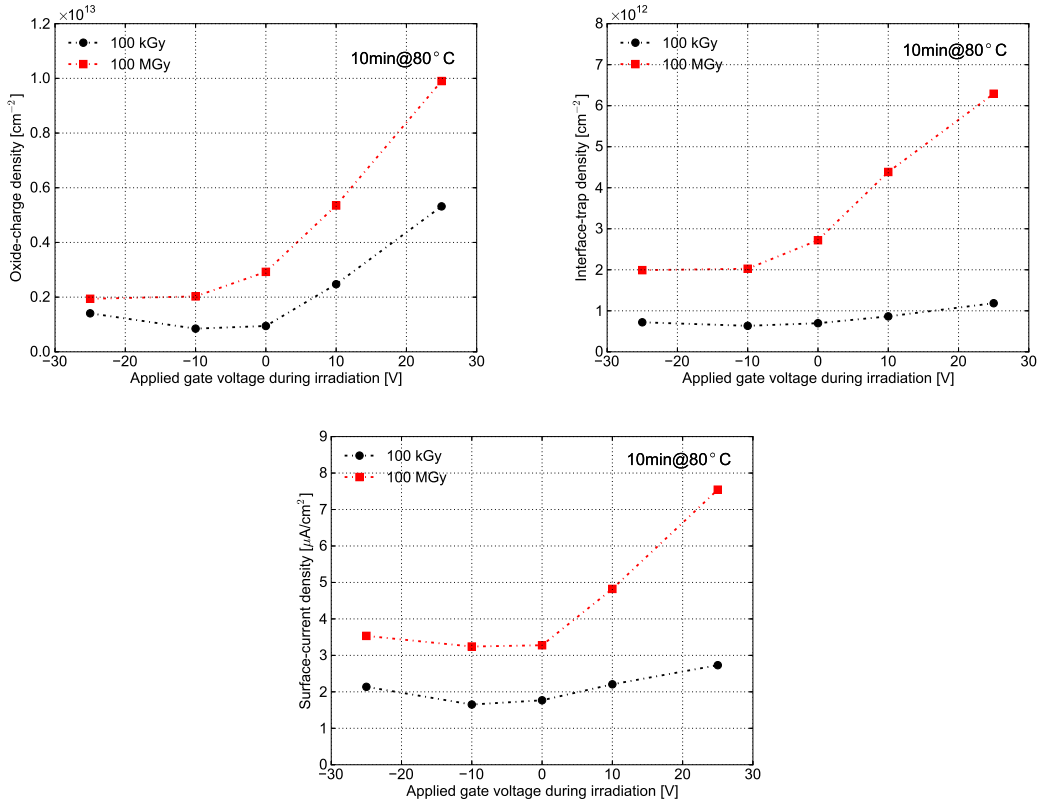

Figure 10.5: Top left: Gate-voltage dependence of the oxide-charge density N_{ox} for the MOS capacitors irradiated to 100 kGy and 100 MGy, annealed at 80 °C for 10 minutes. Top right: Gate-voltage dependence of the interface-trap density N_{it} for the MOS capacitors irradiated to 100 kGy and 100 MGy, annealed at 80 °C for 10 minutes. Bottom: Gate-voltage dependence of the oxide-charge density J_{surf} for the gate-controlled diodes irradiated to 100 kGy and 100 MGy, annealed at 80 °C for 10 minutes.

(i) For $V_{irrad} = 0$ V, the initial electric field in the SiO_2 is zero and thus the situation is similar to the case without gate voltage applied during irradiation. In both cases, the electric field in the SiO_2 during irradiation is dominated by the field created by the oxide charges, which points from the Si-SiO_2 interface to the aluminium gate. Hence,

the values of N_{ox} and J_{surf} obtained under 0 V are similar to the values obtained without gate voltage applied during irradiation.

(ii) For $V_{irrad} < 0$ V, the direction of the electric field in the SiO_2 points from the Si-SiO_2 interface to the aluminium gate, as for 0 V. The electric field in the SiO_2 is the sum of the electric field due to external voltage and that created by the positive oxide charges close to the Si-SiO_2 interface. With increasing "accumulated dose", the electric field due to the oxide charges increases; thus, the fraction of the electric field due to the gate voltage is reduced. For example, the electric field created by the oxide charges with a density of $N_{ox} = 2 \times 10^{12}$ cm^{-2} is $\sim$ 0.9 MV/cm if it is assumed that the oxide charges are located at the interface, compared to a field of 0.7 MV/cm for a gate voltage of -25 V. Therefore, no big difference is observed between the values of N_{ox} and J_{surf} obtained under negative gate voltage and under 0 V. However, the situation may change for a different spatial distribution of oxygen vacancies in the SiO_2.

(iii) For $V_{irrad} > 0$ V, the direction of the electric field in the SiO_2 points from the aluminium gate to the Si-SiO_2 interface. The number of holes drifting to the interface is larger than for $V_{irrad} < 0$ V and $V_{irrad} = 0$ V. Thus, more holes are captured by the oxygen vacancies located close to the interface and produce oxide charges. As the fraction of holes escaping from the initial recombination process increases with the electric field in the SiO_2, the number of holes drifting to the interface increases with the positive gate voltage applied to the aluminium gate. Thus, a strong voltage dependence of N_{ox} and J_{surf} is observed in this case.

10.4. Summary

The influences of the voltage applied to the gates of the MOS capacitor and the gate-controlled diode during X-ray irradiation on the oxide-charge density, (integrated) interface-trap density and surface-current density has been investigated at doses of 100 kGy and 100 MGy. It is found that both strongly depend on the gate voltage if the electric field in the oxide points from the surface of the SiO_2 to the Si-SiO_2 interface.

At the European XFEL, p^+n silicon pixel sensors will be used for the AGIPD detector. For this type of sensor, the potential in the gap region below/at the Si-SiO_2 interface is > 0 V, which gives an electric field in the SiO_2 pointing from the Si-SiO_2 interface to the readout electrodes. In this sense, the sensor is operated in a situation similar to a negative gate voltage applied to the MOS capacitor and the gate-controlled diode; hence, no large differences in the oxide-charge density and the surface-current density extracted from the study of their dose dependence are expected.

11. Time and temperature dependence of N_{ox}, N_{it} and J_{surf}

Radiation-induced defects influence the electrical properties of silicon sensors. In order to understand the long-term performance and stability of silicon sensors, the annealing behaviour of the oxide-charge density, interface-trap density and surface-current density have to be known.

In this chapter, annealing kinetics of oxide charges and interface traps are discussed based on a modified "tunnelling model" [71, 72] and the "two reaction model" [73]. Measurement results on C/G-V curves and TDRC signals of MOS capacitors and I-V curves of gate-controlled diodes, both of which have been irradiated to a dose of 5 MGy and annealed at 60 °C and 80 °C, are presented. In addition, the oxide-charge density N_{ox} and surface-current density J_{surf} as function of time at 60 °C and 80 °C are fitted with functions derived from the "tunnelling model" and "two reaction model", and extrapolated parameters determined. Finally, the evolution with time of N_{ox} and J_{surf} for different annealing temperatures are shown.

11.1. Annealing kinetics

The formation of oxide charges and interface traps due to ionizing radiation follow different mechanisms: The former is caused by the hole-trapping, whereas the latter is due to the breaking of Si-H bonds. Hence, the annealing of oxide charges and interface traps is due to different processes: The annealing of oxide charges is due to the removal of trapped holes, the annealing of interface traps due to the passivation of dangling silicon bonds. In this chapter, the annealing kinetics of oxide charges and interface traps are introduced separately.

11.1.1. Annealing model for oxide charges

The annealing of oxide charges is described by two different hole-removal processes [17]. Below $\sim$ 125 °C, the removal of oxide charges is mainly due to the recombination of trapped holes with electrons tunnelling into the SiO_2 from the silicon, which has been described by a tunnelling model [71,72]. Above $\sim$ 150 °C, a rapid removal or recombination of trapped holes in the SiO_2 can be observed, which is described by a thermal detrapping model [74]. As silicon sensors normally work in a temperature range from -20 °C to room temperature, tunnel anneal is the dominant process in our applications.

Figure 11.1 illustrates the tunnel-anneal process. The trapped holes close to the Si-SiO_2 interface recombine with electrons which tunnel from the silicon substrate.

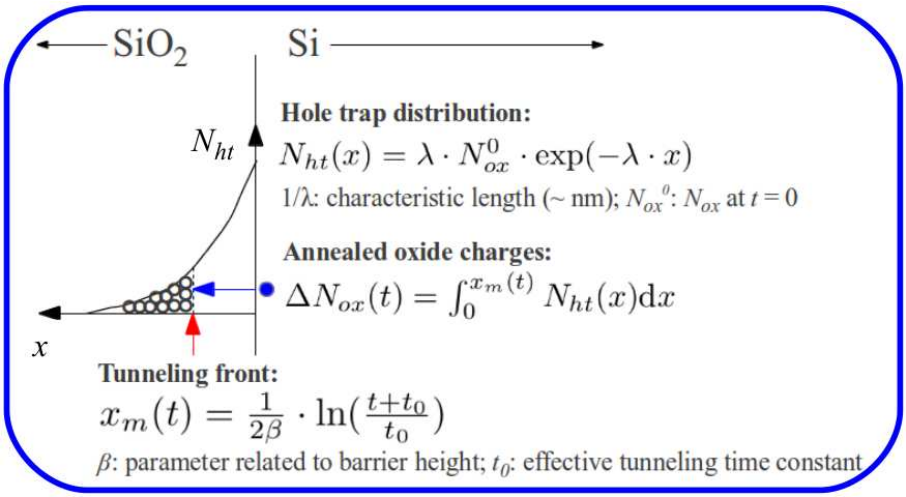

Figure 11.1: Annealing kinetic of the oxide-charge density N_{ox}.

According to the tunnelling theory [75], the tunnelling front $x_m(t)$[1], defined as the maximum depth that electrons are able to tunnel into the SiO_2, increases logarithmically with time, as

$$x_m(t) = \frac{1}{2\beta}\ln\left(\frac{t+t_0}{t_0}\right) \tag{11.1}$$

where β is a parameter related to the barrier height the electrons have to overcome, and t_0 the effective tunnelling time constant related to the fundamental transition rate to the closest traps in the oxide [74]. It should be mentioned that the formula for the tunnelling front x_m has been modified compared to the original one: t is replaced by $t + t_0$ to avoid unreasonable negative value for $t < t_0$. In this case, the correct initial condition $x_m(0) = 0$ can be satisfied.

The density of oxide charges annealed with time t, $\Delta N_{ox}(t)$, can be calculated by

$$\Delta N_{ox}(t) = \int_0^{x_m(t)} N_{ht}\,(x)\,\mathrm{d}x \tag{11.2}$$

where as shown in figure 11.1 x is the distance to the Si-SiO_2 interface, $x_m(t)$ given by eq.(11.1) and $N_{ht}(x)$ the spatial distribution of occupied hole traps in the SiO_2. Although $N_{ht}(x)$ is not known, it is commonly assumed that the spatial distribution of the hole traps follows an exponential function,

$$N_{ht}(x) = \lambda \cdot N_{ox}^0 \cdot \exp\left(-\lambda \cdot x\right) \tag{11.3}$$

with $1/\lambda$ the characteristic depth of the hole-trap distribution and N_{ox}^0 the oxide-charge density at $t = 0$. Then, performing the integration in eq.(11.2) and subtracting $\Delta N_{ox}(t)$ from N_{ox}^0 , the oxide-charge density at any time t, $N_{ox}(t)$, can be written as

[1] $x_m(t)$ is the boundary of the region where the trapped holes have recombined after a time t.

$$N_{ox}(t) = N_{ox}^{0} \cdot \left(1 + \frac{t}{t_0}\right)^{-\frac{\lambda}{2\beta}} \tag{11.4}$$

In addition, the effective tunnelling time constant t_0 at any temperature T, by using the Wentzel-Kramers-Brillouin (WKB) approximation and adding up all possible transitions [76], can be approximated:

$$t_0(T) = t_0^* \cdot \exp\left(\frac{\Delta E}{k_B T}\right) \tag{11.5}$$

with t_0^* the tunnelling time constant, ΔE the difference between the energy level of the defects in the SiO_2 and the Fermi level of silicon, k_B the Boltzmann constant.

11.1.2. Annealing model for interface traps

The annealing mechanism of interface traps (dangling silicon bonds) has not been fully understood yet. A traditional annealing model of interface traps is a bi-molecular recombination of a hydrogen atom and a dangling silicon bond Si· [73]:

$$\mathrm{Si} \cdot + \mathrm{H} \rightarrow \mathrm{SiH} \tag{11.6}$$

where SiH is the shorthand notation for $\mathrm{Si_3} \equiv \mathrm{Si} - \mathrm{H}$, which stands for a silicon atom with three covalent bonds with neighbouring silicon atoms and one covalent bond with a hydrogen atom. The reaction can be expressed as a differential equation [73]:

$$\frac{\mathrm{d}}{\mathrm{d}t} N_{it} = -k_1 \cdot N_{it} \cdot N_H \tag{11.7}$$

with k_1 the rate constant of the bimolecular reaction, N_{it} the density of the dangling silicon bonds (interface traps) and N_H the concentration of the hydrogen atoms. It should be noted that the units of k_1, N_{it} and N_H are $\mathrm{cm^3 \cdot s^{-1}}$, $\mathrm{cm^{-2}}$ and $\mathrm{cm^{-3}}$, respectively. If no other reactions are involved, integrating eq.(11.7) results in an exponential decay of interface-trap density with time. However, the simple exponential function is not able to describe the experimental data. Hence, to explain the measurement results, in addition to the above reaction (11.6), a second reaction is introduced [73]:

$$\mathrm{H} + \mathrm{H} \rightarrow \mathrm{H_2} \tag{11.8}$$

Reaction (11.8) describes the binding of two hydrogen atoms to a hydrogen molecule, which occurs in the SiO_2. The corresponding differential equation for this reaction can be written as, either second order process

$$\frac{\mathrm{d}}{\mathrm{d}t} N_H = -2k_2 \cdot N_H \cdot N_H \tag{11.9}$$

for the non-consumptive mechanism of hydrogen atoms in reaction (11.6), or

$$\frac{\mathrm{d}}{\mathrm{d}t} N_H = -\frac{k_1}{t_{ox}} \cdot N_{it} \cdot N_H - 2k_2 \cdot N_H \cdot N_H \tag{11.10}$$

for the consumptive mechanism of hydrogen atoms in reaction (11.6). k_2 is the rate constant of the reaction between two hydrogen atoms, and t_{ox} the thickness of the oxide.

For the consumptive mechanism, eq.(11.7) and (11.10) are coupled and cannot be solved analytically. To find the interface-trap density N_{it} at any time t, one must resort to numerical techniques. However, for the non-consumptive mechanism, it is possible to obtain an analytical expression. Eq.(11.9) can be solved for N_H:

$$N_H(t) = \frac{N_H^0}{1 + 2k_2 \cdot N_H^0 \cdot t} \tag{11.11}$$

with N_H^0 the initial concentration of hydrogen atoms at $t = 0$. Hence, substituting the solution for N_H into eq.(11.7), the solution for N_{it} is

$$N_{it}(t) = N_{it}^0 \cdot \left(1 + \frac{t}{t_1}\right)^{-\eta} \tag{11.12}$$

where N_{it}^0 is the interface-trap density at $t = 0$, η is a parameter related to the ratio of the two rate constants of the two reactions, $\eta = k_1/2k_2$, and t_1 is the annealing time constant, $t_1 = 1/(2k_2 N_H^0)$. t_1 is assumed to depend on temperature according to

$$t_1(T) = t_1^* \cdot \exp\left(\frac{E_\alpha}{k_B T}\right) \tag{11.13}$$

with $1/t_1^*$ the frequency factor and E_α the activation energy.

As the interface traps close to the mid-gap of silicon contribute to the surface current, the annealing of surface-current density J_{surf} can be also expressed in a way analogous to eq.(11.12):

$$J_{surf}(t) = J_{surf}^0 \cdot \left(1 + \frac{t}{t_1}\right)^{-\eta} \tag{11.14}$$

with J_{surf}^0 the surface-current density at $t = 0$.

11.2. Investigated structures and their electrical properties before irradiation

Two test fields, labelled CB0416 and CB0423, produced by CiS are investigated for the annealing study. Each test field consists of a MOS capacitor and a gate-controlled diode[2], as mentioned in a previous chapter.

The investigated test fields are fabricated on high resistivity n-type silicon with an orientation of <111> produced by CiS. Table 11.1 is a list of the properties of the test fields used in the annealing study.

[2]The MOS capacitor has a circular shape with a diameter of 1.5 mm. The gate-controlled diode contains a circular diode (diameter $\sim$ 1.0 mm) in the center and 5 concentric gate rings. The width of the gate rings is 50 μm and neighbouring gate rings are separated by 5 μm.

Label	CB0416 and CB0423
Material	DOFZ
Orientation	<111>
Doping	1.2×10^{12} cm^{-3}
Insulator	360 nm SiO_2 + 50 nm Si_3N_4
N_{ox}	5.6×10^{11} cm^{-2}
N_{it}	8.9×10^{11} cm^{-2}
J_{surf}	2.8 nA/cm^2

Table 11.1: Properties of the test fields used for annealing study. The high density of interface traps, whose energy level is located at $\sim$ 0.39 eV with respect to the conduction band of silicon, is not the main source of the surface current.

Figure 11.2(a)-(d) show the C-V, G-V, I-V and TDRC curves measured on the non-irradiated test fields. The total density of interface traps, N_{it} before irradiation, is estimated by integrating the TDRC signal I_{tdrc} divided by the heating rate β used in the measurement and the elementary charge q_0: $N_{it} = 1/(\beta \cdot q_0) \cdot \int I_{tdrc} dT = 8.9 \times 10^{11}$ cm^{-2}. The oxide-charge density, N_{ox}, is calculated according to the model introduced in chapter 6 by putting in the measured TDRC spectra, which gives a value of 5.6 $\times$ 10^{11} cm^{-2}. The surface-current density at 20 °C, $J_{surf}(T = 20°C)$, is determined from the surface current I_{surf} scaled to 20 °C and the area of the 1^{st} gate ring of the gate-controlled diode A^{1st}_{gate}: $J_{surf}(T = 20°C) = I_{surf}(T = 20°C)/A^{1st}_{gate} = 2.8$ nA/cm^2. It should be noted that the TDRC signal at $\sim$ 135 K for the non-irradiated MOS capacitors is as large as 9 pA. The reason of the large TDRC signal before irradiation is not clear so far, but it is supposed that the large TDRC signal is caused by an additional oxygen-enrichment process, which is the only different process compared to the other MOS capacitors giving small TDRC signals. This interface trap is not the cause of the surface current because its energy level is far away from the silicon mid-gap. The large TDRC signal before irradiation will be added to the signal due to the traps introduced by X-ray irradiation and thus it will change the shape of the distribution of $I_{tdrc}(T)$. However, the large values of N_{ox} and N_{it} before irradiation are not expected to change the annealing behaviour of N_{ox} and N_{it} after irradiation as their same origins.

Both test fields were irradiated to a dose of 5 MGy for the annealing study. The annealing has been performed at 80 °C and 60 °C for CB0416 and CB0423, respectively.

11.3. Measurements after irradiation

C/G-V, I-V and TDRC measurements were performed for CB0416 and CB0423 after each annealing step. The C/G-V curves were measured on the MOS capacitors by scanning the gate voltage from 0 V down to a voltage when C-V curves of 1 kHz and 10 kHz merge in inversion, in order not to inject holes into the border traps in SiO_2. Injecting holes into the border traps causes a shift of C/G-V curves in gate voltage, which makes the determination of N_{ox} difficult. The I-V curves were always measured

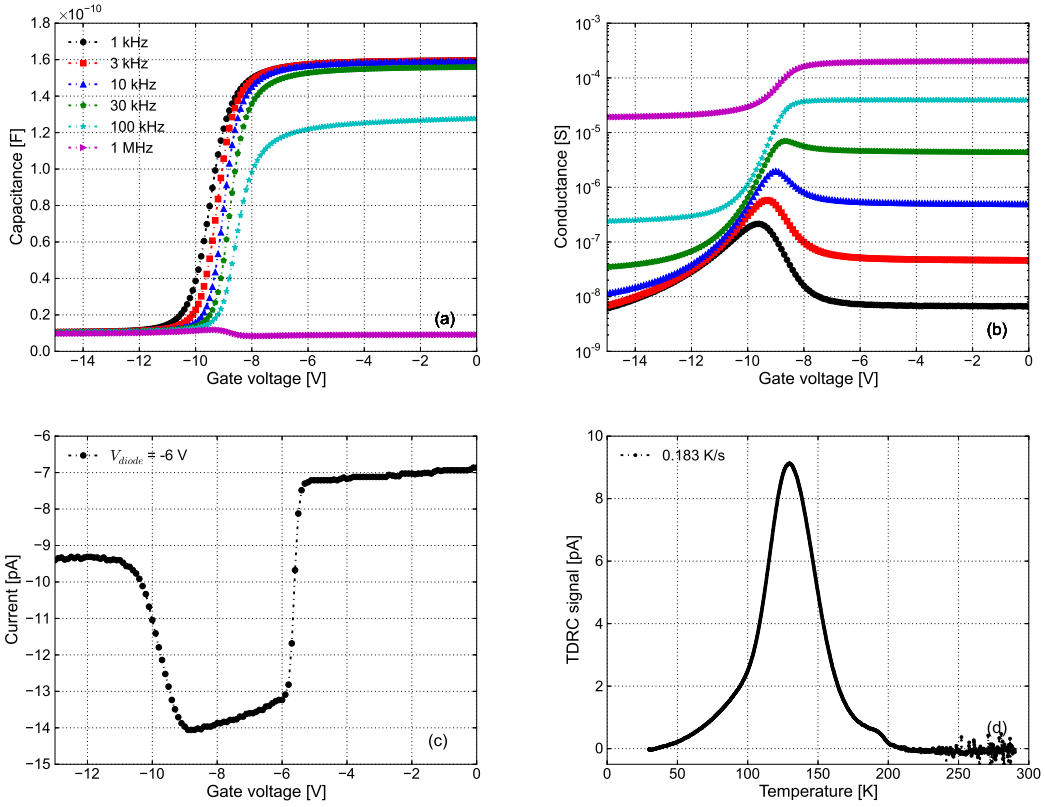

Figure 11.2: Measurements on the non-irradiated test fields: (a) C-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of gate-controlled diode for V_{diode} = -6 V. (d) TDRC spectrum of MOS capacitor. The large TDRC signal at $\sim$ 135 K is supposed to be caused by an additional oxygen-enrichment process for the test field. Results for CB0416 are shown.

on the gate-controlled diodes in the voltage range from 0 V to -100 V. For the TDRC measurement, the gate voltage applied to the MOS capacitors was 0 V (accumulation) during cooling down; during heating up, the gate voltage at which the C-V curves of 1 kHz and 10 kHz merge at room temperature was applied. The heating rate β of the TDRC measurement was 0.183 K/s. After each TDRC measurement, a C/G-V measurement was performed again to check its reproducibility compared to the curves before the TDRC measurement.

The "accumulated" annealing time shown in the following figures are 10, 20, 30, 60, 120, 240 and 480 minutes.

11.3.1. C/G-V curves of MOS capacitors

Figure 11.3(a)-(d) shows the C/G-V curves for different annealing times, which were measured at 80 °C and 60 °C on the MOS capacitors of the test fields, CB0416 and CB0423, after irradiation to 5 MGy. Only curves of 1 kHz and 10 kHz are shown.

Compared to the C/G-V curves before irradiation, the X-ray radiation causes an obvious shift in gate voltage from an initial value of $\sim$ -10 V to a value of at least -65 V. Increases of the peak values of the conductance compared to the ones before irradiation indicate an increase of the density of interface traps introduced by X-ray irradiation.

With annealing, the C/G-V curves shift towards lower voltages (absolute value). However, differences in frequency shift of the C/G-V curves and in the peak value of the conductance are hardly seen, which indicates a slow process for annealing of part of the interface traps.

From figure 11.3(a) and (b), it is observed that the shift of C/G-V curves with annealing at 80 °C is faster than that at 60 °C. The reason is that the annealing of N_{ox} at 80 °C is faster than that at 60 °C.

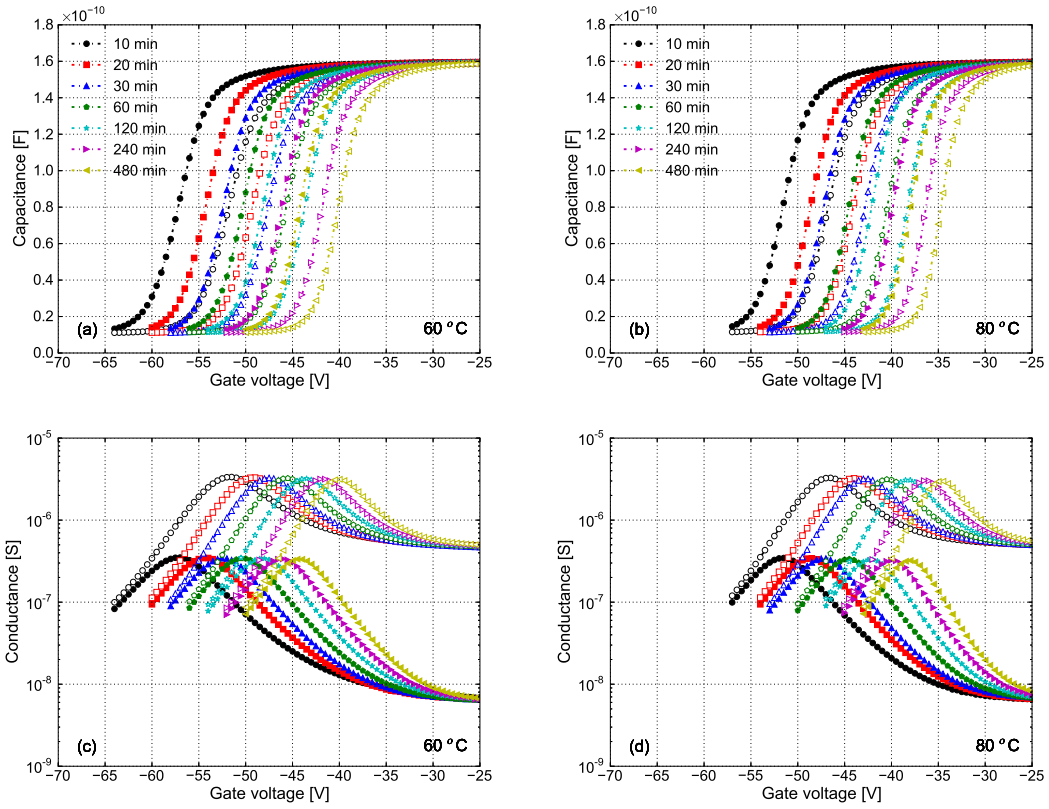

Figure 11.3: Measurements on the MOS capacitors irradiated to 5 MGy. (a) C-V curves of the MOS capacitor as function of annealing time at 60 °C. (b) C-V curves of the MOS capacitor as function of annealing time at 80 °C. (c) G-V curves of the MOS capacitor as function of annealing time at 60 °C. (d) G-V curves of the MOS capacitor as function of annealing time at 60 °C. Frequencies of 1 and 10 kHz are shown: Filled symbols - 1 kHz; open symbols - 10 kHz.

11.3.2. TDRC spectra of MOS capacitors

The TDRC spectra as function of annealing time are shown in figure 11.4. The initial $I_{tdrc}(T)$ before irradiation is added to the TDRC signal due to interface traps introduced by X-ray irradiation, which results in a different shape of the TDRC spectra compared to the ones obtained from <100> silicon.

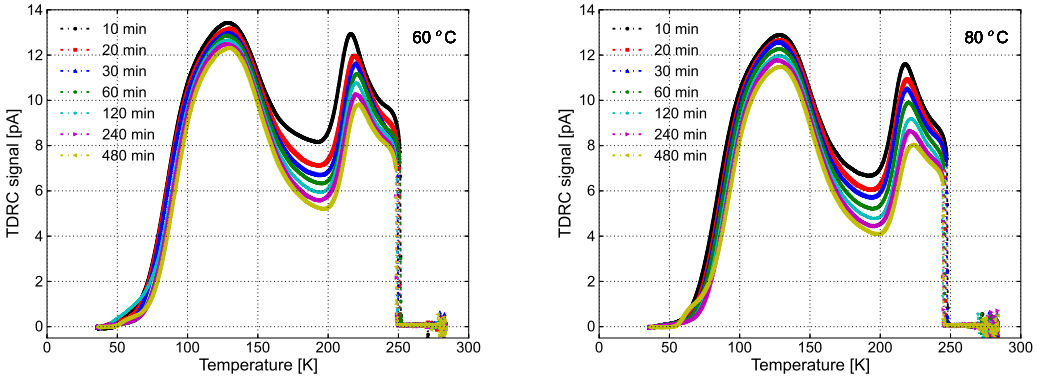

Figure 11.4: Measurements on the MOS capacitors irradiated to 5 MGy. Left: TDRC spectra of the MOS capacitor as function of annealing time at 60 °C . Right: TDRC spectra of the MOS capacitor as function of annealing time at 80 °C.

It is found, from the TDRC spectra in figure 11.4, that the annealing of interface traps at $T \simeq 195$ K and $T \simeq 225$ K is faster than that at $T \simeq 135$ K: for example, the TDRC signals at $T \simeq 195$ K and $T \simeq 225$ K are reduced by $\sim 37\%$ and $\sim 31\%$ after annealing at 80 °C for 8 hours; however the TDRC signal at $T \simeq 135$ K is just reduced by less than 12%. As the interface traps at $T \simeq 135$ K are mainly responsible for the frequency shift of C/G-V curves and the peak values of the conductance, this confirms the observation from the C/G-V curves: The changes of the frequency shift of the C/G-V curves and of the peak values of the conductance with annealing time are hardly seen.

A comparison of the TDRC spectra of the MOS capacitors annealed at 80 °C with the spectra at 60 °C shows, as expected, the annealing of the TDRC signals is faster at a higher temperature.

11.3.3. I-V curves of gate-controlled diodes

The I-V curves from the gate-controlled diodes as function of annealing time at 80 °C and 60 °C are shown in figure 11.5. The annealing of the surface current I_{surf} is fast: For example, I_{surf} is reduced by 50% after annealing for 8 hours at 60 °C and for 4 hours at 80 °C. This implies a fast annealing of the surface-current density J_{surf} at room temperature and the interface traps, which contribute to the TDRC signals at $T \simeq 195$ K and $T \simeq 225$ K, are the possible cause of the surface current. In addition, as the two interface traps are located close to the mid-gap of silicon, this makes them the best candidates responsible for the surface current.

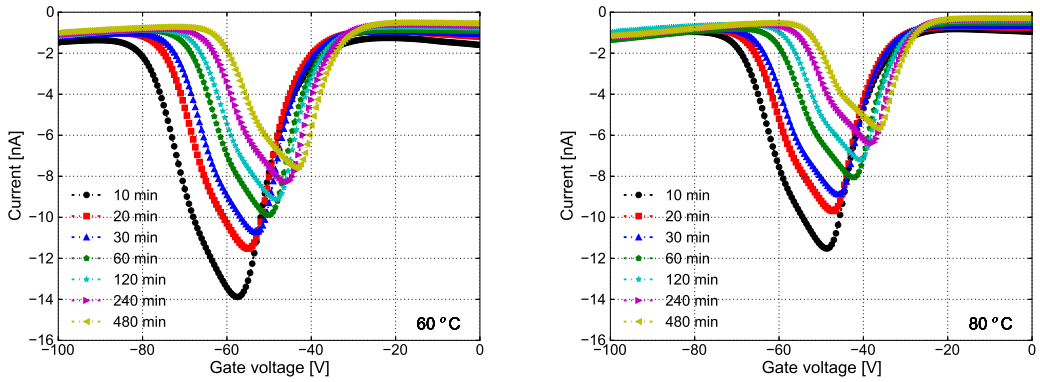

Figure 11.5: Measurements on the gate-controlled diodes irradiated to 5 MGy. Left: I-V curves of the gate-controlled diode annealed at 60 °C . Right: I-V curves of the gate-controlled diode annealed at 80 °C.

11.4. Results: N_{ox} and J_{surf} vs. annealing

The extraction of the oxide-charge density N_{ox} and surface-current density J_{surf} has been discussed in chapter 8; hence, it is shortly summarized as follows: To extract N_{ox}, the measured TDRC spectra are fitted by three Gaussian functions for the three interface traps ($N_{it}^{1,2,3}$). Then the TDRC signals for each trap and their capture cross sections ($\sigma^{1,2,3} = 1.2 \times 10^{-15}$, 5.0×10^{-17} and 1.0×10^{-15} cm^2, refer to table 8.1) are used in the model for MOS capacitors, which is described in chapter 6. And the value of N_{ox} is adjusted till the calculated C/G-V curves describe the measured ones. The surface current I_{surf} determined from irradiated gate-controlled diode is extracted from the "maximum" current measured in depletion and the average value of the currents obtained in accumulation. Finally, J_{surf} is calculated by dividing I_{surf} by the gate area of the 1st gate ring.

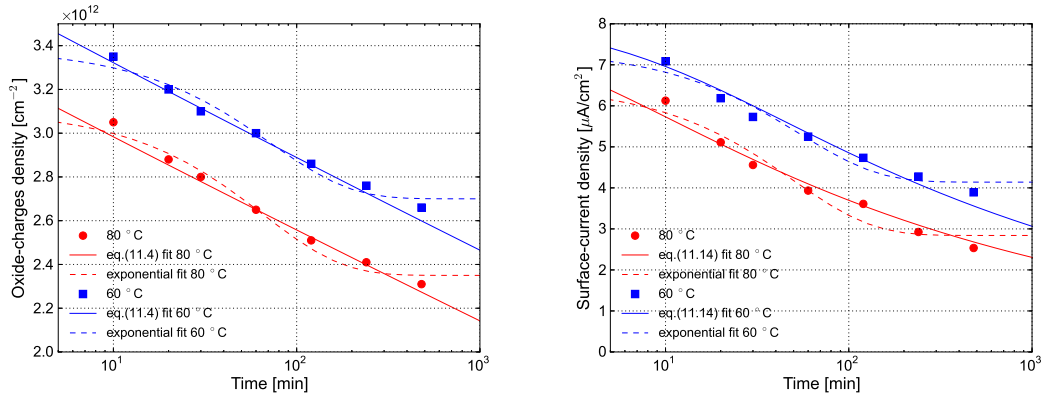

Figure 11.6: Left: Annealing of the oxide-charge density N_{ox} at 60 °C and 80 °C. Right: Annealing of the surface-current density J_{surf} at 60 °C and 80 °C.

Figure 11.6 shows the results of N_{ox} and J_{surf} as function of annealing time at 60 °C

and 80 °C. The measurements are fitted by the functions given in eq.(11.4) and (11.14) and an exponential function. The latter is expected for an annealing with a constant annealing probability. To fit the experimental data at both temperatures with the same function and parameters, a "global fit" procedure is used: For N_{ox}, eq.(11.4) with the same values of N_{ox}^0 and $\lambda/2\beta$ but different values of t_0 are used for 60 °C and 80 °C; for J_{surf}, eq.(11.14) with the same J_{surf}^0 and η but different t_1 is used for both temperatures. It is seen that eq.(11.4) and (11.14) provide a good description of the data supporting the modified "tunnelling model" and the "two reaction model".

N_{ox}^0 [cm^{-2}]	$\frac{\lambda}{2\beta}$	t_0^* [s]	ΔE [eV]
3.6×10^{12}	0.070	5.4×10^{-12}	0.91

Table 11.2: Parameters for the annealing of N_{ox} by the function given in eq.(11.4) described by the modified "tunnelling model".

J_{surf}^0 [μA/cm^2]	η	t_1^* [s]	E_α [eV]
8.1	0.21	1.4×10^{-8}	0.70

Table 11.3: Parameters for the annealing of J_{surf} by the function given in eq.(11.14) described by the "two reaction model".

Tables 11.2 and 11.3 show the parameters found from the fits for N_{ox} and J_{surf}. The oxide-charge density at $t = 0$, N_{ox}^0, and the surface-current density at $t = 0$, J_{surf}^0, are 3.6×10^{12} cm^{-2} and 8.1 μA/cm^2, respectively. The initial values of N_{ox} and J_{surf} obtained from the fits are compatible with the ones from measurements on test fields within one hour after irradiation to 5 MGy, as seen in the figure of the dose dependence of oxide-charge density and surface-current density annealing for 0 minutes at 80 °C. The extracted value of ΔE is 0.91 eV. Given the fact that the energy difference of valence bands of silicon and SiO_2 is $\sim$ 4.7 eV [76] (assuming the band bending during annealing is negligible compared to this value) and the energy difference between the quasi Fermi level of the n-bulk silicon and the valence band of silicon is 0.69 eV for a doping of 1.2×10^{12} cm^{-3}, the energy level of the hole traps in the oxide with respect to the valence band of SiO_2 is $\sim$ 6.3 eV. The value obtained is consistent with existing data in the literature [72, 76].

Using the parameters given in table 11.2 and 11.3 and the functions given in eq.(11.4,11.5) and (11.13,11.14) allows to calculate the annealing of N_{ox} and J_{surf} at other temperatures. Figure 11.7 shows the annealing of N_{ox} and J_{surf} extrapolated to other temperatures and to annealing times as long as 3 years according to the extracted values. It is found that the annealing of N_{ox} is a slow process whereas the annealing of J_{surf} is relatively fast. For example, it takes three years to remove 50% of the oxide charges at 20 °C but only 5 days to reduce the surface current by 50%. But one should bear in mind that the results extrapolated to 20 °C from the measurements at 60 °C and 80 °C contain large uncertainties.

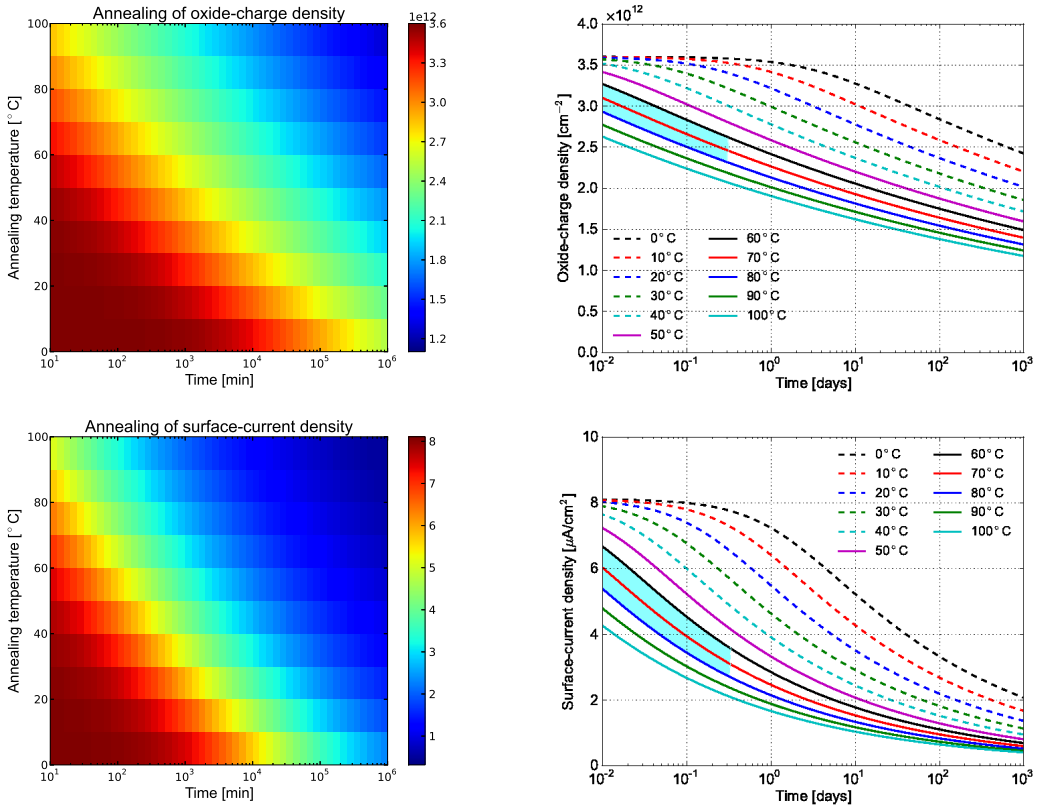

Figure 11.7: Top: Annealing of N_{ox} extrapolated to other temperatures. Bottom: Annealing of J_{surf} extrapolated to other temperatures. The region of measurement data is indicated in cyan.

11.5. Summary

Annealing studies have been performed at 60 °C and 80 °C on MOS capacitors and gate-controlled diodes irradiated to 5 MGy. The annealing kinetics of oxide charges, interface traps and surface currents are discussed. Functions for $N_{ox}(t)$ and $J_{surf}(t)$ given by the modified "tunnelling model" and the "two reaction model" are used to fit the measurements and the values of the parameters in the formulae are determined. The results allow to calculate the values of N_{ox} and J_{surf} at other temperatures and times. It is found that the annealing of N_{ox} is a slow process at room temperature, whereas the annealing of J_{surf} is relatively fast compared to N_{ox}.

The information delivered from the annealing studies for silicon sensors at the XFEL is that: The leakage current in the sensor reduces with time if the detector is not being irradiated; however, some critical issues for sensors, for example the breakdown voltage which is strongly influenced by the oxide-charge density [77,78], are not able to be recovered with time. Nevertheless, the electrical properties of silicon sensors after irradiation are stable and no significant changes are expected due to annealing.

12. Characterization of electrical properties of p^+n microstrip sensors

Radiation-induced defects in the SiO_2 and at the Si-SiO_2 interface change the performance and electrical properties of segmented p^+n sensors. For example,

- formation of an electron-accumulation layer below the interface between strips
- increase of leakage current due to interface traps
- reduction of breakdown voltage
- increase of interpixel/interstrip capacitance
- increase of full depletion voltage
- charge losses close to the Si-SiO_2 interface

In order to understand the influence of surface-radiation damage on the AGIPD sensors, p^+n microstrip sensors have been irradiated to doses up to 100 MGy with 12 keV X-rays at the beamline F4 of DESY DORIS III. The electrical properties of the microstrip sensors as function of X-ray dose and with different bias conditions during irradiation have been characterized. The breakdown behaviour of the segmented p^+n sensor has been simulated by J. Schwandt with damage-related parameters extracted from MOS capacitors and gate-controlled diodes as discussed in a previous chapter and documented in [77]. The investigation of the phenomenon of charge losses in silicon sensors is a topic of the PhD thesis of T. Poehlsen, and first results have been published in [79–81]. Therefore, results, except for the two topics related to sensor breakdown and charge losses, are presented in this chapter.

12.1. Investigated sensors

Figure 12.1 shows the top view and cross section of the microstrip sensor under investigation. The sensors in this study were fabricated by CiS on an n-doped silicon substrate with a thickness of 280 $\pm$ 10 μm and with the orientation <100>. The AC coupling between the p^+ implants and the aluminium strips is made of 200 nm SiO_2 and 50 nm Si_3N_4. In between the aluminium strips, the silicon is covered by 300 nm SiO_2 and 50 nm Si_3N_4. The gap between neighbouring implants is 62 μm, the pitch 80 μm and the length of the 98 strips of each sensor 7.9 mm. The metal overhang on top of the insulating layer is -2 μm. The negative sign means that the width of the metal layer is smaller than the width of the p^+ implant. All implanted strips are connected to a bias ring through bias resistors, which are made by low dose p^+ implants. The bias ring, the current-collection ring (CCR), namely the innermost ring close to the bias ring, and 13 guard rings surround all strips and define the active

detection area of the sensor, which approximately equals to the area of overall strips inside the bias ring. The entire sensor, except for the AC pads[1], DC pads[2], bias ring and current-collection ring, is covered by a layer of final passivation consisting of silicon-dioxide and silicon-nitride.

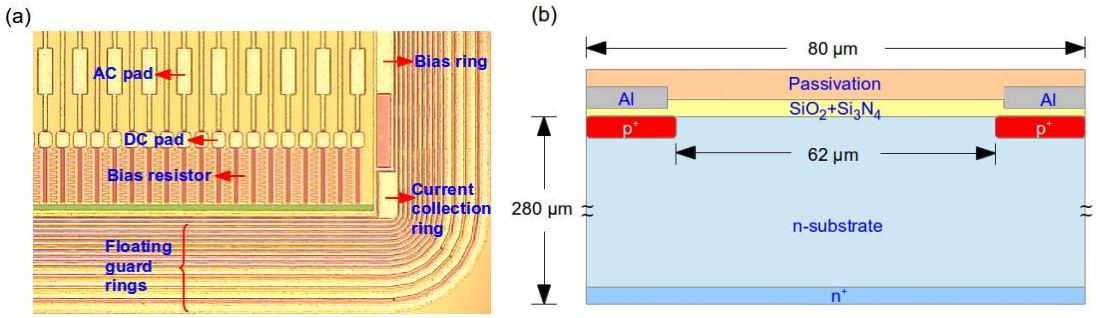

Figure 12.1: The AC coupled p^+n microstrip sensor fabricated by CiS: (a) Top view of one corner of the sensor. (b) Cross section of one pitch of the sensor.

Table 12.1 is a list of the CiS microstrip sensors used and their effective doping concentrations N_{eff}. N_{eff} is determined from the C-V curve of a close-by pad diode on the same wafer.

Label of sensor	CF0551	CF0817	CF0632	CF0636
N_{eff} [cm^{-3}]	8.1×10^{11}	8.5×10^{11}	4.7×10^{11}	5.6×10^{11}

Table 12.1: Properties of the CiS microstrip sensors used in this study.

The CiS microstrip sensors are mounted onto ceramic substrates for the convenience of irradiation and measurements as discussed in chapter 7. For the study of the dose dependence of the electrical properties of the microstrip sensor, CF0551 and CF0817 were irradiated step-by-step to X-ray doses of 1 MGy, 10 MGy and 100 MGy, and no bias voltage was applied to the sensors during irradiation. For the study of the bias-voltage dependence, CF0632 and CF0636 were irradiated to 1 MGy without and with a bias voltage of 35 V applied during irradiation, respectively.

12.2. Change of electrical properties of microstrip sensors with irradiation

The electrical properties of the microstrip sensors were measured in a probe station at room temperature before and after X-ray irradiation. The sensors under test were exposed to a normal laboratory atmosphere (air) with relative humidity (RH) in the range [35%, 50%]. In order to obtain reproducible results, the microstrip sensors were

[1] AC pads refer to those contact pads on top of the insulator for reading out signals from the aluminium strips.
[2] DC pads refer to the contact pads which are connected with the p^+ implants of strips.

annealed at 80 °C for 60 minutes after irradiation. A number of measurements were performed to investigate the following parameters:

- bias resistance - R_{bias}
- full depletion voltage - V_{dep}
- leakage current - $I_{leakage}$
- interstrip capacitance - C_{int}
- interstrip resistance - R_{int}
- coupling capacitance - C_c

12.2.1. Bias resistance

The connection between the impants of p^+ strips and bias ring is accomplished with bias resistors. The bias resistors of the CiS microstrip sensor were produced by ion implantation and drive-in processes.

Figure 12.2(a) shows the profiles of boron concentration after ion implantation and drive-in separately. A depth of the boron profile of $\sim$ 430 nm is obtained. The process of ion implantation is simulated with the Stopping and Range of Ions in Matter (SRIM) [82] program. 92% of the boron ions are deposited in silicon. Based on the result of the SRIM simulation, the profile of boron concentration is calculated by solving the diffusion equation considering a constant diffusivity,

$$\frac{\partial n_B(x,t)}{\partial t} = D_B \frac{\partial^2 n_B(x,t)}{\partial x^2} \tag{12.1}$$

with $n_B(x,t)$ being the position x (relative to the Si-SiO_2 interface) and time t dependent concentration of boron ions. D_B is the diffusion coefficient of boron in silicon: $D_B = D_{B0} \cdot \exp(-\frac{E_a}{k_0 T})$, with the diffusion coefficient $D_{B0} = 0.76$ cm^2/s and the activation energy $E_a = 3.46$ eV [6]. It is assumed that no diffusion flux into/out of the silicon surface so that the total number of boron ions in silicon is conserved; therefore, the boundary condition $\frac{\partial n_B}{\partial x}|_{x=0} = 0$ is used to solve the above partial differential equation (12.1). Hence, the sheet resistance of the bias resistor, $R_\square$, is obtained

$$R_\square = \frac{1}{q_0 \mu_h \int n_B(x) dx} = 0.85\ k\Omega/\square \tag{12.2}$$

To experimentally determine the bias resistance, the current through one of the bias resistors is measured by a Keithley 6485 pico-ammeter as a function of voltage, supplied by a Keithley 6517A electrometer, across the bias resistor. During the measurement, a bias voltage of 100 V is applied to the sensor to fully deplete the sensor. Figure 12.3 shows the measurement scheme on the bias resistor of the AC coupled microstrip sensor. As shown in figure 12.2, the bias resistance R_{bias}, derived from the slope of the I-V measurement between one of the DC pads and the bias ring, before irradiation, and after irradiation to 1 and 10 MGy are 0.5, 0.6 and 1.0 MΩ. After irradiation to 100 MGy, the bias resistance exceeds 100 MΩ. The failure of the bias resistor

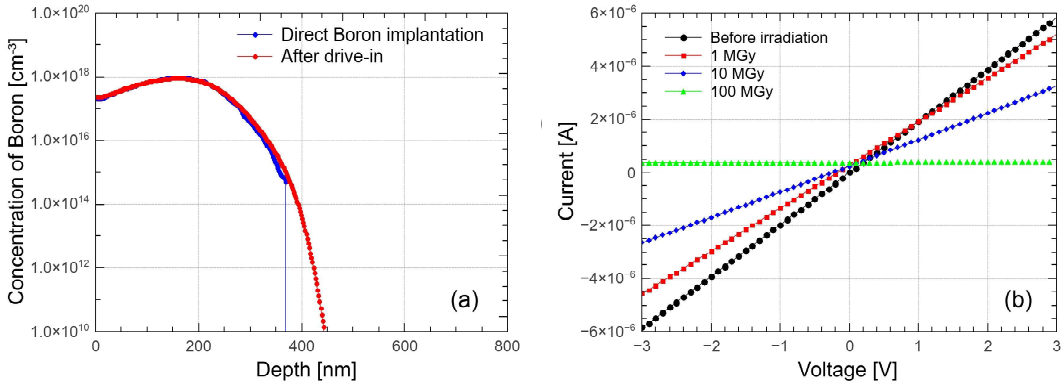

Figure 12.2: (a) Distribution of boron concentration close to the interface. Blue line: Simulation result of SRIM directly after boron implantation; Red line: Calculated profile after drive-in process based on the simulation result. (b) I-V measurements on the bias resistor of the microstrip sensor.

can be explained by the removal of free holes in the low dose p^+ implants due to the positive oxide and interface charges, which causes a pinch-off of the implanted bias resistor resulting in a depleted region. Therefore, in the following only the results obtained for dose values of 0, 1 and 10 MGy will be presented.

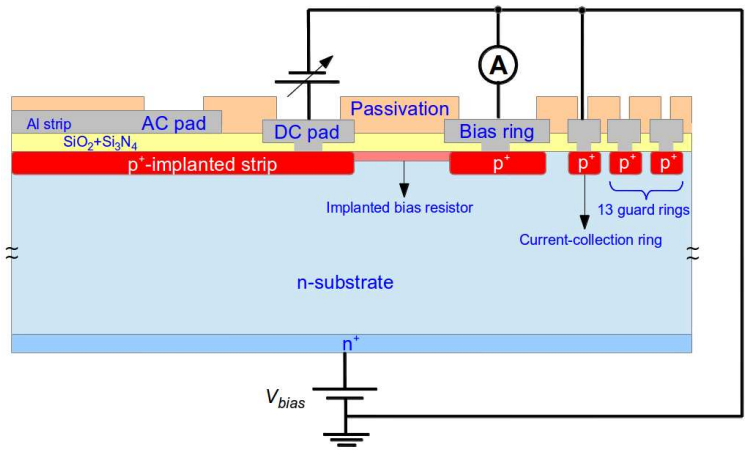

Figure 12.3: Measurement scheme on the bias resistor of the AC coupled microstrip sensor.

12.2.2. Full depletion voltage

To determine the full depletion voltage, the capacitance of the entire sensor has been measured as function of bias voltage. For this measurement, a DC power supply Keithley 6517A was connected to the rear side of the sensor through a 1 kΩ resistor; the high frequency terminal of the Agilent 4980A LCR meter was connected to the rear side of the sensor through a capacitor of 1 μF and the AC current from the

bias ring of the sensor fed back to the input terminal of the LCR meter. The current-collection ring was grounded through a Keithley 6485 pico-ammeter and the guard rings were kept floating during the measurement. During the capacitance measurement, an AC voltage of 0.5 V was applied. The measurement scheme for the full depletion voltage is shown in figure 12.4.

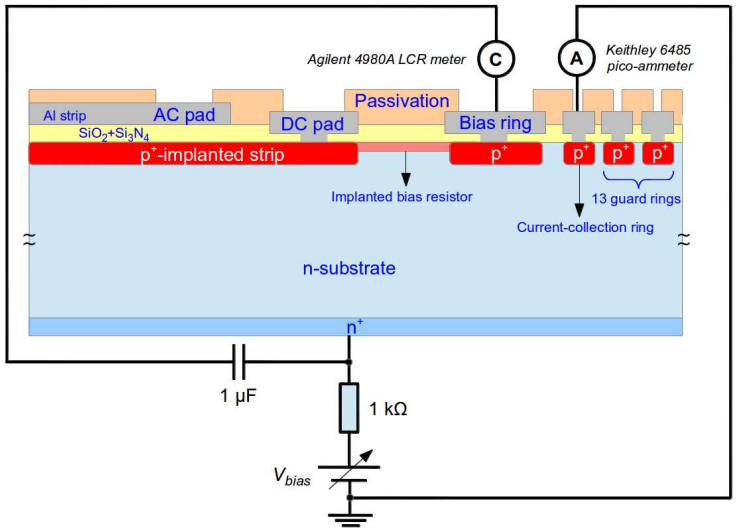

Figure 12.4: Measurement scheme for the full depletion voltage of the AC coupled microstrip sensor.

Figure 12.5(a) shows the capacitance of the entire sensor measured in series mode at 100 kHz for doses of 0, 1 and 10 MGy, plotted as $1/C^2$ versus bias voltage. In series mode, no frequency dependence of the sensor capacitance is found for frequencies up to 100 kHz for the non-irradiated sensor. However, if the measurement was performed in parallel mode, a frequency dependence of the sensor capacitance can be seen, which is caused by the resistance of the quasi-neutral region and the bias resistor. It can be seen from figure 12.5(a) that $1/C^2$ increases linearly with bias voltage and saturates at the full depletion voltage V_{dep}. A kink at $\sim$ 6 V, the voltage at which the depletion regions below the individual strips merge (V_{merge}), is observed. The capacitance C_{dep} at the full depletion voltage expected for a pad diode with the same area and thickness of the silicon substrate is 23.3 pF, close to the measured value of 23.6 pF for the microstrip sensors. In addition, the capacitance of a single strip to backplane has also been investigated. The value is consistent with the capacitance of the entire sensor divided by the number of strips.

It is noted that, compared to a pad diode, an additional voltage is needed for microstrip sensors to fully deplete the sensor. The full depletion voltage V_{dep} for a pad diode, calculated from the same effective doping concentration ($N_{eff} = 8.1 \times 10^{11}$ cm^{-3}) and thickness (280 μm), is 48 V (calculated curve shown as green line in figure 12.5); whereas the V_{dep} for the microstrip sensor (before irradiation) is about 60 V. The additional 12 V is required to charge up (deplete) the Si-SiO_2 interface region between p^+ implanted electrodes. After irradiations to 1 MGy and 10 MGy,

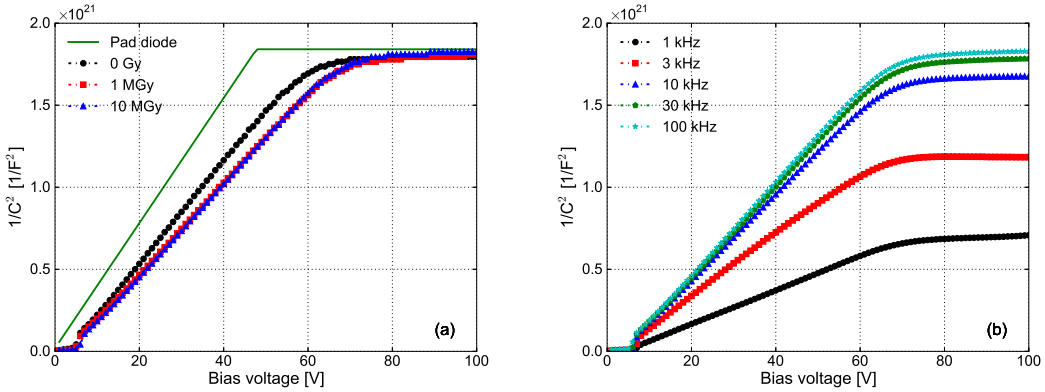

Figure 12.5: (a) $1/C^2$ vs. bias voltage of the microstrip sensor (in series mode) for doses of 0, 1 and 10 MGy and of a pad diode. 100 kHz curves are shown. The curve for a pad diode shown as green line is calculated by the same effective doping concentration, thickness and area as of the microstrip sensor. (b) $1/C^2$ vs. bias voltage (in series mode) for frequencies of 1, 3, 10, 30 and 100 kHz after irradiating the sensor to 10 MGy.

the full depletion voltage V_{dep} increases by another $\sim$ 10 V, which is required to compensate for the radiation-induced positive charges in the oxide and at the Si-SiO_2 interface. The increase of the full depletion voltage, $\triangle V_{dep}$, saturates at high doses. The results have been verified by a TCAD simulation [83], which shows that the full depletion voltage reaches a maximum constant value when the density of positive charges at the interface is above 3.0×10^{11} cm^{-2}. Therefore, it can be concluded that the full depletion voltage of a microstrip sensor, being different from a pad diode, depends on its specific design, i.e. pitch, gap between neighbouring electrodes and effective doping concentration, and the densities of oxide charges and interface traps. In addition, the full depletion voltage of the irradiated sensor also depends on the humidity of the atmosphere during the measurement: The higher the humidity, the more the oxide charges can be compensated by the charges deposited on top of the sensor and thus the lower the full depletion voltage is expected compared to the voltage in a dry atmosphere. It should be noted that the slope of the $1/C^2 - V$ curve and the extracted full depletion voltage of a segmented p^+n sensor cannot be used to determine the effective doping concentration in silicon, as it's also influenced by the density of surface charges.

In addition, the radiation-induced traps at the Si-SiO_2 interface can be charged and discharged by the external AC signal, and thus they act like a frequency dependent capacitor. As seen in figure 12.5(b), the measured capacitance and the slope of $1/C^2$ versus bias voltage from a sensor irradiated to 10 MGy shows a frequency dependence due to the presence of interface traps after irradiation. The effect due to interface traps has been implemented in the model for the MOS capacitor discussed in chapter 6.

Separated curves of the sensor capacitance and resistance versus bias voltage with X-ray doses are presented in appendix B.1.

12.2.3. Leakage current

The leakage current was measured from the bias ring of the microstrip sensor by a Keithley 6517A electrometer. The bias ring and the rear side (n^+-side) of the sensor were connected to the current-input terminal and the voltage-output terminal of the electrometer, repectively. A Keithley 6485 pico-ammeter was used to monitor the current flowing into the current-collection ring. All guard rings were left floating. Figure 12.6 shows the measurement scheme for the leakage current.

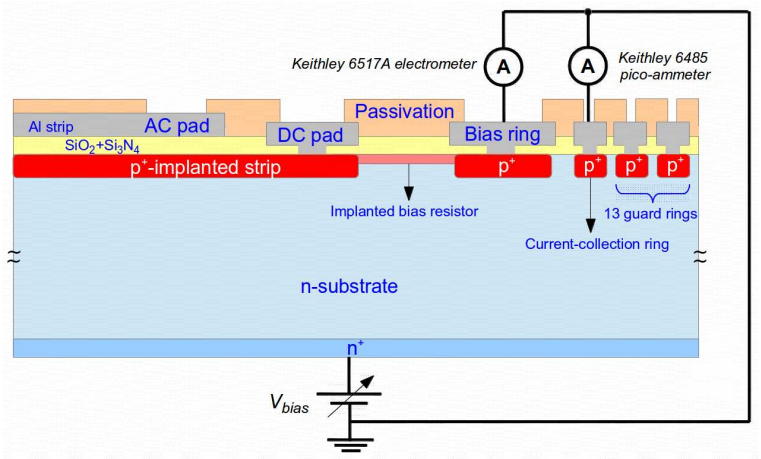

Figure 12.6: Measurement scheme for the leakage current of the AC coupled microstrip sensor.

The results of the measurements are shown in figure 12.7. Two main sources contribute to the leakage current $I_{leakage}$: Bulk generation current, I_{bulk}, and surface generation current, I_{surf}. Hence, the leakage current can be expressed by $I_{leakage} = I_{bulk} + I_{surf}$. For the non-irradiated sensor, the leakage current is dominated by the bulk-generation current due to the defects in the depletion region of silicon; however, for the irradiated sensor, the surface-generation current due to the traps at the Si-SiO_2 interface dominates.

As seen in figure 12.7, the leakage current of the non-irradiated sensor increases with bias voltage and saturates when the sensor is fully depleted (the full depletion voltage $V_{dep} \sim 60$ V). The saturation value of the leakage current scaled to 20 °C is 5.8 nA, which corresponds to a current density of 0.33 $\mu A/cm^3$. Compared to the I-V curve of the non-irradiated sensor, the leakage currents after irradiation to doses of 1 and 10 MGy are two orders of magnitude larger and do not show any saturation with bias voltage even above the full depletion voltage V_{dep}. This observation can be explained as follows: Radiation-induced positive charges induce an electron-accumulation layer below the Si-SiO_2 interface. The electrons in the accumulation layer shield the interface traps: The electric field at the Si-SiO_2 interface in the electron-accumulation layer is much lower than that at the depleted interface region. Only the interface traps located at the depleted interface region are able to contribute to the surface current. Hence, the leakage current for irradiated sensors is mainly due to the surface-generation current I_{surf} from the Si-SiO_2 interface regions

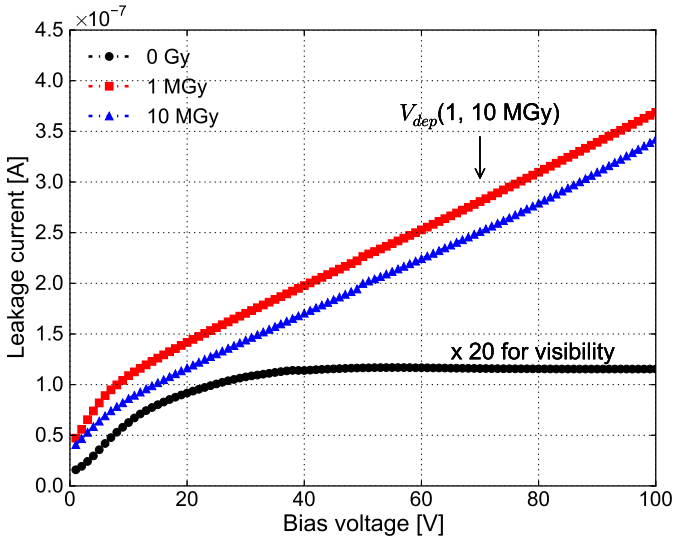

Figure 12.7: Leakage current vs. bias voltage for doses of 0, 1 and 10 MGy.

not covered by an electron-accumulation layer (shown in figure 12.8). The area of the electron-accumulation layer however decrease approximately linearly with bias voltage, which results in an increase of leakage current with bias voltage. This behaviour has been verified by Synopsys TCAD simulation [77]. Hence, it can be concluded that I_{surf} is proportional to the surface-current density, J_{surf}, and the area of the depleted Si-SiO_2 interface, A_{dep}: $I_{surf} = J_{surf} \cdot A_{dep}$.

As the surface-current density has been characterized as function of dose and annealing from gate-controlled diodes. The surface-current densities are expected to be 2.7 $\mu A/cm^2$ and 2.4 $\mu A/cm^2$ (values extrapolated to 60 minutes at 80 °C according to the annealing of the surface-current density described in chapter 11 and the measurement results after annealing) for doses of 1 and 10 MGy after annealing for 60 minutes at 80 °C, respectively. The depleted area of the Si-SiO_2 interface A_{dep}, therefore, can be extracted for doses of 1 and 10 MGy. The width of the depleted Si-SiO_2 interface, W_{dep}, defined as the distance between the p^+ electrode and the electron-accumulation layer, is calculated by using $A_{dep}/2$ divided by the length of the strip and the number of the strips. The values of W_{dep} according to fore-mentioned calculation for a bias voltage of 100 V are 8.9 μm and 9.1 μm for doses of 1 and 10 MGy. As the extraction of the surface-current density from a gate-controlled diode gives the minimal value, the actual values of W_{dep} are even smaller than the calculated values.

12.2.4. Interstrip capacitance

In addition to the leakage current, the interstrip capacitance is one of the main sources contributing to the noise in the read-out signals. Hence, it is necessary to understand the factors that influence the interstrip capacitance. In this study, the interstrip capacitance between neighbouring p^+ implants was measured as function of bias voltage for different frequencies after each X-ray dose.

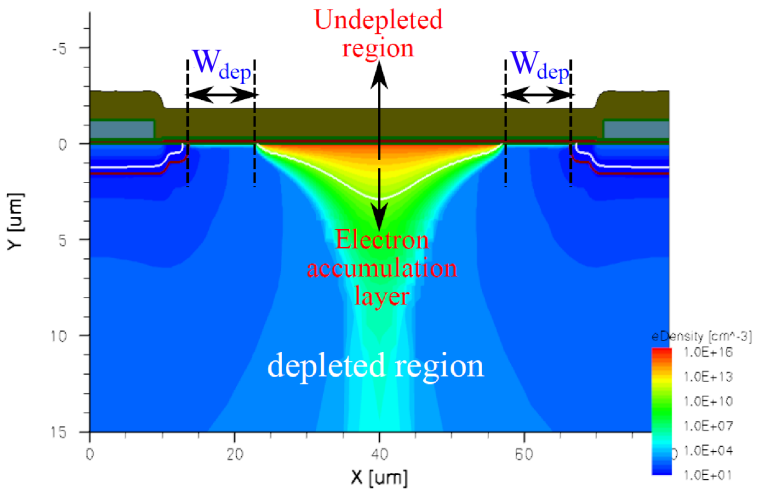

Figure 12.8: The electron-accumulation layer below the Si-SiO_2 interface of the CiS microstrip sensor. The distribution of electron density in the sensor is simulated with an oxide-charge density of 1×10^{11} cm^2 by J. Schwandt.

The interstrip capacitance was measured in such a way: A DC voltage from a Keithley 6517A was applied to the rear side of the sensor, while the bias ring and the current collection ring were grounded; an AC voltage with frequencies of 1 kHz, 2 kHz, ..., up to 2 MHz and with an amplitude of 50 mV from the output terminal of Agilent 4980A LCR meter was connected to one of the DC pads (refer to figure 12.1) and the AC current flowing into its neighbouring DC pad was fed back to the input of the LCR meter (shown in figure 12.9). The capacitance and conductance were measured as function of bias voltage.

Figure 12.10(a) shows the interstrip capacitance (in series mode) as function of bias voltage for doses of 0, 1 and 10 MGy. For the non-irradiated sensor, the interstrip capacitance decreases with bias voltage until the depletion regions below the individual strips merge, in which case the measured capacitance is dominated by the capacitance of a single strip to the backplane; then the interstrip capacitance starts to increase and the value saturates when the depletion region reach the rear side of the sensor. For the doses of 1 and 10 MGy, above V_{merge}, the interstrip capacitance decreases with bias voltage. The decrease of the interstrip capacitance is due to the increase of the depleted area at the Si-SiO_2 interface. Thus, the interstrip capacitance does not saturate at the full depletion voltage, which confirms the behaviour observed for the leakage current. As the depleted area at the Si-SiO_2 interface for 10 MGy is larger than that for 1 MGy for the same bias voltage, as observed in figure 12.10(a), the interstrip capacitance for 10 MGy is lower than the value for 1 MGy. However, the interstrip capacitance for the irradiated sensor is larger than the value for the non-irradiated sensor in the investigated voltage range due to the presence of the electron-accumulation layer after irradiation.

The interstrip capacitance shows a strong frequency dependence, as seen from the results of the sensor irradiated to 10 MGy in figure 12.10(b). At lower frequencies higher interstrip capacitances are obtained. A similar behaviour is also observed for

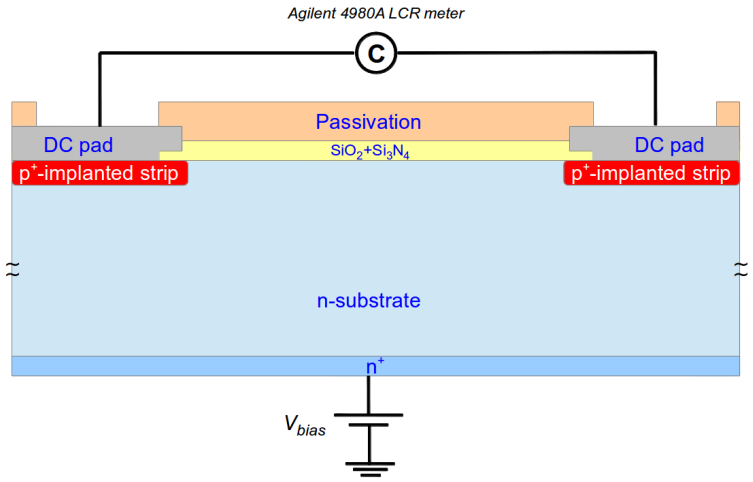

Figure 12.9: Measurement scheme for the interstrip capacitance of the AC coupled microstrip sensor. The bias ring and current-collection ring are not shown in the figure but are grounded.

the non-irradiated sensor. The strong frequency dependence can be explained as follow: The two strips used in the measurement can be described by a distributed RC network consisting of resistors for the segmented p^+ implant along the strip and capacitors between the strips. The RC circuit acts like a filter: For low frequencies, the AC signal passes along the entire strip; for high frequencies, it passes only part of the strip resulting in a reduced capacitance. However, how the interface traps contribute to the RC circuit and how to calculate their contributions is still unclear at present. The RC circuit for the interstrip capacitance has been implemented into a SPICE model aiming for a complete RC network for the microstrip sensor. The SPICE model will be discussed in the following chapter.

In addition, a time dependence of the interstrip capacitance has also been observed: The value of the interstrip capacitance measured at 1 MHz is reduced by $\sim$ 5% after biasing the sensor for 400 minutes in a normal atmosphere. The reduced fraction of the interstrip capacitance is expected to be a function of time and humidity of the measurement environment.

12.2.5. Interstrip resistance

The interstrip resistance is another important parameter to understand a silicon microstrip sensor [84], as it is important for strip isolation which has an impact on the position resolution. The punch-through voltage of the interstrip resistance, especially for DC coupled sensors, should be optimized so that even if one of the strips is not grounded properly due to bonding problems no large current flows into the read-out electronics of its neighbouring strips. The interstrip resistance and punch-through voltage are mainly influenced by the layout of the strip, ionizing-radiation dose (and bias voltage for irradiated sensors).

The measurement scheme for the interstrip resistance is shown in figure 12.11. To

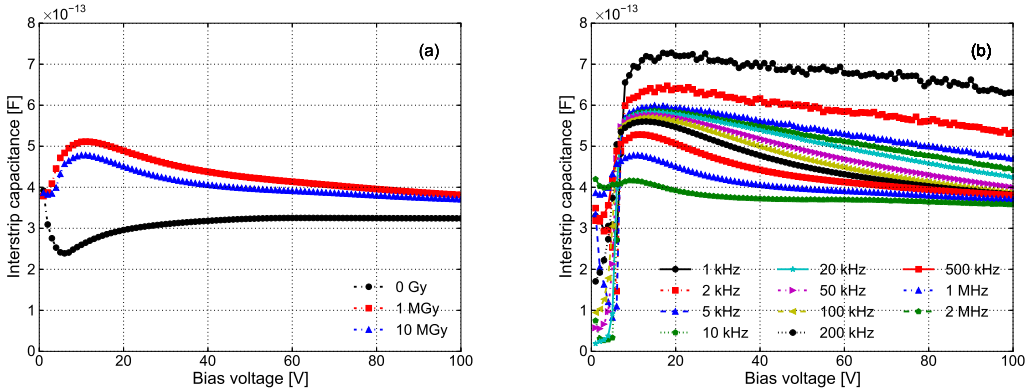

Figure 12.10: (a) Change of the interstrip capacitance (in series mode) with bias voltage and dose. Measurement results with 1 MHz are shown. (b) Interstrip capacitance vs. bias voltage (in series mode) for frequencies of 1 kHz, 2 kHz, ..., up to 2 MHz after irradiation to 10 MGy.

measure the interstrip resistance, a constant DC voltage from a Keithley 6485 was applied to the rear side of the sensor while keeping the bias ring and current-collection ring grounded. The voltage-output terminal of Keithley 6517A multimeter was connected to one of the DC pads of the sensor and the current flowing into one of its neighbouring DC pads was fed back to the current-input terminal of the multimeter. The current between the neighbouring DC pads (interstrip current I_{int}) was measured as function of the voltage difference between the DC pads (interstrip voltage V_{int}).

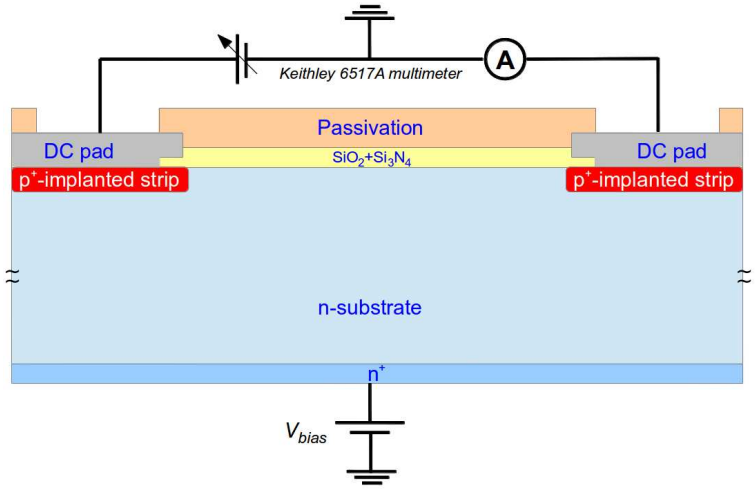

Figure 12.11: Measurement scheme for the interstrip resistance of the AC coupled microstrip sensor. The bias ring and current-collection ring are not shown in the figure but are grounded.

Figure 12.12(a) shows I_{int} vs. V_{int} of the non-irradiated microstrip sensor biased to voltages of 0, 10, ..., 100 V. It is seen that the punch-through voltage, V_{pt}, depends on

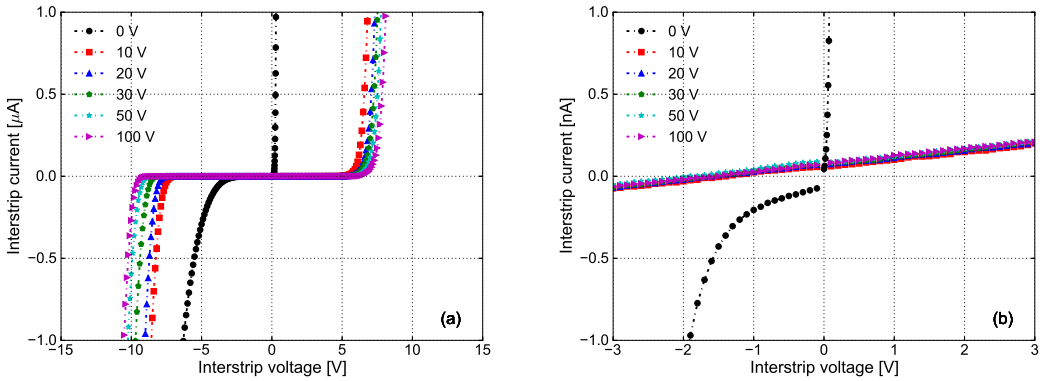

Figure 12.12: (a) Interstrip current vs. interstrip voltage of the non-irradiated microstrip sensor for bias voltages of 0, 10, ..., 100 V. (b) Zoom in of (a) to indicate the interstrip resistance from the slope.

the bias voltage applied to the sensor and the polarity of the interstrip voltage: The higher the bias voltage, the higher the punch-through voltage; the punch-through voltages under negative V_{int} are higher than those under positive V_{int}: $|V_{pt}(V_{int} < 0)| > |V_{pt}(V_{int} > 0)|$. To explain the measured punch-through behaviour, as shown in figure 12.13, the following notations are defined: "A" - the DC pad where the interstrip voltage is applied; "B" - the DC pad from which the interstrip current is measured; "C" - the point in the middle of the gap between the neighbouring p^+ implants; "D" - the rear side of the sensor.

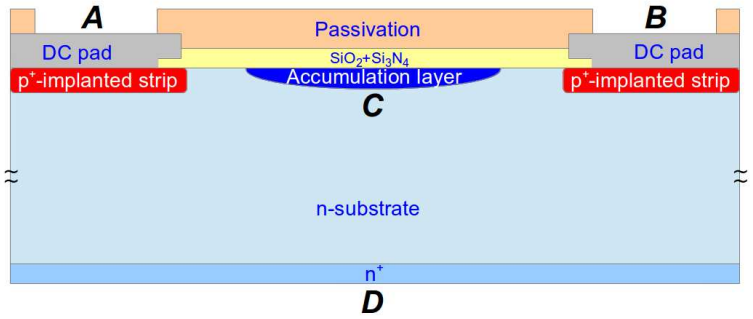

Figure 12.13: Defined notations for the interstrip resistance of the AC coupled microstrip sensor.

For V_{bias} = 0 V (and $V_{bias} < V_{merge}$): For positive V_{int}, the strip layout is equivalent to a bipolar junction transistor (BJT). "A" can be regarded as the emitter of the BJT, "B" the collector and "D" the base. Hence the region below "B" is partially depleted due to the built-in voltage V_{bi} ($\sim$ 0.7 V) even if V_{BD}, the voltage difference between "B" and "D", is zero. The depth of the depletion layer for V_{bias} = 0 V depends on the effective doping concentration and is typically 30 μm for high-ohmic silicon. For V_{int} > 0 V, the voltage difference between "A" and "D", V_{AD}, is a forward voltage for a p^+n junction. In this case, electrons from "D" drift to "A", as well as a large number of holes

from "A" drift into the silicon. The holes which drift into the silicon, can be collected by "B" if they diffuse to the depletion boundary below "B". The current measured from "B", namely I_{int} as defined previously, depends on the number of holes injected into the silicon from "A", and thus sharply increases with the voltage applied to "A", that is V_{int}. Under negative V_{int}, the depletion region below "B" is also due to V_{bi}. However, the region below "A" starts to deplete and the depletion layer expands with decreasing V_{int}, which causes an increase in the reverse bias voltage between "A" and "D". Hence, no punch through is observed at low V_{int}. The potential at the depleted Si-SiO_2 interface close to "A" is in-between the potential of "A", ϕ_A, and the potential of "D", ϕ_D. When the depletion regions below "A" and "B" merge, the potential of "C" at the depleted Si-SiO_2 interface, ϕ_C, is larger than ϕ_A but smaller than ϕ_B: $\phi_A < \phi_C < \phi_B$. In this case, the carriers flow from one electrode to its neighbouring electrode. Hence, a punch through is observed for $V_{int} < 0$ V. According to this analysis, it can be concluded that the condition for punch through is that either $\phi_A < \phi_C < \phi_B$ or $\phi_A > \phi_C > \phi_B$.

For V_{bias} = 10, 20,..., 100 V (and $V_{bias} > V_{merge}$), the Si-SiO_2 interface between p^+ implants is depleted if no oxide charges are present in the SiO_2. If "A" and "B" are at the same potential, the potential at the middle of the gap, ϕ_C, depends on the bias voltage applied. It is several volts according to TCAD simulations [3]. Hence, the potentials at "A", "B" and "C" along the interface satisfy $\phi_A < \phi_C > \phi_B$. The electric field along the interface points from "C" to "A" and "B" so that no carriers drift from "A" to "B" or from "B" to "A". Under positive V_{int}, ϕ_A increases with V_{int}; thus, the potential at "C", ϕ_C, increases with V_{int}. However, as the potential difference between "A" and "D" decreases with increasing V_{int}, the electric field at the interface region between "A" and "C", E_{AC} ($E_{AC} > 0$ for field points from "C" to "A"; $E_{AC} < 0$ for field points from "A" to "C"), decreases. When $E_{AC} < 0$, the condition $\phi_A > \phi_C > \phi_B$ is reached. Thus, the holes drift from "A" to "C" and further to "B" and a punch through is observed. Whereas under negative V_{int}, ϕ_A decreases with V_{int}. In this case, ϕ_A is always smaller than ϕ_C; however, the potential at "C", ϕ_C decreases with V_{int}. Hence, the electric field at the interface region between "C" and "B", E_{BC}($E_{BC} > 0$ for field points from "C" to "B"; $E_{BC} < 0$ for field points from "B" to "C"), decreases. When $E_{BC} < 0$, the condition $\phi_A < \phi_C < \phi_B$ is satisfied and thus a punch through is seen for negative V_{int}. With increasing bias voltage, ϕ_C increases; therefore, a higher voltage V_{int} is required to punch through either the region between "A" and "C" (for $V_{int} > 0$ V) or the region between "B" and "C" (for $V_{int} < 0$ V). The asymmetry of the punch-through voltages for $V_{int} > 0$ V and $V_{int} < 0$ V is due to the fact that the decrease of E_{AC} is faster than that of E_{BC}. Hence, the punch-through voltages, V_{pt}, for $V_{int} > 0$ V is smaller than the values for $V_{int} < 0$ V at the same bias voltage. The values of V_{pt} of the non-irradiated sensor for different bias voltages V_{bias} are given in table 12.2. The punch-through voltage V_{pt} in this text is defined as a voltage where the interstrip current equals to 100 nA.

Figure 12.12(b) is a zoom of figure 12.12(a) in the voltage range from -3 V to 3 V. The interstrip current I_{int} at $V_{int} = 0$ is given by the leakage current of a single strip, $I_{int}(V_{int}) \simeq 60$ pA. The interstrip resistance, R_{int}, is derived from the slope of the I_{int}

[3] ϕ_C is a strong function of the oxide-charge density.

V_{bias} [V]	0	10	20	30	50	100
V_{pt} ($V_{int} > 0$ V) [V]	0.2	6.2	6.6	6.8	7.0	7.4
V_{pt} ($V_{int} < 0$ V) [V]	-4.2	-7.8	-8.3	-8.9	-9.4	-9.8

Table 12.2: The punch-through voltages V_{pt} of the non-irradiated sensor under bias voltages of 0, 10, 20, 30, 50 and 100 V.

vs. V_{int} curves: $R_{int} = \mathrm{d}V_{int}/\mathrm{d}I_{int} = 22.1 \pm 0.1$ GΩ.

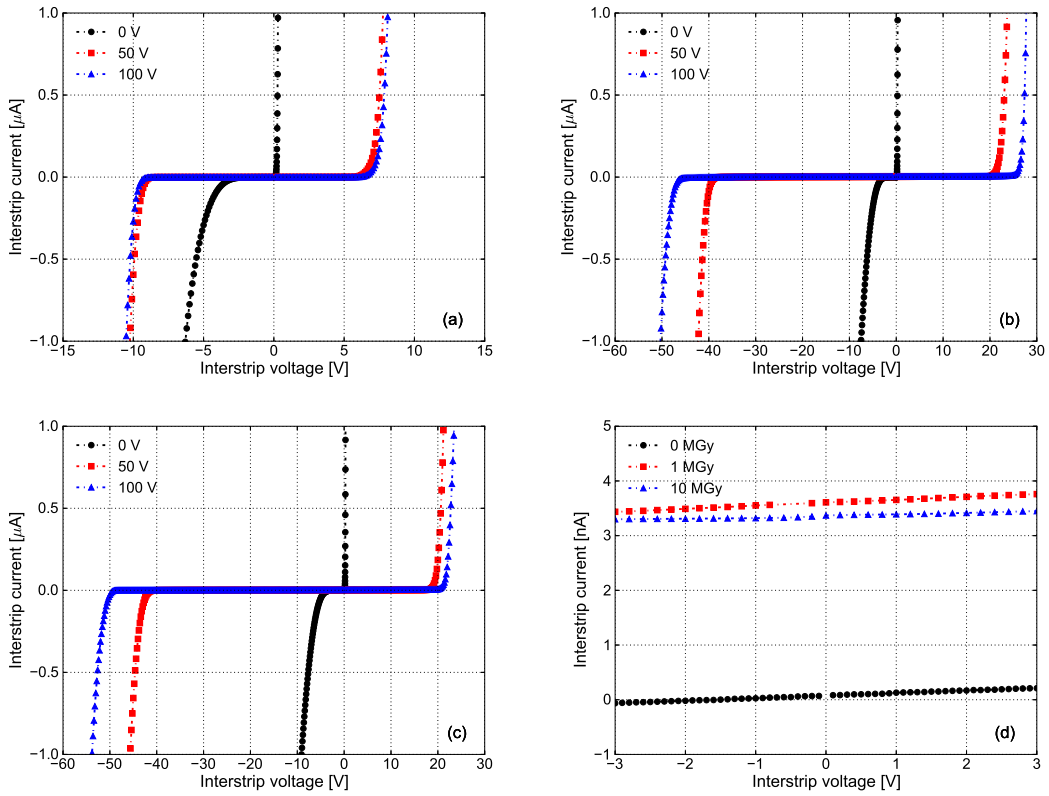

Figure 12.14: Interstrip current vs. interstrip voltage of the microstrip sensor under bias voltages of 0, 50 and 100 V for doses of 0 (a), 1 (b) and 10 MGy (c). (d) Interstrip current vs. interstrip voltage of the microstrip sensor under bias voltage of 100 V for different doses: slopes indicate the values of interstrip resistance.

The I_{int} vs. V_{int} curves were also characterized for doses up to 10 MGy, as seen in figure 12.14(a)-(c). It is observed that, after X-ray irradiations, the punch-through voltages increase compared to the ones obtained from the non-irradiated sensor. Table 12.3 is a list of the values of V_{pt} for doses of 0, 1 and 10 MGy under bias voltages of 0, 50 and 100 V.

The punch-through voltages V_{pt} in the table 12.3 show a significant increase for doses of 1 and 10 MGy compared to 0 MGy. The reason is that the radiation-induced oxide charges and positively charged interface traps produce a high electric field close

V_{bias} [V]	0	50	100
V_{pt} (V_{int} > 0 V) [V] for 0 MGy	0.2	7.0	7.4
V_{pt} (V_{int} < 0 V) [V] for 0 MGy	-4.2	-9.4	-9.8
V_{pt} (V_{int} > 0 V) [V] for 1 MGy	0.2	22.0	26.6
V_{pt} (V_{int} < 0 V) [V] for 1 MGy	-4.5	-40.2	-47.6
V_{pt} (V_{int} > 0 V) [V] for 10 MGy	0.2	19.8	22.0
V_{pt} (V_{int} < 0 V) [V] for 10 MGy	-5.7	-43.2	-51.0

Table 12.3: The punch-through voltages V_{pt} of the sensor irradiated to 0, 1 and 10 MGy under bias voltages of 0, 50 and 100 V.

to the p^+ electrode so that the electric field between "A" and "C" ("B") is enhanced and the potential at "C" for a fixed bias voltage is increased. Hence, to reduce the high field of E_{AC} for $V_{int} > 0$ or E_{BC} for $V_{int} < 0$ to zero and furthermore change the direction of the field, a higher voltage is needed compared to the case for the non-irradiated sensor.

Figure 12.14(d) shows the I_{int} vs. V_{int} curves for doses of 0, 1 and 10 MGy at V_{bias} = 100 V in the voltage range $V_{int} \in$ [-3.0 V, 3.0 V]. I_{int} at V_{int} = 0 V are due to the leakage current. In table 12.4, the interstrip resistance, $R_{int} = \mathrm{d}V_{int}/\mathrm{d}I_{int}$, is shown for different doses.

Dose [MGy]	0	1	10
R_{int} [GΩ]	22.1 ± 0.1	18.3 ± 0.1	36.3 ± 1.3

Table 12.4: R_{int} of the sensor irradiated to 0, 1 and 10 MGy, as determined from the voltage range $V_{int} \in$ [-3.0 V, 3.0 V].

Compared to the value of R_{int} for 0 MGy of 22.1 GΩ, R_{int} decreases to 18.3 GΩ after irradiation to 1 MGy and then increases by a factor of 2 after 10 MGy. This can be regarded as a result of the redistribution (different distributions) of the electric field at and below the Si-SiO_2 interface in the gap region.

12.2.6. Coupling capacitance

The AC coupling is used to prevent the leakage current to flow into the amplifier in the read-out electronics. The coupling capacitance C_c in an AC coupled sensor is in series with the sum of the capacitance of a single strip to the backplane C_{strip} and the interstrip capacitance C_{int}. C_c should be large compared to C_{strip} and C_{int}. The real part of the impedance of the AC coupling reflects the resistance of the p^+ implant along the strip.

As shown in figure 12.15, the complex impedance of the AC coupling has been measured in the following way: The sensor was biased to full depletion first. The DC and AC pads of one strip were connected to the two terminals of the LCR meter

(Agilent 4980A), and the coupling impedance were measured for different frequencies of the AC voltage.

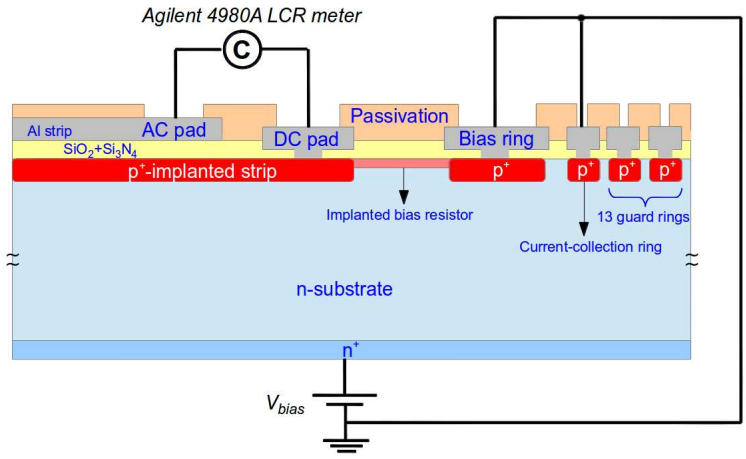

Figure 12.15: Measurement scheme for the coupling capacitance of the AC coupled microstrip sensor.

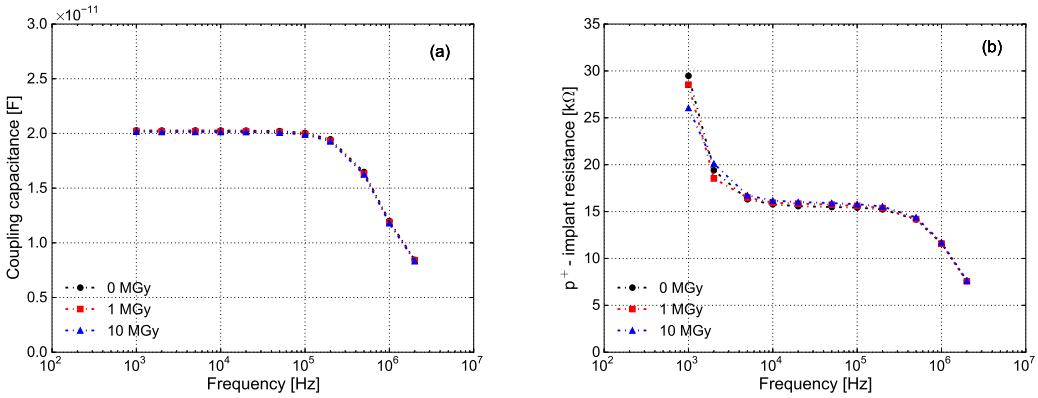

Figure 12.16: (a) Coupling capacitance (in series mode) as function of frequency for doses of 0, 1 and 10 MGy. (b) The real part of coupling impedance (in series mode) as function of frequency for doses of 0, 1 and 10 MGy.

The coupling capacitance C_c, as seen in figure 12.16(a), does not change with X-ray irradiation. Its value measured at low frequencies is 20.2 pF. The calculated value of the coupling capacitance from the geometrical parameters is $C_c^{cal} = C_{ox} \cdot C_{ni}/(C_{ox} + C_{ni})$ = 19.1 pF, with C_{ox} and C_{ni} the capacitances due to the SiO_2 and Si_3N_4 layers. The calculated value agrees with the measurement within 6%, which may arise due to the errors of the thicknesses of SiO_2 and Si_3N_4 layers ($\pm$ 5 nm) or the width of the aluminium ($\pm$ 1 μm). A reduction of coupling capacitance at high frequencies is observed: As the frequency increases, the AC signal does not propagate along the entire strip. A simple RC circuit for the complex coupling impedance is shown in figure 12.17.

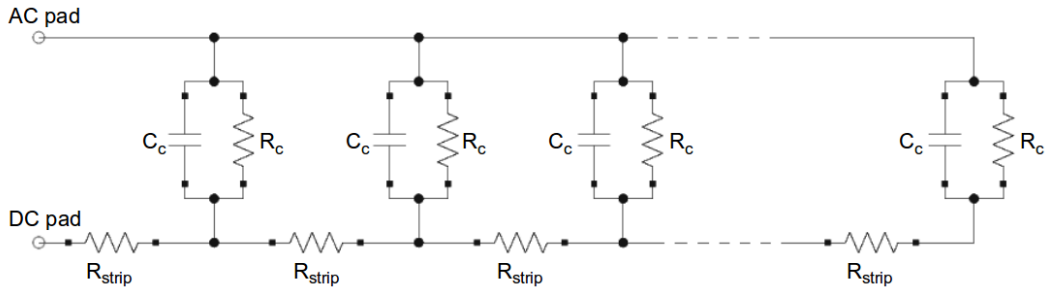

Figure 12.17: The RC circuit for the coupling impedance measurement: C_c and R_{strip} are the coupling capacitance and the p^+-implant resistance per unit cell.

A similar frequency dependence of the real part of coupling impedance is also seen in figure 12.16(b). In the medium frequency region ($f \sim$ [10 kHz, 100 kHz]), the resistance given by the measurement is 15.6 kΩ. The increase of the resistance at frequencies below 10 kHz is caused by the resistor R_c due to the leakage current through the SiO_2. The values of C_c, R_c and R_{strip} used in the RC circuit consisting of 100 unit cells shown in figure 12.17 are 0.202 pF, 400 GΩ and 460 Ω, respectively.

The RC circuit for the coupling capacitance and p^+-implant resistance has also been implemented into a SPICE model, which will be discussed in chapter 13.

12.3. Change of electrical properties of microstrip sensors irradiated with bias

In a previous chapter, the electric field dependence of the oxide-charge density, surface-current density and interface-trap density have been discussed for a MOS capacitor as function of X-ray dose. It was concluded that, as the electric field in the oxide of a segmented p^+n sensor points from the Si-SiO_2 interface to the aluminium electrodes, the electrical properties (dominated by N_{ox}, N_{it} and J_{surf}) will not show significant changes if a bias voltage is applied during irradiation. To verify this, two silicon microstrip sensors, labelled CF0632 and CF0636 as indicated in table 12.1, were irradiated to 1 MGy dose without and with a bias voltage of 35 V applied. The resistivity of the two sensors, CF0632 and CF0636, are 9.2 and 7.7 kΩ·cm, respectively.

The electrical properties of the two sensors have been characterized before and after irradiation. To address the main differences for the two sensors irradiated without and with bias voltage applied, the measurements on sensor capacitance, leakage current and interstrip capacitance will be shown in the following.

12.3.1. Sensor capacitance

Figure 12.18(a) shows the sensor capacitance C_{bulk}, which refers to the capacitance measured by connecting the bias ring and the backplane, as function of bias voltage for the microstrip sensors irradiated to 1 MGy without and with a bias voltage of 35 V applied, as well as the curve before irradiation. A shift of $\sim$ 10 V of the full depletion voltage is observed after irradiation; however, the same shift of V_{dep} is observed for

sensors irradiated without and with bias voltage applied during irradiation. Even if there is a (small) difference in N_{ox} for the two cases, the values of N_{ox} are larger than 3.0×10^{11} cm^{-2}, where the full depletion voltage V_{dep} is independent of N_{ox}.

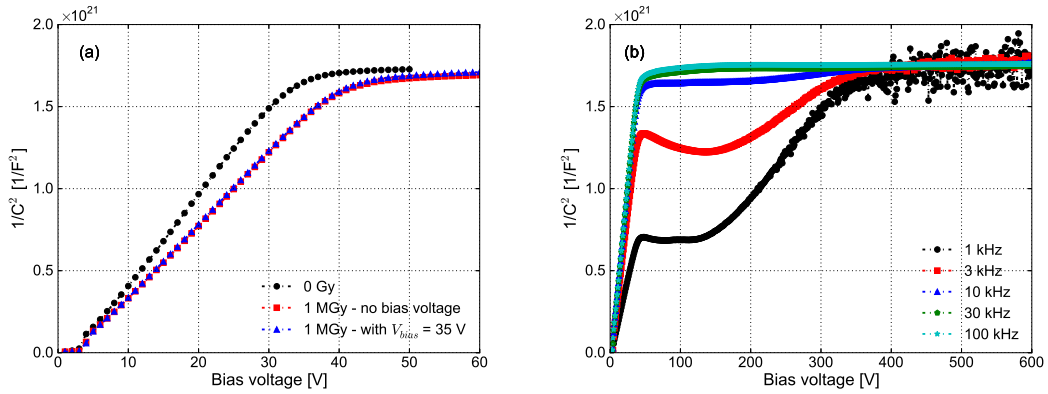

Figure 12.18: (a) Change of the full depletion voltage after irradiation to 1 MGy with or without bias. Curves measured with 100 kHz are shown. (b) Sensor capacitance vs. bias voltage for frequencies of 1, 3, 10, 30 and 100 kHz after irradiating the sensor to 1 MGy with a bias voltage of 35 V.

Figure 12.18(b) are the curves of C_{bulk} vs. V_{bias} measured with frequencies of 1, 3, 10, 30 and 100 kHz for the sensor irradiated with a bias voltage of 35 V. The frequency dependence of the sensor capacitance below 100 V is similar to that shown in figure 12.5(b); however, the extended measurement to the bias voltage of 600 V show that the frequency dependence of C_{bulk} disappears above 400 V. This behaviour can be understood in the following way: Radiation-induced traps at the Si-SiO_2 interface contribute to the capacitance measurement, as discussed in chapter 6, but how much the interface traps are able to contribute depends on the position of the quasi Fermi level of the n-bulk silicon with respect to the energy level of the trap. The interface traps covered by the accumulation layer will not contribute to the measured capacitance due to the shielding by electrons. In the region between the p^+ implant and the electron-accumulation layer, the interface is in deep depletion. In this situation, the quasi-Fermi level of the n-bulk silicon is below the valence band and the energy levels of all interface states so that the contribution to the capacitance due to the interface traps is small, refer to figure 6.8. However, in the boundary region between the electron-accumulation layer and the depletion layer at the interface, the quasi-Fermi level is within the silicon band gap and the density of majority carriers is not high enough to shield the interface traps. Hence, the interface traps located in this boundary region contribute to the capacitance. The capacitance caused by the interface traps, C_{it}, in the boundary region is in series with the capacitance due to the depleted interface, C_{dep}^{int}. Then, the expected sensor capacitance, C_{bulk}^{exp}, is given by

$$C_{bulk}^{exp}(f) = C_{dep}^{bulk} + \frac{C_{it}(f) \cdot C_{dep}^{int}}{C_{it}(f) + C_{dep}^{int}} \tag{12.3}$$

with C_{dep}^{bulk} the capacitance of the depleted Si-bulk. With increasing bias voltage V_{bias}, as the depleted area at the Si-SiO_2 interface increases according to $I_{leakage} - V_{bias}$ measurement and shown by the TCAD simulation, the value of C_{dep}^{int} decreases. C_{it} dominates in the branch of the circuit consisting of C_{it} and C_{dep}^{int} at small voltages, whereas C_{dep}^{int} dominates for higher voltages. Hence, at high voltages, the frequency response of the measured bulk capacitance disappears due to the reduction of the effects from the interface traps. This is also expected for the sensor without bias voltage applied during irradiation (not shown here).

12.3.2. Leakage current

The leakage current measured between bias ring and backplane was also measured for the sensors irradiated to 1 MGy without and with a bias voltage applied during irradiation. The leakage current from CF0636 before irradiation is as low as 4.8 nA, which corresponds to a bulk-generation current of 0.27 $\mu A/cm^3$.

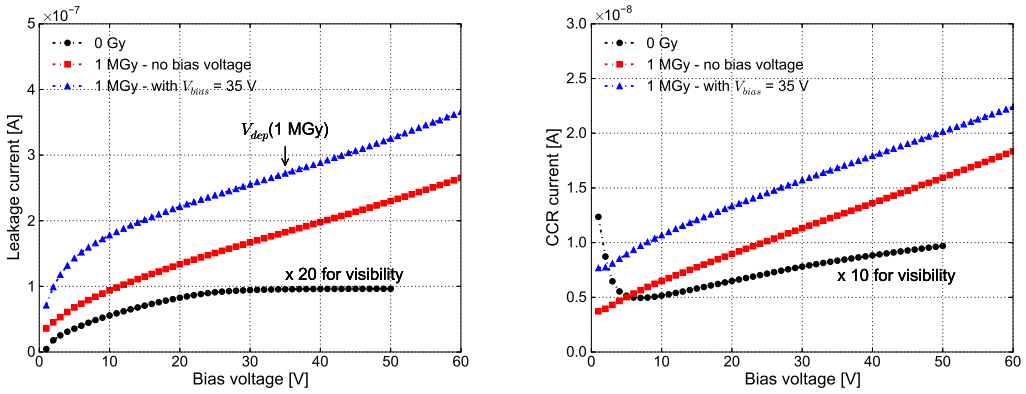

Figure 12.19: (a) Sensor leakage current vs. bias voltage for doses of 0 and 1 MGy without and with bias during irradiation. (b) CCR current vs. bias voltage for doses of 0 and 1 MGy without and with bias during irradiation.

As seen in figure 12.19(a), both the $I_{leakage} - V_{bias}$ curves of the sensors with and without bias applied show a similar linear dependence on bias voltage as shown in figure 12.7, which is explained by the increase of the depleted area at the Si-SiO_2 interface. The leakage currents $I_{leakage}$ at $V_{bias} = 60$ V are 345 nA and 462 nA for the irradiations without and with bias voltage, respectively. The values of $I_{leakage}$ at different V_{bias} for the two irradiation conditions agree within 50%, which is consistent with the study on the gate-voltage dependence of N_{ox} and J_{surf}.

Figure 12.19(b) are the measured currents flowing into the current-collection ring (CCR) versus bias voltage. The linear dependence of CCR current on the bias voltage is similar to the measurement of the leakage current through the bias ring, which can be interpreted by the same model; however, the values of the CCR current are about 10 times smaller than the leakage current. For irradiated sensors, both the leakage current of the sensor and the CCR current are dominated by the surface current, which equals to the surface-current density multiplied by the depleted interface area.

As the surface-current density is fixed after irradiation, the large difference in the values of the CCR current and the leakage current comes from the different depleted interface area.

12.3.3. Interstrip capacitance

The interstrip capacitance C_{int}, as mentioned in a previous section, depends on frequency, irradiation dose and bias voltage. The frequency dependence of C_{int} is explained by a SPICE model presented in chapter 13. The bias voltage dependence of C_{int} is due to the change of the width of the electron-accumulation layer (or the depleted area at the Si-SiO_2 interface), which however depends on the density of positive charges at the interface.

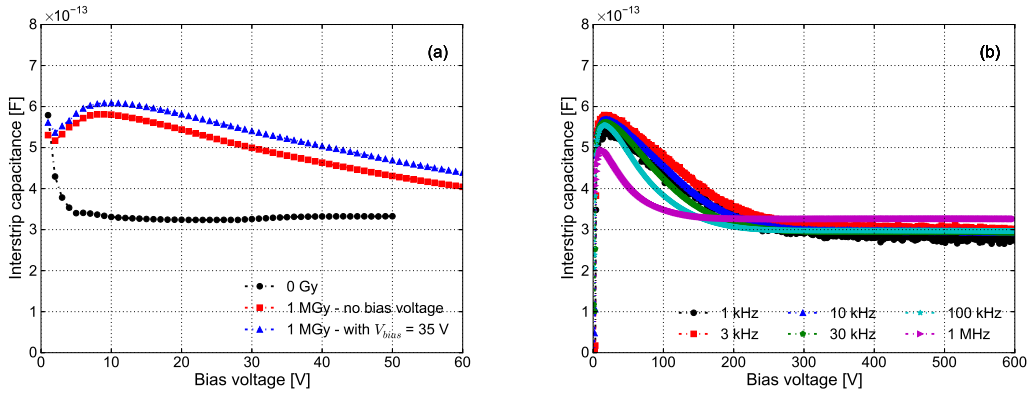

Figure 12.20: Change of the interstrip capacitance with bias voltage and irradiation condition. (a) Interstrip capacitance vs. bias voltage for 0 Gy and 1 MGy irradiated with and without bias voltage appled. Measurement results for 1 MHz are shown. (b) Interstrip capacitance vs. bias voltage for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz after irradiation to 1 MGy with bias.

For the irradiation with a bias voltage, the oxide-charge density is slightly higher than for the case without a bias, as seen in figure 10.5 the gate-voltage dependence of N_{ox} for a dose at which N_{ox} does not saturate. Hence, an increase in C_{int} is expected and observed for irradiation with bias compared to an irradiation without bias because of the different depleted area at the interface between the p^+ implant and the electron-accumulation layer. The measured C_{int} as function of bias voltage for 0 Gy and 1 MGy without and with bias applied during irradiation is shown in figure 12.20(a).

Figure 12.20(b) are the $C_{int} - V_{bias}$ curves for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz from the sensor irradiated to 1 MGy with bias. A frequency dependence of C_{int} below 200 V is also observed as already seen in 12.10(b). C_{int} saturates at bias voltage $V_{bias} > \sim 200$ V, and its value is reduced to a level similar to 0 Gy.

12.4. Summary and relevance to AGIPD sensor

p^+n silicon microstrip sensors have been irradiated to doses up to 10 MGy with 12 keV X-rays at the DESY DORIS III synchrotron. The electric properties, full depletion voltage V_{dep}, leakage current $I_{leakage}$, interstrip capacitance C_{int} and resistance R_{int}, and coupling capacitance C_c, have been characterized before and after irradiation. The results can be explained by assuming that the radiation-induced positive charges in the oxide or at the Si-SiO_2 interface produce an electron-accumulation layer in the region between p^+ implants below the interface, and its size decreases with increasing bias voltage V_{bias}. Especially, the leakage current $I_{leakage}$ and interstrip capacitance C_{int} are influenced by the size of this electron-accumulation layer. Hence, it is expected that an optimization of the geometrical layout of the pixels is able to reduce the noise in the read-out signal due to $I_{leakage}$ and C_{int} reasonably.

An increase in the full depletion voltage V_{dep} with irradiation is observed. However, the change of V_{dep} with dose saturates at an oxide-charge density of $\sim 3 \times 10^{11}$ cm^{-2}. As the change of V_{dep} before and after irradiation is only $\sim$ 10 V, it will not affect the operation of the AGIPD sensor used at the XFEL, where a high voltage is required to reduce the plasma effect [85–87] caused by the intense X-ray photons.

As the formation of oxide charges and interface traps depend on the electric field in the SiO_2, the oxide-charge density, the interface-trap density and the uniformity of the charges at the Si-SiO_2 interface will be different for silicon sensors irradiated with and without bias. Thus, the electrical properties have also been characterized for the silicon microstrip sensor irradiated with a bias voltage applied during irradiation. Results show an increase in $I_{leakage}$ and C_{int} compared to the irradiation without a bias voltage applied. However, the differences are small and further reduced with increased bias voltage V_{bias}. This confirms the conclusion that has been drawn in the study of the gate-voltage dependence of oxide-charge density, interface-trap density and surface-current density: For a p^+n segmented sensor, the electric field in the oxide points from the Si-SiO_2 interface to the aluminium electrode, and therefore no big differences exist in the dose dependence of N_{ox}, N_{it} and J_{surf}; and no pronounced differences in the electrical properties and performance of segmented p^+n sensors are expected.

13. SPICE simulation for p^+n microstrip sensors

The total strip capacitance of a silicon microstrip sensor influence the detector performance. In an AC coupled silicon sensor the charge induced on the implanted strip is shared by the coupling capacitance to the read-out electronics of the particular strip, the capacitances to the neighbouring strips and the backplane [88]. Hence, in order to avoid signal losses, the coupling capacitance has to be as high as possible with respect to other capacitances. In addition, the noise level in the readout signal depends on the capacitance seen by the preamplifier. In addition to capacitances, also the resistances influence the signal and the noise of the recorded signals. For a silicon microstrip sensor, each sensor elements behave like a transmission line resulting in a frequency dependence of the measured capacitance and resistance. Therefore, it is important to understand the frequency dependence of the system.

In chapter 12, simple RC circuits have been introduced in order to explain the frequency dependence of the interstrip capacitance and coupling capacitance for the p^+n microstrip sensor. In this chapter, a complete SPICE model for an AC coupled microstrip sensor will be introduced and discussed.

The SPICE model has been developed and extensively used for the propagation of signals through the sensor for single-sided and double-sided AC coupled silicon microstrip detectors [88–95]. This model allows to predict the frequency response of both the real part and imaginary part of the impedance measurements for sensor capacitance, interstrip capacitance and coupling capacitance. The results from the SPICE simulation for the CiS microstrip sensor have been compared to the measurements, and a good agreement is seen.

The SPICE model discussed in this chapter is able to describe the measurement results of the non-irradiated sensor. For irradiated sensors, due to the presence of radiation-induced interface traps at the Si-SiO_2 interface which complicates the RC circuit, the SPICE simulation however is not possible to describe the measurements on irradiated sensors. Thus, a comparison between the results from SPICE simulation and measurements will be made for the non-irradiated sensor, whereas the failure of the SPICE model for irradiated sensor discussed at the end.

13.1. The SPICE model

The SPICE model for an AC coupled microstrip sensor consists of a complex RC circuit. The sensor in the model is divided into unit cells along the strip. Each cell, as seen in figure 13.1, consists of R_{bulk}, C_{bulk}, C_{int}, R_{int}, C_s, C_c (R_c, which is parallel to each C_c, is not shown due to the limit of the space), and C_{met}. The meaning of the

symbols are listed in table 13.1. Neighbouring cells are connected through a resistor for the top layer of aluminium R_{met}, a resistor for the p^+ implant R_{strip}. In addition, R_{bias}, the low-doped bias resistor, is connected to the end of each strip and the bottom (rear side) of each cell is connected together.

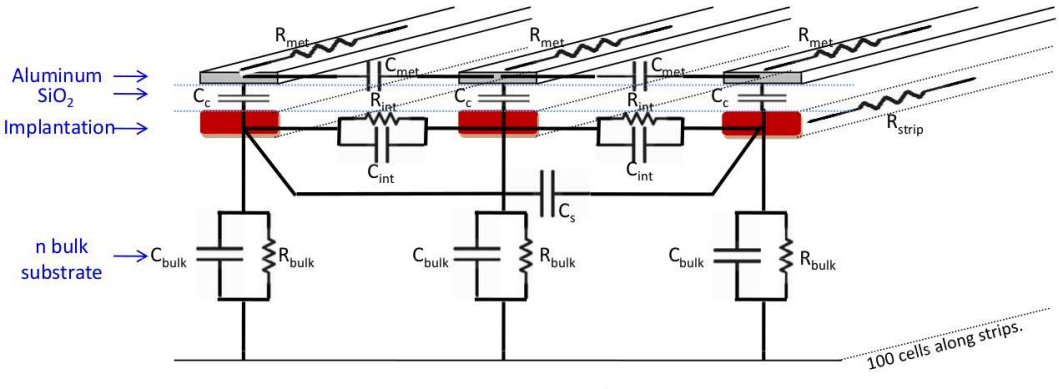

Figure 13.1: SPICE model for the AC coupled p^+n microstrip sensor: One unit cell with only 3 strips is shown. R_c is not shown due to the limit of the space, but parallel to each C_c. For SPICE simulations, 100 unit cells and 5 strips are used.

Parameter	Value
R_{strip}	resistance of p^+-implant strip
R_{bias}	resistance of bias resistor
R_{met}	resistance of aluminium strip
R_{bulk}	bulk resistance of depleted silicon
R_{int}	real part of interstrip impedance
R_c	real part of coupling impedance
C_c	coupling capacitance
C_{bulk}	capacitance of depleted silicon
C_{int}	capacitance between adjacent implanted strips
C_{met}	capacitance between adjacent aluminium strips
C_s	capacitance between one and its second neighbouring strip

Table 13.1: Symbols in the SPICE model.

The RC network of the SPICE model is built up from 100 unit cells ($\sim$ 12 cells/mm for the CiS microstrip sensor with a strip length of 7.9 mm) of capacitors and resistors. The complete model of the sensor contains more than 50 thousand circuit elements. According to [88], it is found empirically that 6 cells/mm is the minimum number of cells needed to reproduce the measured data. Because the strips can be regarded as transmission lines, the more cells are introduced in the circuit the higher accuracy can be obtained. Therefore, 12 cells/mm used in this study is expected to be enough to produce precise simulation results.

13.2. Results

As seen in figure 13.2(a)-1 and (a)-2, the frequency dependence of the capacitance and resistance from the impedance measurement between the 5 implanted strips (DC strips) and the rear side of the sensor exhibit a plateau: The plateau value of the capacitance gives the geometrical capacitance of the depleted silicon; The plateau value of the resistance equals to the value of the bias resistance divided by the number of strips used in the simulation.

From the frequency dependence of the capacitance from the impedance measurement between neighbouring implanted strips through DC pads, as seen in figure 13.2(b)-1, the plateau value of the $C(f)$ curve is given by $C_{int} + C_{bulk}/2$.

Figure 13.2(c)-1 and (c)-2 show the frequency dependence of the capacitance and resistance from the impedance measurement between the DC pad and the AC pad of one strip. The plateau of the $C(f)$ curve gives the value of the coupling capacitance. The decrease of $C(f)$ and $R(f)$ at higher frequencies, as explained in chapter 12, is due to the attenuation of the AC signal at high frequencies. The presence of the resistor due to the p^+ implant and the aluminium, the coupling of the metal and the implanted strips is equivalent to a number of high-pass filters connected in parallel. The sharp increase of $R(f)$ curves with decreasing frequency is caused by the resistance in parallel to the coupling capacitance, namely R_c.

Most of the parameters listed in table 13.1 can be determined either directly from the measurements or from a comparison between the measurements and calculations for a simple RC model consisting of a transmission line: For example, R_{strip}, R_{bulk}, R_c, C_c, C_{int} and C_{bulk}. In addition, R_{met} and R_{bias} can be obtained directly from an I-V measurement. Thus, the remaining parameters are R_{int}, C_{met} and C_s, which however are determined from comparisons between the measured $C(f)$ and $R(f)$ curves and the simulated ones with the SPICE model.

Figure 13.2 shows the $C(f)$ and $R(f)$ curves from both the measurements and SPICE simulations, which show good agreement. The values of the parameters in the SPICE model are listed in table 13.2.

Parameter	Value
R_{strip}	58 kΩ/cm
R_{bias}	0.5 MΩ
R_{met}	20 Ω·cm
R_{bulk}	0.24 TΩ·cm
R_{int}	67 MΩ·cm
R_c	3.2 GΩ·cm
C_c	25 pF/cm
C_{bulk}	0.3 pF/cm
C_{int}	0.13 pF/cm
C_{met}	0.13 fF/cm
C_s	6.25 fF/cm

Table 13.2: Parameters used in SPICE simulation.

According to the understanding of the SPICE model and the results obtained from the SPICE simulation, some features can be concluded as follows: One of the most important parameters, the coupling capacitance, only depends on the parameter C_c in the SPICE model. The behaviour of its $C(f)$ curve at higher frequencies is caused by R_{strip}, as discussed above. The increase of $R(f)$ at lower frequencies is due to R_c. Hence, C_c, R_{strip} and R_c can be determined from the impedance measurement of the coupling capacitance. C_{bulk} and R_{bulk} can be directly obtained from the plateau values of the capacitance between the implanted strips and the backplane of the sensor and the frequency dependence of the resistance at low frequencies.

13.3. Summary and discussion

A SPICE model for the AC coupled silicon microstrip sensor has been used to describe the frequency dependence of the real and imaginary parts of the impedance measurements for sensor capacitance, interstrip capacitance and coupling capacitance. Most of the parameters in the SPICE model can be obtained from the experimental data. Those parameters which cannot be directly obtained are determined through comparisons of $C(f)$ and $R(f)$ curves between the measurements and the SPICE simulations. The simulated curves show good agreement with the measured ones. In addition, some features and experience obtained from this study are summarized for the understanding of the frequency response.

The SPICE model is able to describe the measurement results for the non-irradiated sensor. For the irradiated sensor, the presence of radiation-induced interface traps, which can be charged and/or discharged and thus behave as frequency dependent capacitors, complicates the RC circuit so that the present SPICE model dose not work. For the future improvement, introducing a subcircuit in each unit cell taking the contribution from the interface traps into account is proposed. The subcircuit in each unit cell should at least contains one capacitor coupled to the adjacent p^+ implants from the interface where the interface traps can respond, one capacitor and one resistor coupled from the interface to the rear side of the sensor. The new model approaches to the original SPICE model when the capacitance due to interface traps are not dominant at high bias voltages.

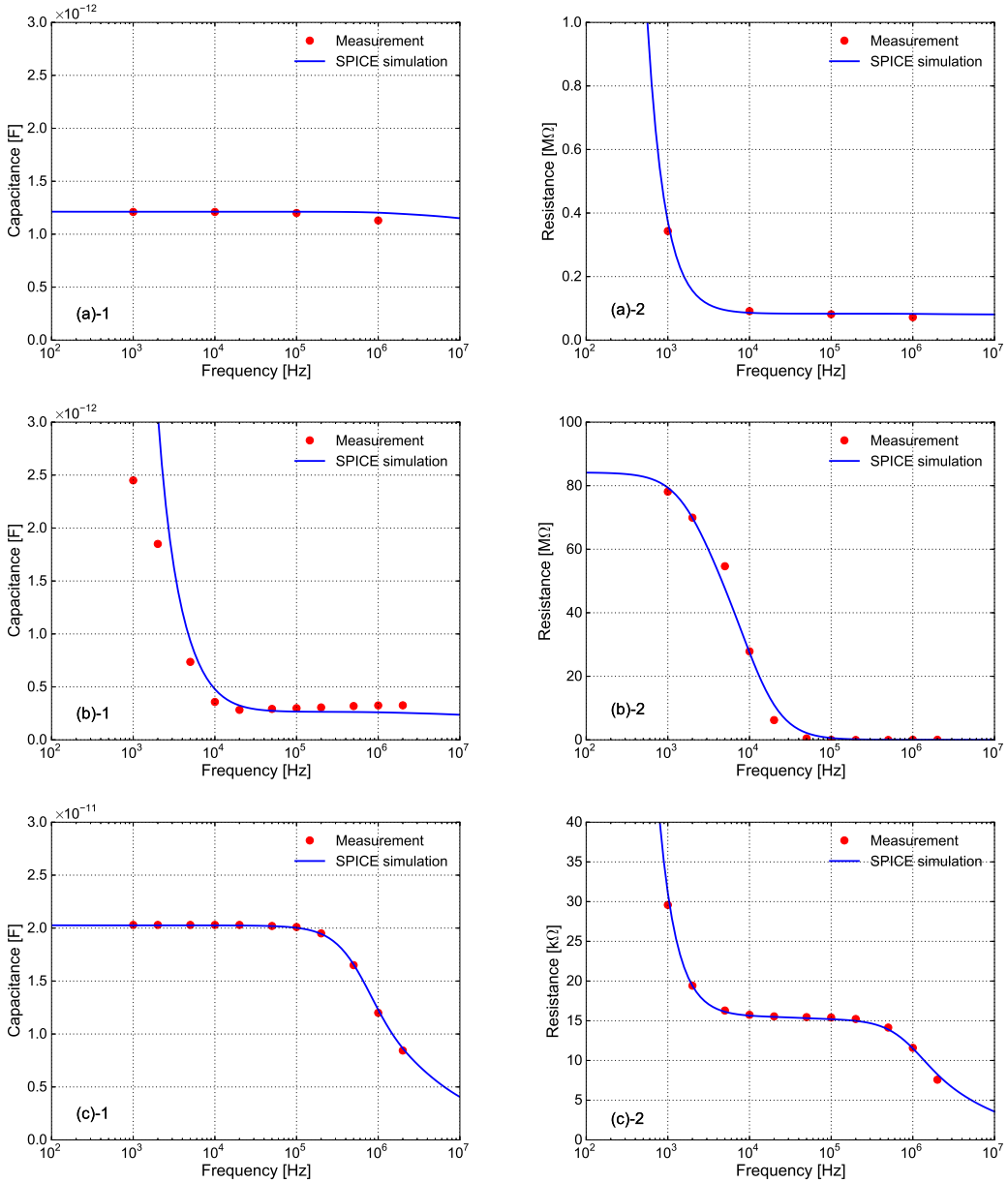

Figure 13.2: Comparison of results from SPICE simulation and measurements: (a)-1 & (a)-2 $C(f)$ and $R(f)$ from the impedance measurement between the 5 implanted strips and the rear side of the sensor. (b)-1 & (b)-2 $C(f)$ and $R(f)$ from the impedance measurement between the neighbouring implanted strips through DC pads. (c)-1 & (c)-2 $C(f)$ and $R(f)$ from the impedance measurement between the DC pad and the AC pad of one strip.

14. Design of the AGIPD sensor

At the European XFEL, silicon pixel detectors will be used for imaging experiments. One of the ongoing detector developments is the Adaptive Gain Integrating Pixel Detector (AGIPD) Project, which has to fulfil extraordinary performance specifications [2]: A dynamic range of 0, 1 up to more than 2×10^4 12.4 keV photons per pixel of 200 μm $\times$ 200 μm arriving within less than 100 fs, a frame rate of 4.5 MHz to satisfy the time interval between XFEL pulses of 220 ns, and a radiation tolerance for doses up to 1 GGy for 3 years of operation. To address these challenges, radiation-hard silicon pixel sensors and electronic components with outstanding performance need to be developed.

The complete AGIPD Project is conducted within a collaboration between Deutsches Elektronen-Synchrotron (DESY), Hamburg University, Bonn University and Paul Scherrer Institute (PSI, Villigen, Switzerland). The detector group of Hamburg University is responsible for the sensor design for AGIPD. In this chapter, efforts made by the detector group of Hamburg University on understanding the plasma effect, X-ray induced radiation damage and their influence on silicon pixel sensors are shortly summarized and the layout design of the AGIPD sensor based on detailed TCAD simulations are presented.

14.1. Studies relevant for the AGIPD sensor

To meet the requirements of silicon sensors for experiments at the European XFEL and to design a radiation-hard silicon pixel sensor for the AGIPD Project, the detector group of Hamburg University has studied the following main issues:

Plasma effect The densities of electrons and holes in silicon sensors created by the high intensity X-rays at the European XFEL produce the so-called plasma effect. The plasma formed by the high densities of electrons and holes dissolves slowly. The boundary of the plasma shields the electric field created by the external bias voltage and the ionized dopant of the silicon crystal. Thus the pulse shape changes significantly and the time needed to collect all charges is increased. Two processes are involved in the separation of electrons and holes from the plasma: Diffusion and repulsion. Before electrons and holes are separated ambipolar diffusion is the dominant process. Once electrons and holes are separated, the electrostatic repulsion increases the spread of the electrons and holes. We have extensively studied this topic [85–87,96]. As expected, the plasma effect decreases as the electric field increases. From the study we conclude: An operating voltage above 500 V of the AGIPD sensor should be used in order to reduce the influence on the charge-collection time, due to the plasma effect.

Surface damage X-rays with energies below 300 keV cause surface damage in silicon sensors, whereas hadrons, gamma-rays and high energy electrons cause bulk damage in silicon crystals. Thus, at the European XFEL surface damage dominates: Oxide charges and interface traps will build up with time in the SiO_2 and at the Si-SiO_2 interface, respectively. The oxide charges are positive, thus they induce electrons which accumulate in the silicon below the Si-SiO_2 interface (electron-accumulation layer); the interface traps increase the surface current. The presence of the oxide charges and interface traps induced by X-rays influences the electrical properties of segmented p^+n sensors [46, 83]: Increase of the leakage current, the full depletion voltage and the interpixel/interstrip capacitance; decrease of the interpixel/interstrip resistance and the mobility of minority carriers below the interface; reduction of the breakdown voltage; and charge losses close to the interface. We observe that an electron-accumulation layer forms below the Si-SiO_2 interface after irradiation, whose width (refer to the lateral extension along the Si-SiO_2 interface in-between adjacent segmented p^+ implants) increases with dose and decreases with applied bias voltage. The electron-accumulation layer is responsible for the change of the electrical properties, i.e. the increase of the full depletion voltage and the interpixel/interstrip capacitance.

Charge losses for charges presented close to the Si-SiO_2 interface The charge losses close to the Si-SiO_2 interface of segmented p^+n sensors have been studied using multi-channel time-resolved current measurements (multi-TCT). Depending on the applied bias voltage, biasing history and environment like humidity, incomplete electron or hole collection and both electron- and hole-accumulation layers with different widths have been observed. For non-irradiated sensors, it is found that electrons losses occur when ramping up the voltage in a dry atmosphere, hole losses when ramping down the voltage in a dry atmosphere and no or little charge losses in a humid atmosphere. For irradiated sensors, electron losses have always been observed no matter ramping up or ramping down the voltage in a dry or humid atmosphere and the higher the voltage the less the electron losses. Results of this study are presented and discussed in [79–81].

Optimization of the AGIPD sensor The AGIPD sensor has to satisfy the following specifications to meet the requirements at the XFEL: Interpixel capacitance of less than 0.5 pF, a maximal leakage current per pixel of 1 nA, and an operating voltage of above 500 V in order to reduce the plasma effect. To guarantee safe operation the design goal has been set at a maximal operating voltage close to 1000 V. A complete list of the AGIPD sensor specifications is described in [77]. The specifications should also be met after 3 years of operation with an accumulated dose up to 1 GGy non-uniformly distributed over the sensor. To design the AGIPD sensor, experimental data on the dose dependence of the oxide-charge density and the surface-current density obtained from surface-damage studies, have been implemented in the Synopsys TCAD simulation program in order to optimize the layouts of the pixel and the guard-ring structure. The methodology of the sensor design, the optimization of the most relevant parameters and the simulated performance, like breakdown voltage, leakage current and interpixel capacitance, as function of the X-ray dose are reported

in [77,78]. It is found that in order to achieve a breakdown voltage of $\sim$ 1000 V for the AGIPD sensor after irradiation to 1 GGy (corresponding to an oxide-charge density of 3×10^{12} cm^{-2}), 15 floating guard rings and 1 current-collection ring with a junction depth of 2.4 μm and an oxide thickness of 250 nm are required. In addition, a gap of 20 μm between the p^+ implants of neighbouring pixels and a metal overhang of 5 μm are needed to meet the requirements for the interpixel capacitance and the leakage current.

The studies mentioned above form the basis of designing a silicon pixel sensor for the AGIPD.

14.2. Specification of the AGIPD sensor

The complete arrangement of AGIPD sensors is shown in figure 14.1(top). It consists of 2 $\times$ 8 separated sensors. An individual sensor is shown at the bottom of figure 14.1. The overall geometrical dimensions of the sensor after cutting are 107.6 mm $\times$ 28.0 mm.

Each sensor consists of 2 $\times$ 8 fields of 64 $\times$ 64 pixels. To each field a separated ASIC is bump-bonded. The specifications of the AGIPD sensor, based on the forementioned studies and science simulation, are given in table 14.1. All the specifications should also be satisfied after irradiation to doses of up to 1 GGy.

Parameter	Specification
Sensor thickness	500 $\pm$ 20 μm
Width guard-ring structure	1200 μm
Pixel size	200 μm $\times$ 200 μm
Type	p^+ on n
Coupling	DC
Resistivity	3-8 kΩ·cm
V_{dep}	< 200 V
V_{op}	500 V
V_{bd}	$\geqslant$ 900 V
C_{int} at V_{op}	< 0.5 pF
I_{leak} at V_{op}	< 1 nA/pixel

Table 14.1: The specifications of the AGIPD sensor. V_{dep}: full depletion voltage; V_{op}: operating voltage; V_{bd}: breakdown voltage; C_{int}: inter-pixel capacitance; I_{leak}: leakage current.

The attenuation length of 12.4 keV X-rays in silicon is 252 μm, thus a thicker silicon (here 500 μm as specified) is needed to absorb more photons. The resistivity of the silicon substrate should not be too high, otherwise the depletion region touches the cut-edge of the sensor and thus reduce the breakdown voltage for the non-irradiated sensor. The specification of the operating voltage of 500 V is a result of the study of plasma effect: The higher the operating voltage, the shorter the time needed to collect all charges produced by the X-rays. For a safe operation of the silicon pixel sensor,

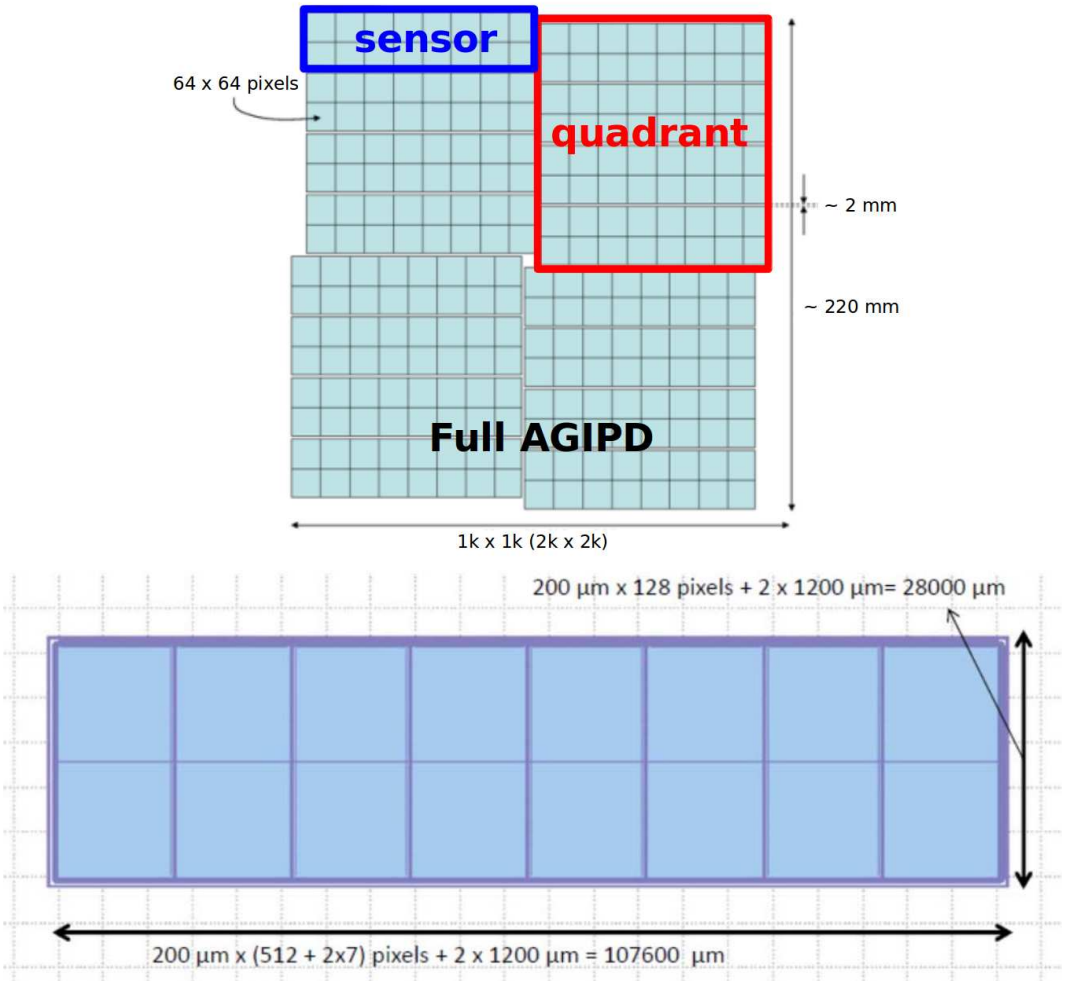

Figure 14.1: Top: The complete sensors of the AGIPD detector. Bottom: Overall layout and dimensions of an AGIPD sensor. The 2 rows of 8 fields correspond to 16 readout chips bump-bonded to the sensor. The dimensions of the sensor after cutting are 107.6 mm $\times$ 28.0 mm.

a breakdown voltage is specified as high as 900 V. 900 V is the maximal breakdown voltage that a sensor (irradiated to 1 GGy) can achieve according to detailed TCAD simulations [77]. The maximal inter-pixel capacitance and leakage current are defined based on their contribution to the readout noise.

14.3. Sensor optimization and design of the AGIPD sensor

14.3.1. Sensor optimization

The design of the pixel layout and of the guard-ring structure of the AGIPD sensor is based on detailed TCAD simulations with damage-related parameters, i.e. the oxide-charge densities and the surface-generation velocities (results of the surface-current densities) for different X-ray doses, extracted from the studies on surface-radiation damage described in this thesis.

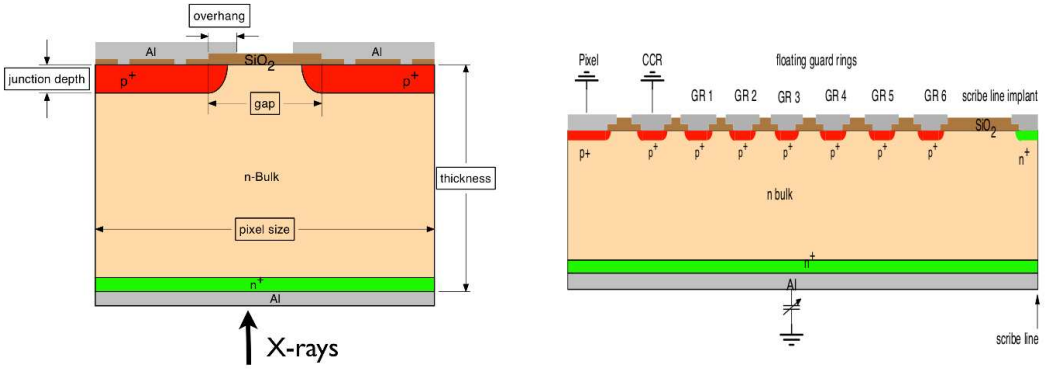

Figure 14.2: Sketch of the sensor region simulated for the pixel (left) and guard-ring (right) optimization. The layout for the guard-ring optimization consists of half a pixel, a current-collection ring (CCR), multiple floating guard rings (GRs) and n^+-implant close to the scribe line. Picture taken from [77].

The parameters shown in figure 14.2, which have been optimized in the design of pixel layout and guard-ring structure to fulfil the specifications, include the gap between neighbouring p^+-implants, metal overhang, radius of p^+-implant and metal at the corners of pixels, guard-ring structure (number of guard rings, p^+-implant widths, metal overhangs of each ring, and gaps between rings), and process-related parameters like the depth of p^+ implant and the thickness of SiO_2 [77]. With Synopsys TCAD, the following electrical parameters have been simulated: For the pixel, the breakdown voltage (V_{bd}), the leakage current (I_{leak}) and the inter-pixel capacitance (C_{int}); for the guard-ring structure, the breakdown voltage (V_{bd}) and the minimal distance between the boundary of depleted region and the cut-edge of the sensor for doses from 0 to 1 GGy and for different bias voltages.

The strategy which was used for the optimization of pixel layout and guard-ring structure has been described by J. Schwandt in [77]. It can be shortly summarized as follow:

Optimization of guard-ring structure The guard-ring structure (GR) was optimized using Synopsys TCAD with 2-dimensional simulations in Cartesian coordinate for the straight edges, and with quasi 3-dimensional simulations in cylindrical coordinate for the four corners of the sensor:

- Optimize the breakdown voltage for a zero guard-ring structure consisting of only half a pixel and a current-collection ring (CCR) for different oxide-charge densities from 5×10^{10} cm^{-2} to 3×10^{12} cm^{-2} as function of the thickness of SiO_2, p^+-implant depth and size of metal overhang. It is found that the maximal breakdown voltage which can be achieved is $\sim$ 70 V for a SiO_2 thickness of 270 nm and a p^+-implant depth of 2.4 μm.
- Estimate the number of floating guard rings needed to achieve a breakdown voltage of above 1000 V: $N_{rings} = V_{bd}(\text{expected})/V_{bd}(\text{zero guard ring}) = 1000\ \text{V}/70\ \text{V} \simeq 15$. Hence, aiming for a breakdown voltage of 1000 V, the number of guard rings has to be at least 15.
- Design a guard-ring structure with 15 floating guard rings and vary the gap between guard rings, the p^+-implant widths and metal overhangs of guard rings to achieve a maximal breakdown voltage.

Optimization of pixel layout The pixel layout of the AGIPD sensor was optimized with 2-dimensional simulations in Cartesian coordinates, and cross-checked with 3-dimensional simulations in (x,y,z) coordinates:

- Optimize the thickness of SiO_2, size of metal overhang, gap between neighbouring p^+ implants and p^+-implant depth and extrapolate the simulated values of the breakdown voltage, the leakage current and the inter-pixel capacitance to their values in 3-dimensions.
- Check the breakdown voltage and leakage current with 3-dimensional simulations in (x,y,z) coordinates.

14.3.2. Layout of the AGIPD sensor

Guard-ring structure According to the TCAD simulations, it is found that a guard-ring structure with a current-collection ring and 15 floating guard rings, and with a p^+-implant depth of 2.4 μm and an oxide thickness of 270 nm, is able to achieve a breakdown voltage of 1000 V after irradiation to high doses (1 GGy). The breakdown voltage in a simulation with large oxide-charge density of 3×10^{12} cm^{-2} is found to be very sensitive to the oxide thickness t_{ox}: The value of the breakdown voltage increases with the oxide thickness for $t_{ox} \leqslant 270$ nm and then decreases for $t_{ox} > 270$ nm. The sudden decrease of the breakdown voltage is related to the electron-accumulation layer below the metal overhang: If an electron-accumulation layer exists below the metal overhang, the high electric field is located at the near-interface boundary of the p^+ implant; if no electron-accumulation layers are present below the metal overhang, two high field regions are found. One is located at the near-interface boundary of the p^+ implant, and the other one is located below the end of the metal overhang. In this case, the voltage drops over the entire region below the metal overhang and

thus the maximal electric field is reduced. To avoid the sharp drop of the breakdown voltage due to a possible variation of the oxide thickness caused during the growth of SiO_2, an oxide thickness of 250 nm is a reasonably choice. Following the procedures of optimization of the guard-ring structure, the optimized geometrical parameters for the layout of the guard-ring structure have been determined:

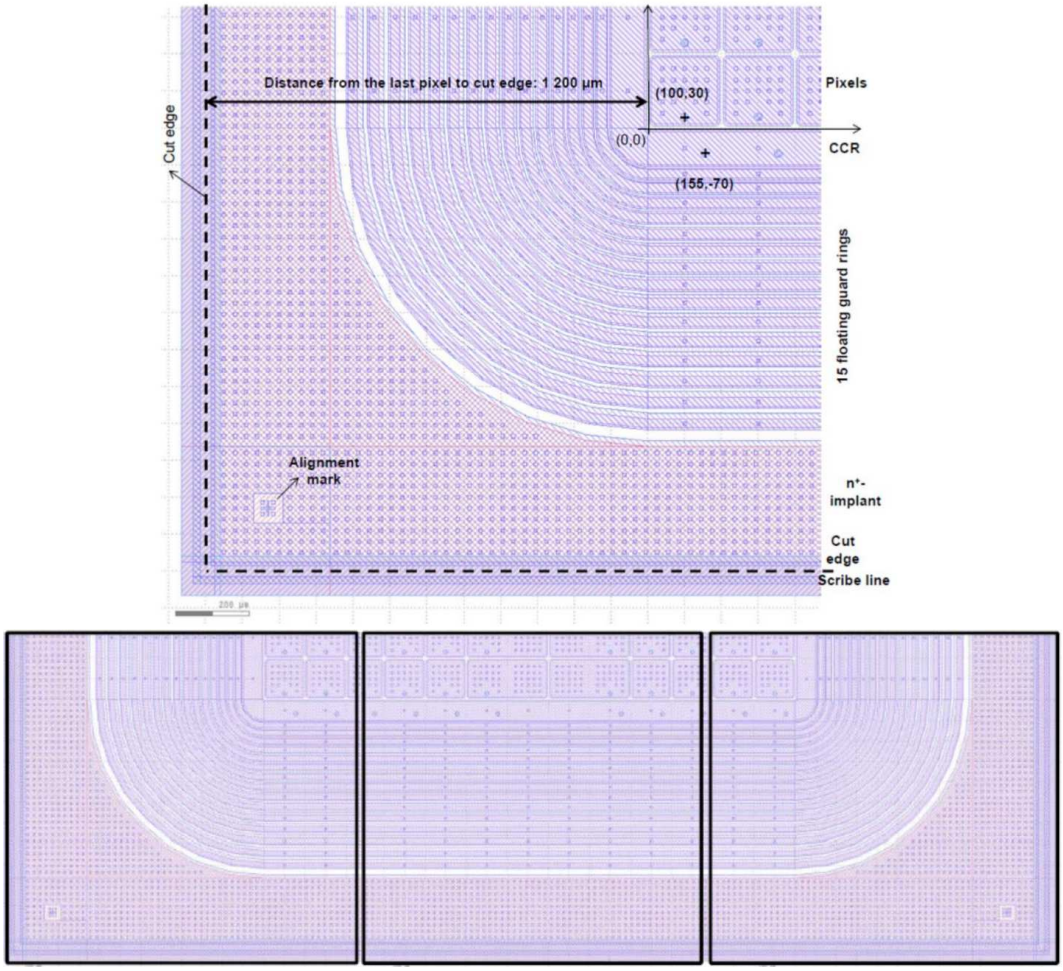

Figure 14.3: Layout and dimensions of the guard-ring structure. Top: Layout and dimensions of the guard-ring structure at the left lower corner of the sensor. Bottom: The guard-ring structures at the left, middle and right lower corners of the sensor.

- Gap between the last pixel and CCR: 20 μm
- Width of the p^+ implant of CCR: 90 μm
- Metal overhang of CCR on both sides: 5 μm
- Gap between CCR and 1^{st} GR: 12 μm
- Widths of the p^+ implants of 15 GRs: 25 μm
- Metal overhangs of GRs towards the last pixel: 2, 3, 4,..., 16 μm

- Metal overhangs of GRs towards the cut-edge: 5 μm
- Gaps between 1^{st} and 2^{nd}, 2^{nd} and 3^{rd},..., 14^{th} and 15^{th} GRs: 12, 13.5, 15,..., 33 μm

The layout of the guard-ring structure is shown in figure 14.3. The figure on the top gives the dimensions of the guard-ring structure at the left lower corner of the sensor: The distance from the last pixel to the cut-edge is 1200 μm. For the alignment of the bump-bonding, an alignment mark can be found at the corner of the guard-ring structure. The figures on the bottom shows the guard-ring structures at the left, middle and right lower corners of the sensor. Their corresponding upper parts are obtained by rotating the layout shown by 180°.

Using the present guard-ring structure, the breakdown voltage for sensors with different resistivity is simulated. The results show that the minimum breakdown voltage is 830 V for a resistivity of 3 kΩ·cm and an oxide-charge density of 2×10^{12} cm^{-2}, and is above 900 V for resistivities of 5 and 8 kΩ·cm. Additional simulations with low densities of oxide charges (5×10^{10} cm^{-2}) show that the depleted region of the sensor with a resistivity between 3 and 8 kΩ·cm dose not touch the cut-edge for voltages below 990 V. Thus the present design of the guard-ring structure according to the simulation satisfies the specifications.

Pixel layout Based on the results of pixel optimization [78], it is found that, in addition to the process parameters of p^+-implant depth of 2.4 μm and of the thickness of SiO_2 of 250 nm, with the following parameters the specifications can be met:

- Gap between neighbouring p^+ implants: 20 μm
- Metal overhang: 5 μm
- Radius of p^+ implants at pixel corners: 10 μm
- Radius of metal layers at pixel corners: 12 μm

The layout and dimensions of the standard 200 μm $\times$ 200 μm pixel is shown in figure 14.4. The squares are vias, through which the p^+ implant and the metal layer are connected. The three octagons centred at (100,30) are the opening through the passivation layer, the UBM (under-bump-metal) and the indium layer, respectively. The UBM is just 6 μ wider than the opening through the passivation, thus it is difficult to see their difference in the figure. They are used for the bump-bonding of the readout chips. In addition to the standard pixels, another two kinds of double-sized pixels in-between the lateral fields indicated on the bottom of figure 14.1. The size of these pixel layouts is 400 μm $\times$ 200 μm, and the gap, metal overhang and radius of p^+ implants and metal layers of these double-sized pixels are the same as those of the standard pixels. The only difference between the two kinds of double-sized pixels is the location of the three octagon layers: The octagons are located at (100,30) for one kind and at (300,30) for another.

The AGIPD wafer The AGIPD sensor will be produced on 6 inch wafers. Each wafer includes 2 AGIPD sensors and a number of test structures for quality-control tests. The layout of the AGIPD wafer and arrangements of sensors and test structures on this wafer are shown in figure 14.5.

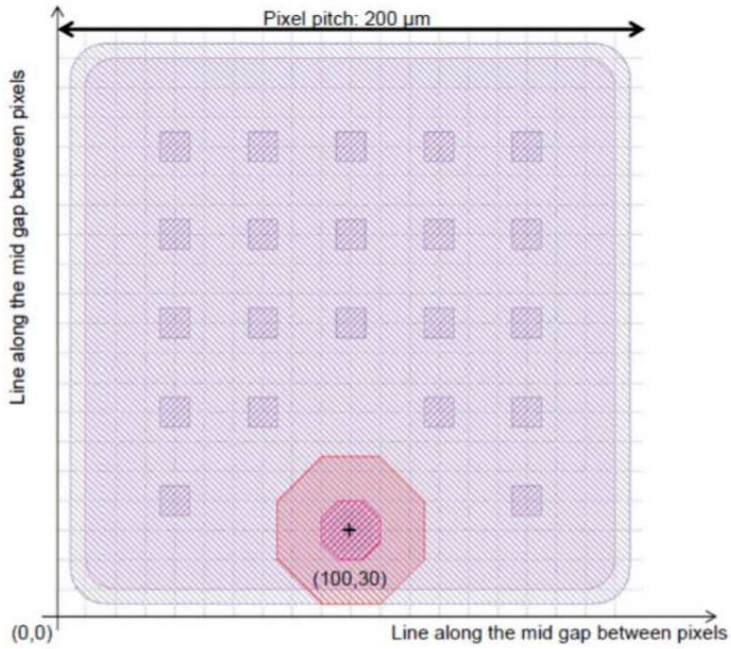

Figure 14.4: Layout and dimensions of the standard 200 μm $\times$ 200 μm pixel.

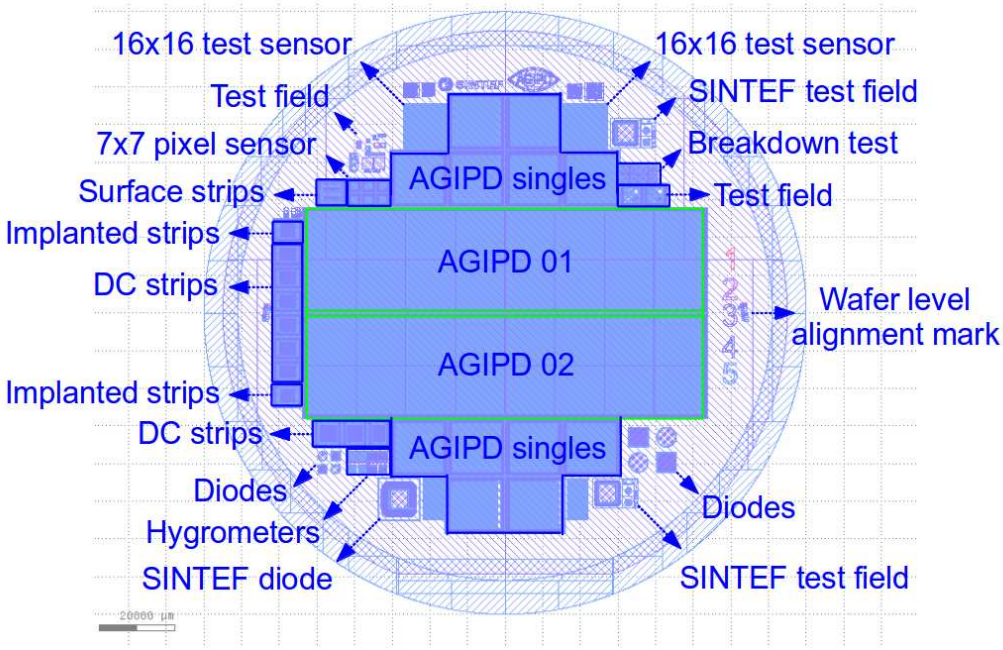

Figure 14.5: Layout of the AGIPD wafer and arrangements of sensors and test structures on the wafer.

The main test structures, planned measurements on the test structures and expected parameters from the measurements are summarized as follow:

- 64 × 64 single sensor: The single sensor will be bump-bonded to the AGIPD 64 × 64 single chip. The switching gain of the ASIC and the functionality of the single chip detector will be tested and qualified.
- 7 × 7 pixel sensor with the same pixel layout and guard-ring structure as the AGIPD sensor: C/I-V measurements will be performed on this sensor, from which the leakage current, breakdown voltage and full depletion voltage can be determined and the results will be used to qualify whether the specifications are met or not. In addition, interpixel capacitance and interpixel resistance will be also measured on the 7 × 7 pixel sensor. According to the values obtained from the measurements, the noise level in the readout signal can be obtained according to the leakage current and interpixel capacitance. The interpixel resistance will be used to judge the isolation between pixels.
- 16 × 16 test sensor: The sensor is designed for the test of previous AGIPD chips (AGIPD-02/03/04 with 16 × 16 pixels).
- DC coupled strip sensors with 200 μm pitch but with different gaps and metal overhangs: C/I-V measurements will be performed in order to obtain the sensor capacitance, leakage current and breakdown voltage of active detection area. In addition, the interstrip capacitance will be measured as function of bias voltage of the DC coupled strip sensors. The measurement results will be used to verify the 2-D simulation results from TCAD with the same geometries and provide an idea on how to improve the sensor performance according to different designs of the DC coupled strip sensors.
- Implanted strips: I-V measurements will be performed on the two sides of the p^+ and n^+ implanted strips. From the measurements, the resistivities of p^+ and n^+ implants can be obtained.
- Surface strips: The structure consists of several aluminium strips. There are two opening through passivation layer at the two ends of each aluminium strip. I-V measurements will be performed on each strips. Then, the resistivity of the metal layer can be obtained.
- Diodes: The diode capacitance and current will be measured as function of bias voltage. From the C-V curve, the doping concentration of Si substrate can be determined; from the value of leakage current at full depletion voltage, the generation lifetime of carriers obtained.
- Test fields with pad diode, MOS capacitor, gate-controlled diode, p-channel MOSFET: From the TDRC and C-V measurements on the MOS capacitor, the distribution of interface-states density and the oxide-charge density can be obtained. The surface-current density will be extracted from the I-V measurement on the gate-controlled diode, and the mobility of minority carriers below the Si-SiO_2 interface determined from the measurement of source-to-drain current as function of gate voltage of the p-channel MOSFET.
- Test diode with different guard-ring design: I-V measurements will be performed and the breakdown voltage of different guard-ring structures determined.

- Hygrometers ("cross-finger" aluminium strips): The structure consists of two groups of finger-like aluminium strips deposited on top of SiO_2 insulating layer. I-V measurement between two groups of strips will be made under different humidity. From the slope of the measurement, the surface resistivity as function of humidity can be obtained.

14.4. Summary

The requirements and challenges of silicon sensors at the European XFEL have been presented in this chapter and the studies of the detector group of Hamburg University on how to meet these challenges have been summarized. To reduce the spread in space and time of the signal due to the plasma effect, it has been found that operating voltages for a 500 μm thick sensor in excess of 500 V are desirable. Charge losses close to the Si-SiO_2 interface have been observed, however their influence on measurements at the XFEL are minor and can most probably be ignored. According to the study on surface-radiation damage, the damage-related parameters were extracted. Using this information, the AGIPD pixel sensor has been optimized with the help of detailed TCAD simulations. The simulations show that the challenging requirements can be met. Based on the optimized process and geometrical parameters, the AGIPD sensor combining the pixel layout and the guard-ring structure has been designed. In addition, a large number of test structures and test sensors have been designed for the quality-control tests. The wafers including the AGIPD sensors and test structures are being fabricated by a semiconductor company.

15. Summary, conclusions and outlook

This chapter will summarize the results presented in the previous chapters and the conclusions drawn from these results.

15.1. Summary and conclusions of this thesis

The methods used to extract the oxide-charge density, the surface-current density and the distribution of interface-states density in the silicon band gap have been introduced in this thesis. For the measurement of the interface-states density, the energy levels of the interface states and their electron-capture cross sections, the thermal dielectric relaxation current technique (TDRC) is employed. It is found that, in order to describe the C/G-V curves according to a model calculation for the MOS capacitor, at least three interface traps are required. The properties of the three dominant interface traps, including their energy levels and full widths at half maximum, are obtained through the TDRC measurements with different heating rates and a χ^2 method. For the extraction of the oxide-charge density, a model describing the irradiated MOS capacitor by an RC-network is used. The model allows the calculation of the capacitance and conductance of a MOS capacitor as function of gate voltage for different frequencies using the measured TDRC signal and the surface density of oxide charges N_{ox} as input. N_{ox}, which just shifts the C/G-V curves along the voltage-axis, is obtained by adjusting its value till the calculated C/G-V curves describe the measurements. In the model calculation, the interface traps, which have been measured by the TDRC technique, are assumed to be acceptors, which gives a maximal estimate for N_{ox}. The surface-current densities are extracted from the I-V measurements on gate-controlled diodes. It is found that due to the reduction of the mobility of minority carriers at the Si-SiO_2 interface and the gate-length effects, the extracted J_{surf} for irradiated GCD gives the minimal estimate. This effects and the methods should be further studied in the future.

Results on the oxide-charge densities, the interface-trap densities and the surface-current densities from MOS capacitors and gate-controlled diodes built on high resistivity n-type silicon with orientations <100> and <111> produced by four vendors, CiS, Hamamatsu, Canberra and Sintef, as function of 12 keV X-ray doses up to 1 GGy have been presented. All of them either saturate or decrease at high doses. The saturation values of N_{ox} and N_{it} for all investigated test fields are in the range from 1.5×10^{12} to 3.8×10^{12} cm^{-2}. The maximal values of J_{surf} are in-between 1.7 and 6.4 μA/cm^2.

The influence of the electric field in the oxide on the formation of oxide charges and interface traps has also been investigated using MOS capacitors and gate-controlled diodes. It is found that both strongly depend on the gate voltage if the electric field

in the oxide points from the gate to the Si-SiO_2 interface. However, if the electric field points from the interface to the gate, little dependence on the strength of the electric field is observed. The investigation has also been made at the "saturation" dose of 100 MGy: If the electric field points to the interface, an increase of N_{ox}, N_{it} and J_{surf} is still observed. It means that the saturation of radiation-induced defects from the study of dose dependence is temporary and established under certain condition.

Annealing studies were performed at 60 °C and 80 °C on MOS capacitors and gate-controlled diodes irradiated to 5 MGy. The annealing kinetics of oxide charges and surface current are determined: Both can be described by "power-law" functions. The "power-law" functions for $N_{ox}(t)$ and $J_{surf}(t)$ are explained by a modified "tunnelling model" and the "two reaction model". The values of parameters like the activation energies and the time constants are determined. Based on the parameters, it is predicted that the annealing of oxide charges is a very slow process and the annealing of surface current is relatively fast compared to oxide charges: For example at 20 °C, N_{ox} is reduced by 50% after 3 years however J_{surf} reduced by 50% just in 5 days.

The electrical properties of segmented (microstrip) sensors have also been characterized as function of X-ray dose. After irradiation, an electron-accumulation layer forms in the gap region between neighbouring p^+ implants below the Si-SiO_2 interface, which results in an increase of the full depletion voltage $\sim$ 10 V. In addition, it is found that the leakage current linearly increases with bias voltage, which is explained by the change of the size of accumulation layer. The reduction of the size of the accumulation layer with bias voltage causes the increase of the depleted interface area between the p^+ implants and the accumulation layers. The interface traps located at the depleted interface area are exposed to the electric field and generate leakage currents. An increase of interstrip capacitance after irradiation is also found, whose value is a function of bias voltage and thus influenced by the accumulation layer. Moreover, the electrical properties of segmented sensors irradiated under different biasing conditions have been compared. The leakage current and interstrip capacitance of the sensor irradiated with 35 V bias are higher than the values of the sensor irradiated without bias. However, the differences are small and further reduced with increasing bias voltage. This agrees with the observation from the study on the electric field dependence. The frequency dependence of the sensor capacitance, coupling capacitance and interstrip capacitance and their corresponding real parts are simulated with a SPICE model. Results show that the SPICE model consisting of a RC network for the AC coupled microstrip sensor is able to reproduce the result of the frequency-dependent measurements.

Finally, based on the previous described studies for the AGIPD sensor and the TCAD simulation results taking radiation-damage effects into account, the pixel layout and the guard-ring structure for the AGIPD sensor have been optimized. The AGIPD sensor, together with large number of test structures, have been designed and ready for fabrication.

15.2. Relevance of this study for AGIPD

The central parts of this thesis are the studies of X-ray induced radiation damage and design of a radiation-hard silicon sensor for the AGIPD for the European XFEL.

The study on the dose dependence of N_{ox}, N_{it} and J_{surf} provides a basic understanding on the radiation-induced defects in SiO_2 and at the Si-SiO_2 interface. The extracted values are the main parameters used in TCAD simulation for the sensor optimization.

The study on the electric field dependence provides insight into the electrical properties of the AGIPD sensor with irradiations. The AGIPD sensor is a p^+ on n sensor, whose electric field in the SiO_2 points from the interface to the electrode. Hence, no significant increase of N_{ox}, N_{it} and J_{surf}, compared to the values obtained from the study on dose dependence, is expected at the saturation dose according to this study. Thus, the selection of a p^+n sensor for the AGIPD is a reasonable choice considering the radiation effects.

The annealing study confirms the long-term stability of the AGIPD sensor. After irradiation to high doses, the electrical properties (except for the leakage current) of the AGIPD sensor will not change quickly (stable operation) due to the long annealing time of the oxide charges. The quick reduction of the surface current may help to improve the noise level.

The performance of the segmented (microstrip) sensors with irradiations partly reflect the performance of the AGIPD sensor. All the measurements from the microstrip sensors can be understood qualitatively.

15.3. Suggestions for future studies and summary of remaining problems

A saturation mechanism of oxide charges and interface traps has been discussed. To understand this in details, especially to investigate those factors influencing the saturation dose and saturation value of oxide charges and interface traps, a study on modelling the formation of the oxide charges and interface traps is required.

The types of the three dominant interface traps, whether they are acceptors and donors, are still not clear. Other experimental techniques, for example the electron-spin resonance (ESR), are required to answer this question. In addition, the TDRC signal due to D_{it}^3 whether it is caused by the emission or the generation process of interface traps could not be classified. A cross check with other methods is required.

The model for the irradiated MOS capacitor used to extract the oxide-charge density ignores the communication of interface states with the valence band. The approximation is appropriate when the hole-capture rate is much smaller than the electron-capture rate. A resistor bridging the interface states and the valence band in the RC-circuit model should be implemented in the future.

A gate-length dependence of the extracted surface-current density from the gate-controlled diode has been observed and can be described by introducing a critical gate length. However a systematic study requires a number of gate-controlled diodes with different gate lengths.

Although certain progress has been made in the thesis towards the understanding of X-ray induced radiation damage in silicon sensors up to the GGy regime, it is still far from an in-depth understanding. The remaining problems can be shortly summarized as follows: (1) The types of the interface traps introduced by X-ray irradiation, whether acceptors or donors, are not determined. Different assumptions on the type of an interface trap used in the model calculation influences the extracted values of N_{ox}. (2) The TDRC signal, especially the signal at $\sim$ 225 K, whether it is caused by emission or generation current of an interface trap cannot be distinguished. (3) The type and concentration of interface traps located in the lower half of the silicon band gap are unknown and cannot be seen by TDRC measurement. (4) The measured I-V curve from a gate-controlled diode can not be reproduced by the distribution of interface-states density due to the lack of information on the capture cross section of electrons and holes, and the mobility of minority carriers below the Si-SiO_2 interface. Solving the fore-mentioned problems in future studies will provide more insights to deeper understandings of X-ray induced radiation damage.

Appendix

A. Extensive C/G-V, I-V and TDRC measurements

A.1. Summary of investigated test structures for dose dependence study

The investigated test structures in the study of dose dependence of radiation-induced defects are summarized in table A.1.

Label	CE2250	CB0450
Producer	CiS	CiS
Doping	7.6×10^{11} cm^{-3}	1.1×10^{12} cm^{-3}
Insulator	330 nm SiO_2 + 50 nm Si_3N_4	360 nm SiO_2 + 50 nm Si_3N_4
Gate area of MOS	1.767×10^{-2} cm^{-2}	1.767×10^{-2} cm^{-2}
Gate area of GCD	1.665×10^{-3} cm^{-2}	1.665×10^{-3} cm^{-3}
Label	6336-01-03	HAMA-04
Producer	CiS	Hamamatsu
Doping	7.8×10^{13} cm^{-3}	9.0×10^{11} cm^{-3}
Insulator	335 nm SiO_2	700 nm SiO_2
Gate area of MOS	1.767×10^{-2} cm^{-2}	1.767×10^{-2} cm^{-2}
Gate area of GCD	1.665×10^{-3} cm^{-2}	1.665×10^{-3} cm^{-3}
Label	Canberra-145/7	Sintef-1/2/3
Producer	Canberra	Sintef
Doping	6.2×10^{11} cm^{-3}	3.0×10^{11} cm^{-3}
Insulator	250 nm SiO_2	750 nm SiO_2
Gate area of MOS	1.767×10^{-2} cm^{-2}	3.5×10^{-2} cm^{-2}
Gate area of GCD	7.1×10^{-3} cm^{-2}	4.024×10^{-3} cm^{-2}

Table A.1: Summary of the parameters of investigated test structures.

A.2. C/G-V, I-V and TDRC of the non-irradiated test fields

Figure A.1-A.6 show the C/G-V, I-V and TDRC curves measured from the non-irradiated test fields.

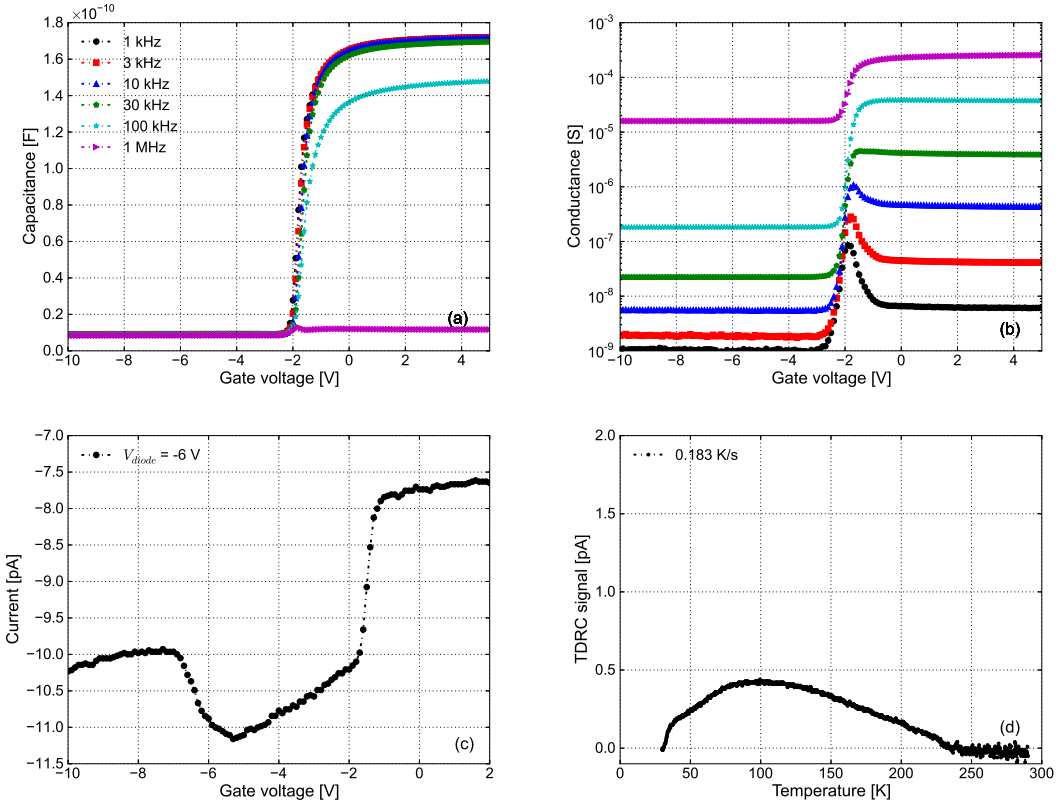

Figure A.1: Measurements on the non-irradiated CE2250 fabricated by CiS: (a) C-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of gate-controlled diode for V_{diode} = -6 V scaled to 20 °C. (d) TDRC spectrum of MOS capacitor.

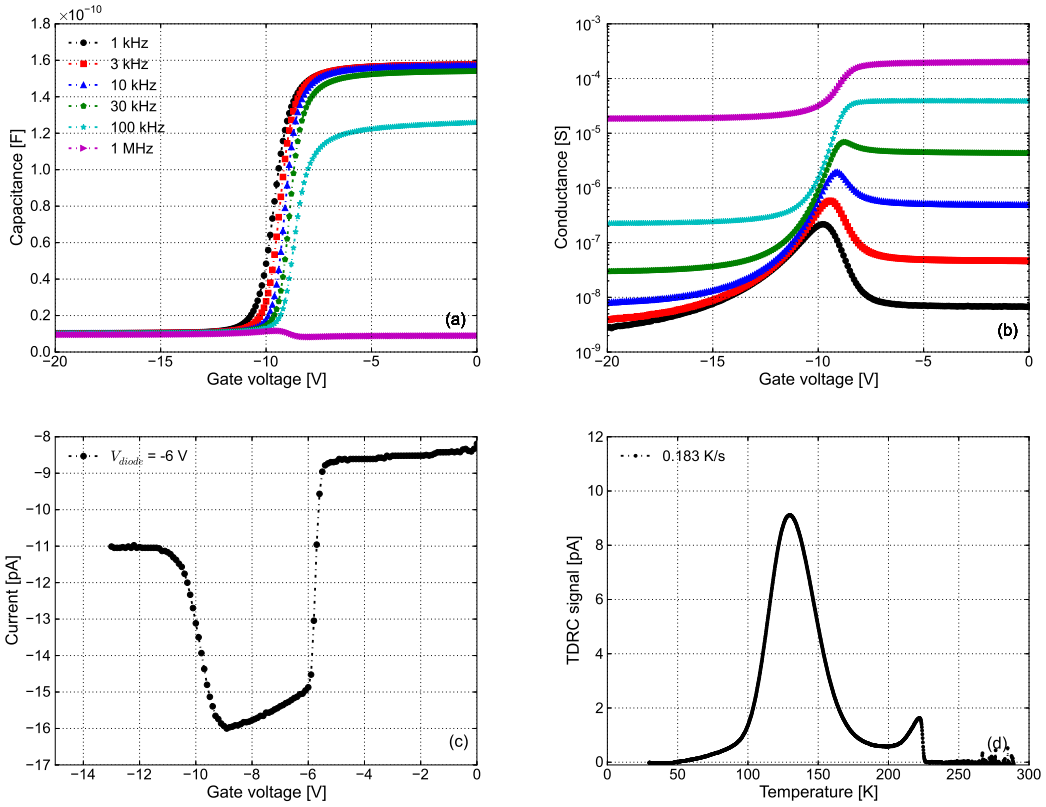

Figure A.2: Measurements on the non-irradiated CB0450 fabricated by CiS: (a) C-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of gate-controlled diode for V_{diode} = -6 V scaled to 20 °C. (d) TDRC spectrum of MOS capacitor.

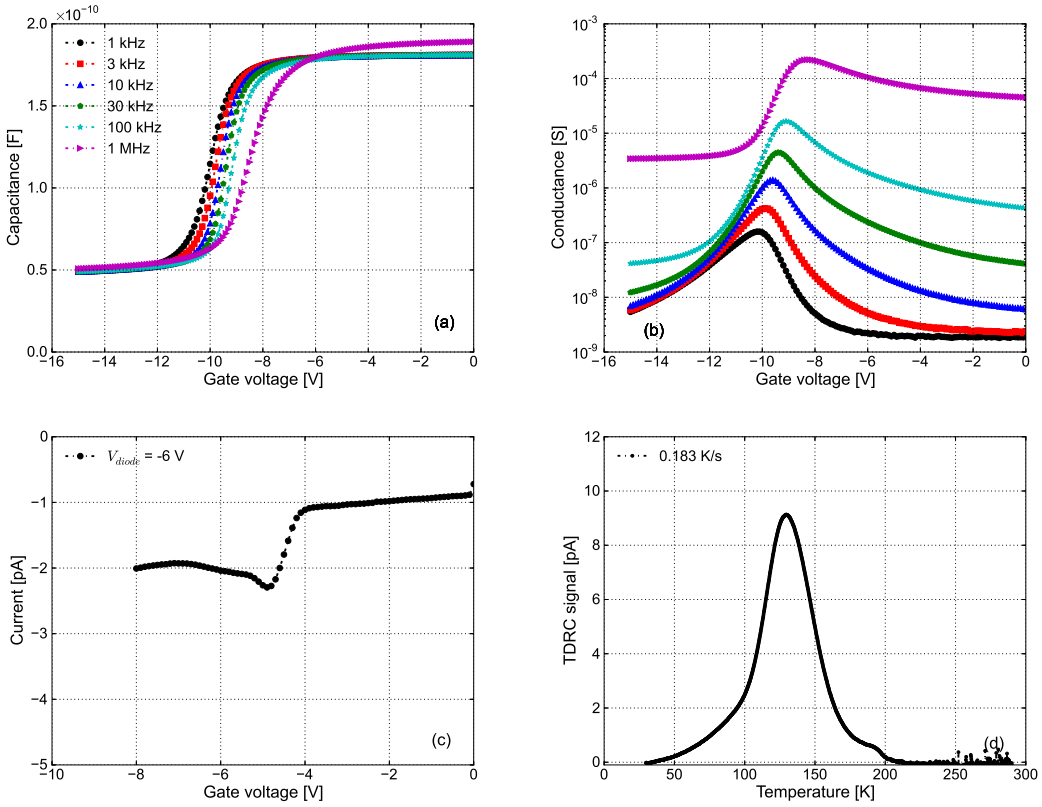

Figure A.3: Measurements on the non-irradiated 6336-01-03 fabricated by CiS: (a) C-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of gate-controlled diode for V_{diode} = -6 V scaled to 20 °C. (d) TDRC spectrum of MOS capacitor.

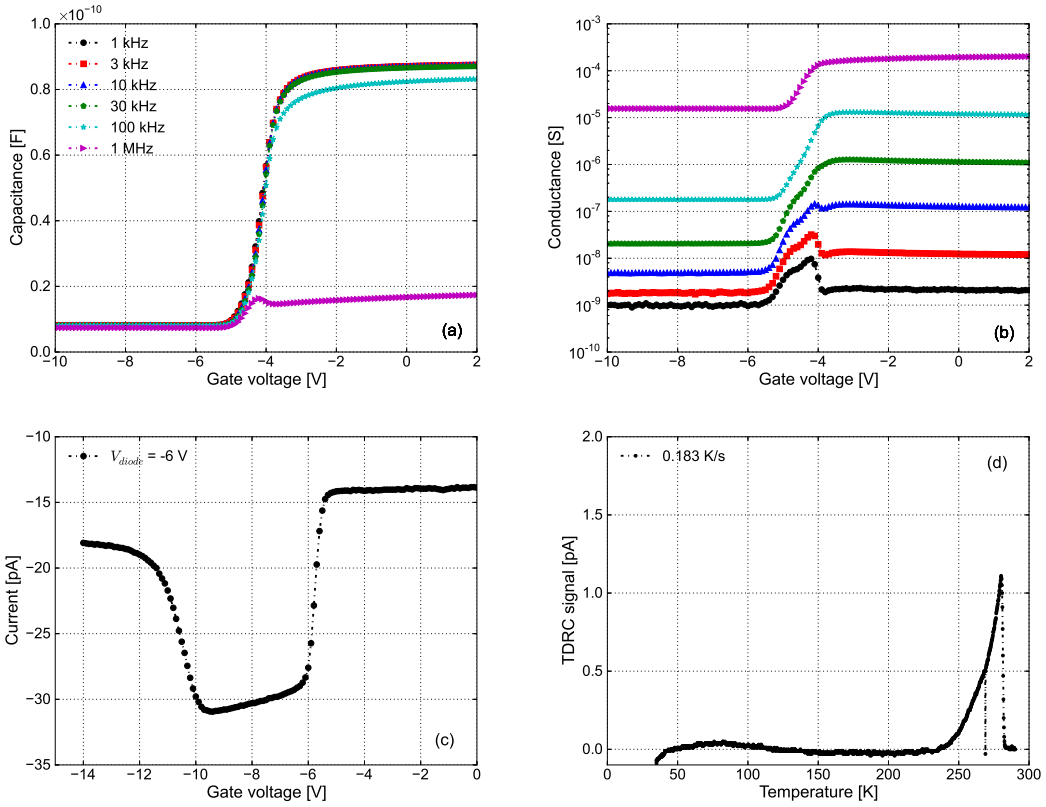

Figure A.4: Measurements on the non-irradiated test field fabricated by Hamamatsu: (a) C-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of gate-controlled diode for V_{diode} = -6 V scaled to 20 °C. (d) TDRC spectrum of MOS capacitor.

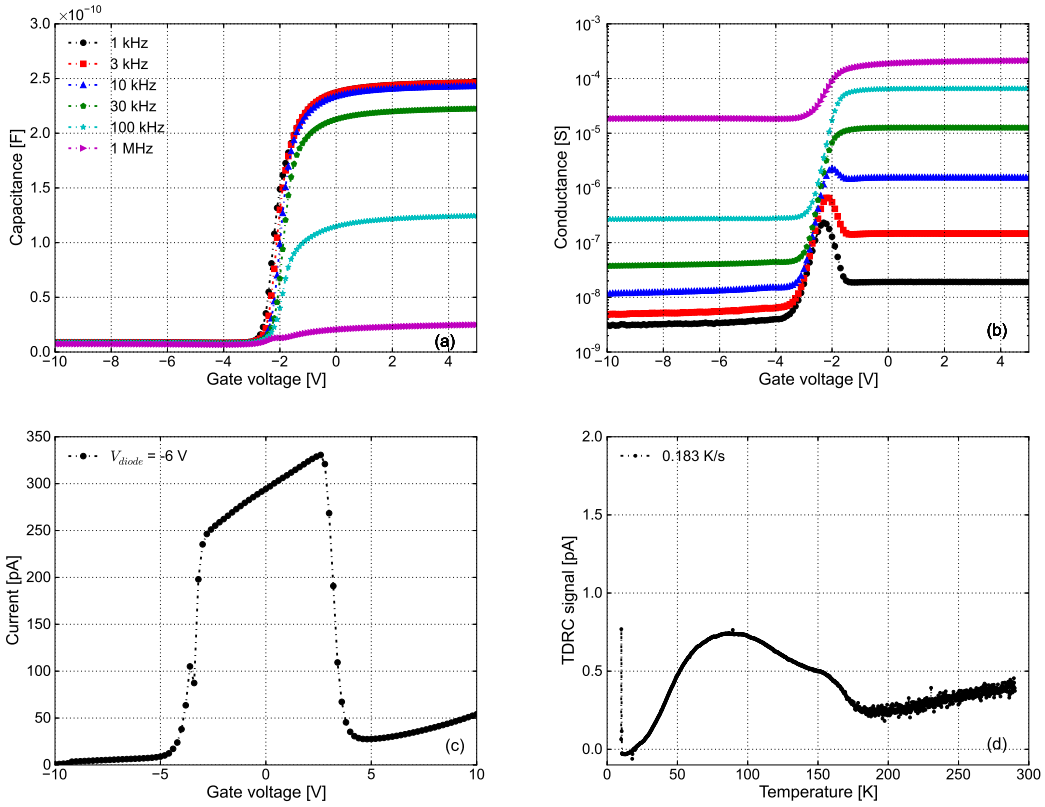

Figure A.5: Measurements on the non-irradiated test field fabricated by Canberra: (a) C-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of gate-controlled diode for V_{diode} = -6 V scaled to 20 °C. (d) TDRC spectrum of MOS capacitor.

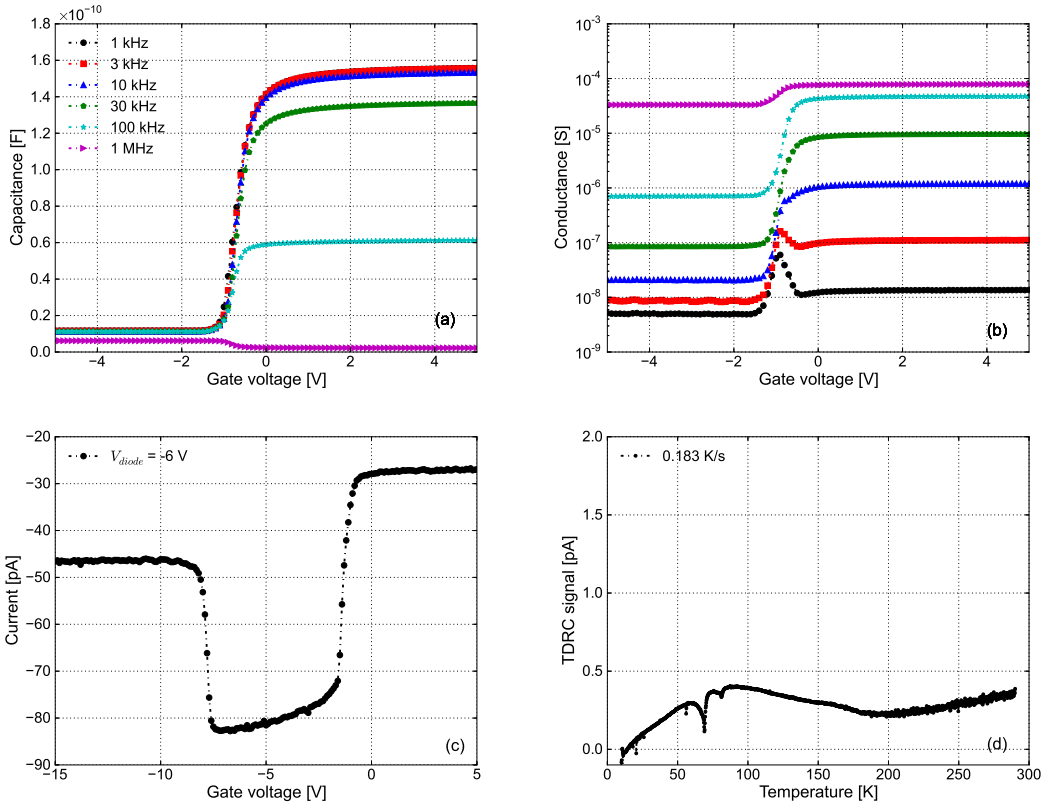

Figure A.6: Measurements on the non-irradiated test field fabricated by Sintef: (a) C-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (b) G-V curves of MOS capacitor for frequencies of 1, 3, 10, 30, 100 kHz and 1 MHz. (c) I-V curves of gate-controlled diode for V_{diode} = -6 V scaled to 20 °C. (d) TDRC spectrum of MOS capacitor.

A.3. C/G-V, I-V and TDRC of the irradiated test fields

Figure A.7-A.9 show the C/G-V, I-V and TDRC curves measured from the test fields irradiated to different doses.

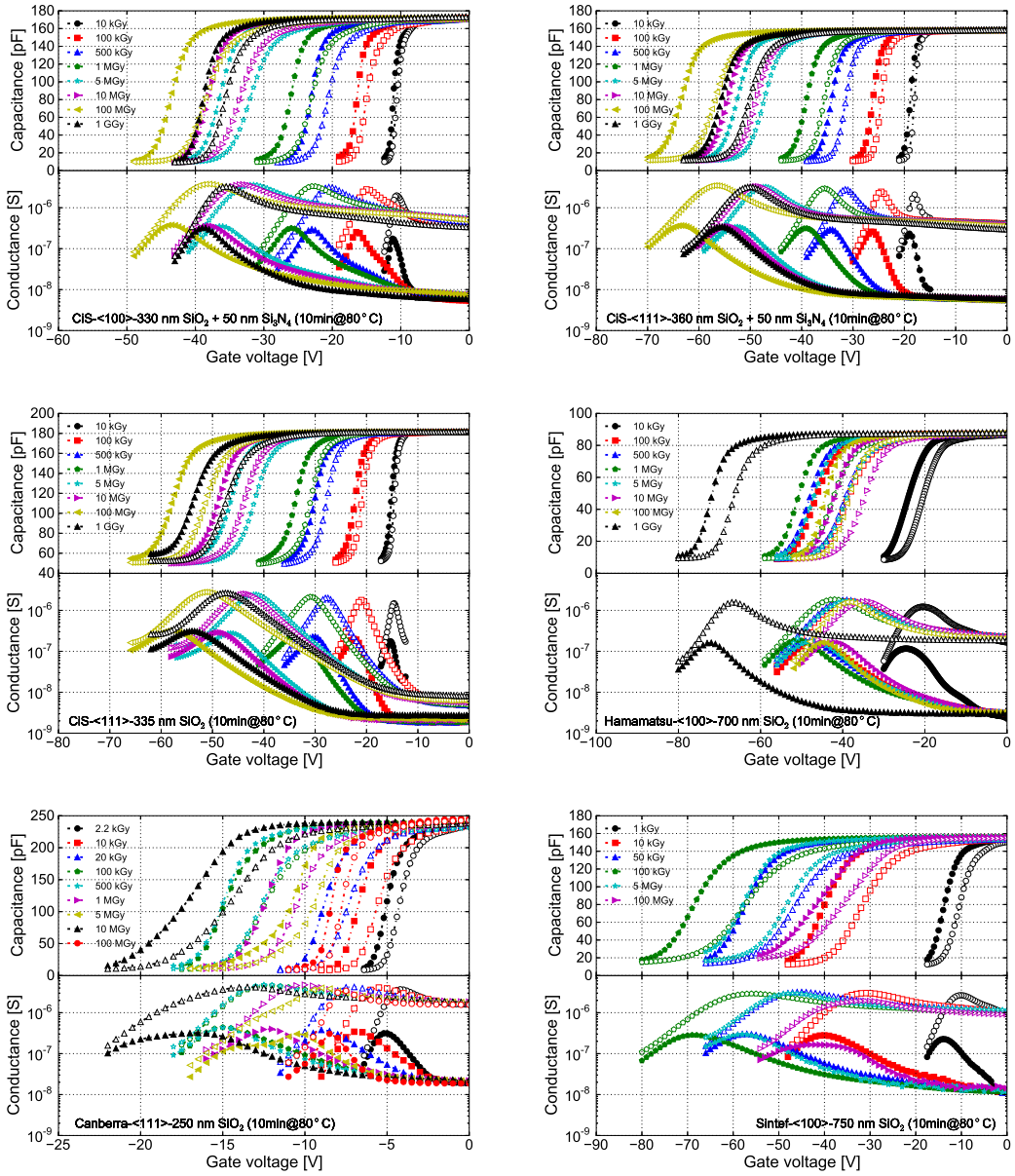

Figure A.7: Measurements of C/G-V curves on irradiated MOS capacitors.

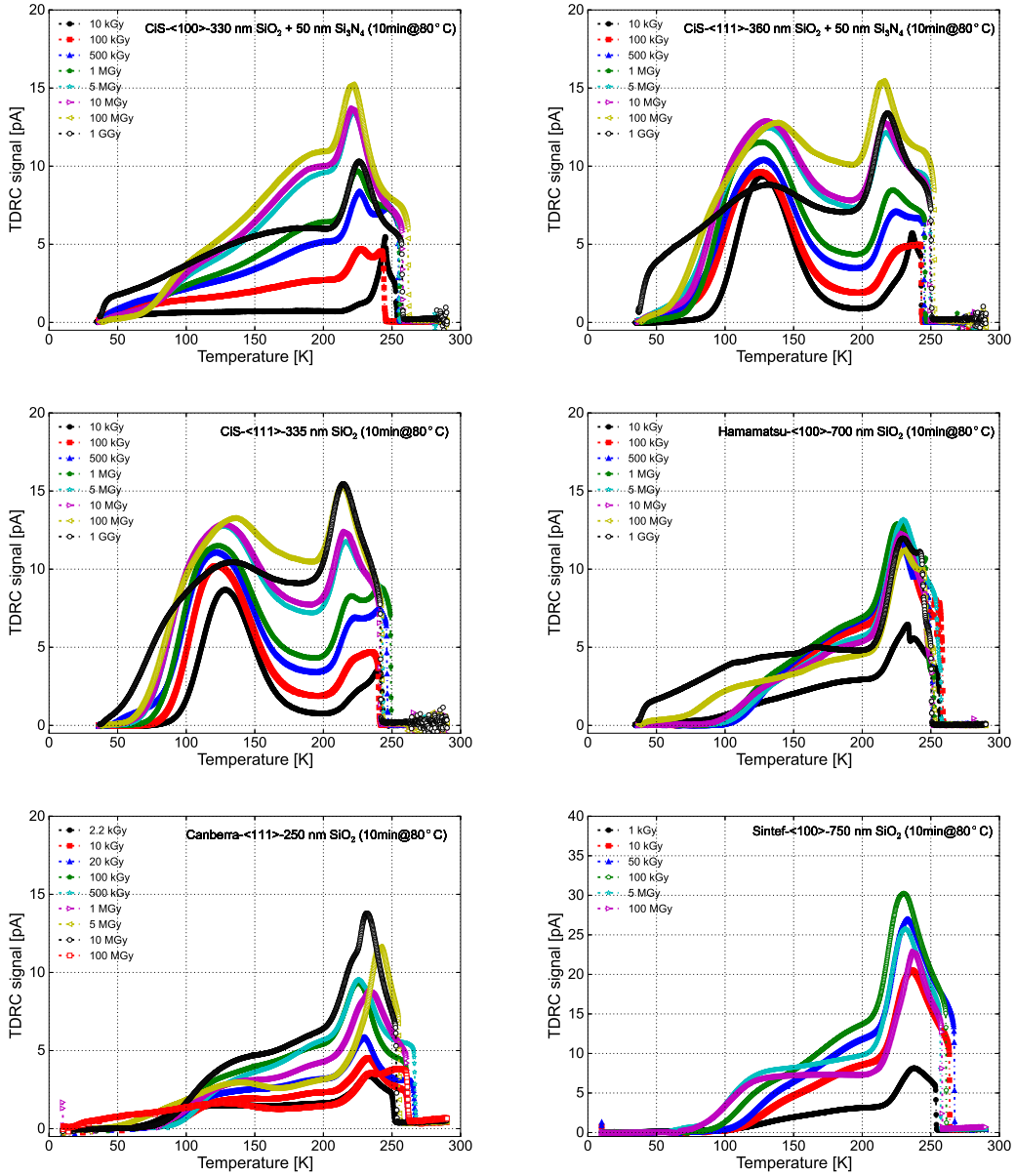

Figure A.8: Measurements of TDRC spectra on the irradiated MOS capacitors.

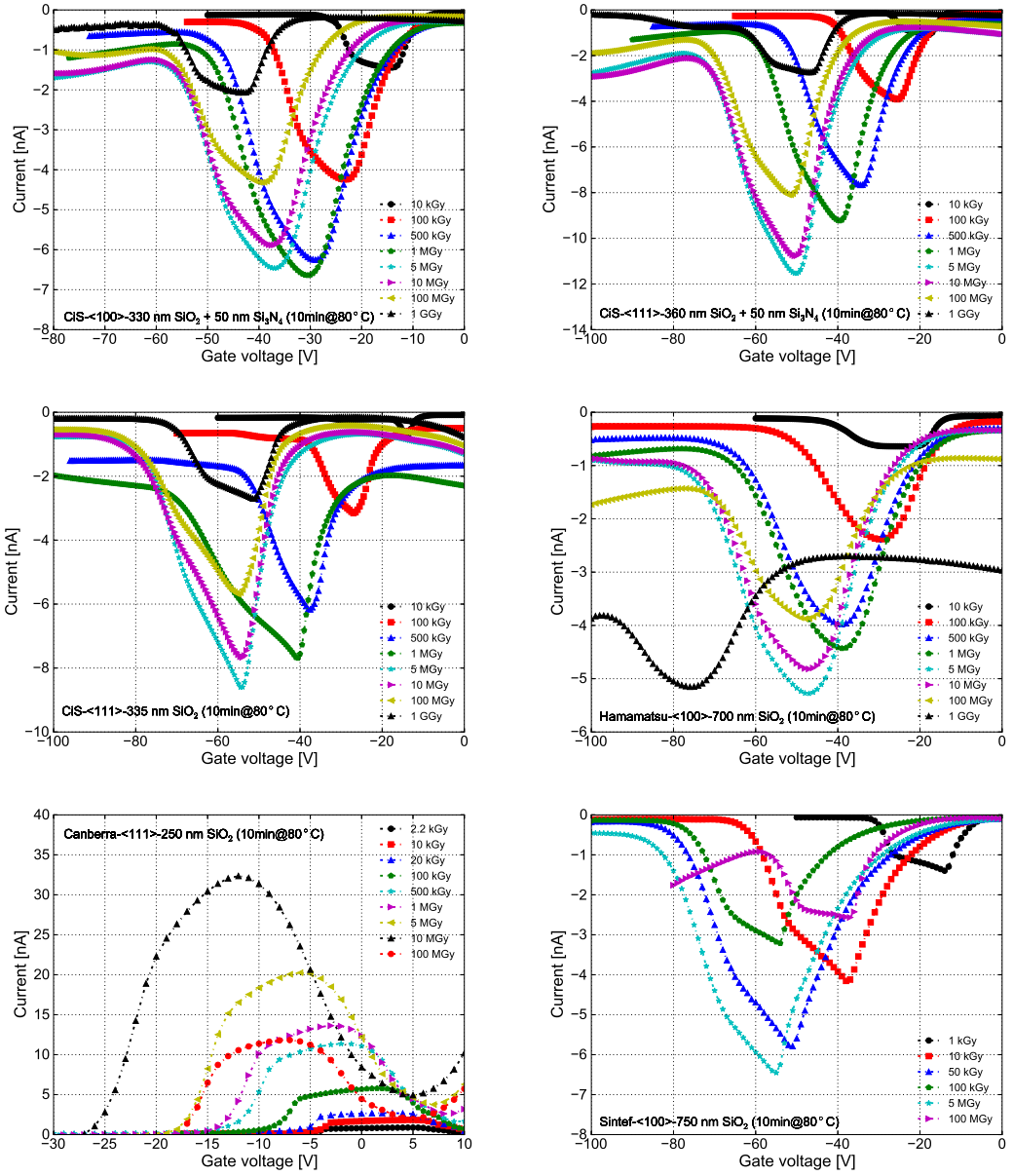

Figure A.9: Measurements of I-V curves on irradiated gate-controlled diodes. The currents have been scaled to their values at 20 °C.

A.4. Results of N_{ox}, N_{it} and J_{surf} as function of dose

The results of N_{ox}, N_{it} and J_{surf} as function of dose for different test fields produced by CiS, Hamamatsu, Canberra and Sintef are summarized in the following.

	N_{ox} [cm^{-2}]	$C_{ox}V_{fb}^{1\,\mathrm{kHz}}/q_0$ [cm^{-2}]	N_{it} [cm^{-2}]	J_{surf} [μA/cm^2]
10 kGy	7.3×10^{11}	7.0×10^{11}	3.7×10^{11}	0.82
100 kGy	1.1×10^{12}	1.1×10^{12}	8.5×10^{11}	2.4
500 kGy	1.6×10^{12}	1.5×10^{12}	1.6×10^{12}	3.6
1 MGy	1.8×10^{12}	1.7×10^{12}	1.8×10^{12}	3.8
5 MGy	2.4×10^{12}	2.3×10^{12}	2.4×10^{12}	3.7
10 MGy	2.6×10^{12}	2.4×10^{12}	2.5×10^{12}	3.4
100 MGy	2.9×10^{12}	2.8×10^{12}	2.9×10^{12}	2.5
1 GGy	2.6×10^{12}	2.5×10^{12}	2.1×10^{12}	1.1

Table A.2: Dose dependence of N_{ox}, N_{it} and J_{surf} for CE2250 (CiS-<100>-FZ) after annealing at 80 °C for 10 minutes. J_{surf} has been scaled to values at 20 °C.

	N_{ox} [cm^{-2}]	$C_{ox}V_{fb}^{1\,\mathrm{kHz}}/q_0$ [cm^{-2}]	N_{it} [cm^{-2}]	J_{surf} [μA/cm^2]
10 kGy	1.1×10^{12}	1.1×10^{12}	1.1×10^{12}	0.61
100 kGy	1.7×10^{12}	1.5×10^{12}	1.6×10^{12}	2.2
500 kGy	2.1×10^{12}	2.0×10^{12}	2.1×10^{12}	4.3
1 MGy	2.4×10^{12}	2.3×10^{12}	2.4×10^{12}	5.2
5 MGy	3.2×10^{12}	3.1×10^{12}	3.2×10^{12}	6.4
10 MGy	3.2×10^{12}	3.2×10^{12}	3.3×10^{12}	6.0
100 MGy	3.7×10^{12}	3.7×10^{12}	3.8×10^{12}	4.6
1 GGy	3.4×10^{12}	3.2×10^{12}	3.2×10^{12}	1.6

Table A.3: Dose dependence of N_{ox}, N_{it} and J_{surf} for CB0450 (CiS-<111>-DOFZ) after annealing at 80 °C for 10 minutes. J_{surf} has been scaled to values at 20 °C.

	N_{ox} [cm^{-2}]	$C_{ox}V_{fb}^{1\,\mathrm{kHz}}/q_0$ [cm^{-2}]	N_{it} [cm^{-2}]	J_{surf} [μA/cm^2]
1 kGy	5.0×10^{11}	4.4×10^{11}	4.9×10^{11}	0.34
10 kGy	1.3×10^{12}	1.2×10^{12}	1.3×10^{12}	1.0
50 kGy	1.9×10^{12}	1.7×10^{12}	1.9×10^{12}	1.4
100 kGy	2.2×10^{12}	2.0×10^{12}	2.1×10^{12}	-
5 MGy	2.0×10^{12}	1.7×10^{12}	1.8×10^{12}	1.6
100 MGy	1.6×10^{12}	1.4×10^{12}	1.5×10^{12}	0.6

Table A.4: Dose dependence of N_{ox}, N_{it} and J_{surf} for Sintef-1/2/3 (Sintef-<100>-FZ) after annealing at 80 °C for 10 minutes. J_{surf} has been scaled to values at 20 °C.

	N_{ox} [cm^{-2}]	$C_{ox}V_{fb}^{1\,\mathrm{kHz}}/q_0$ [cm^{-2}]	N_{it} [cm^{-2}]	J_{surf} [μA/cm^2]
10 kGy	1.1×10^{12}	9.6×10^{11}	9.8×10^{11}	0.38
100 kGy	1.5×10^{12}	1.4×10^{12}	1.5×10^{12}	1.6
500 kGy	2.1×10^{12}	1.9×10^{12}	2.1×10^{12}	2.8
1 MGy	2.4×10^{12}	2.1×10^{12}	2.4×10^{12}	3.4
5 MGy	3.1×10^{12}	2.9×10^{12}	3.0×10^{12}	4.8
10 MGy	3.3×10^{12}	3.1×10^{12}	3.1×10^{12}	4.2
100 MGy	3.8×10^{12}	3.7×10^{12}	3.6×10^{12}	3.2
1 GGy	3.5×10^{12}	3.4×10^{12}	3.4×10^{12}	1.5

Table A.5: Dose dependence of N_{ox}, N_{it} and J_{surf} for 6336-01-03 (CiS-<111>-Epi) after annealing at 80 °C for 10 minutes. J_{surf} has been scaled to values at 20 °C.

	N_{ox} [cm^{-2}]	$C_{ox}V_{fb}^{1\,\mathrm{kHz}}/q_0$ [cm^{-2}]	N_{it} [cm^{-2}]	J_{surf} [μA/cm^2]
10 kGy	1.0×10^{12}	8.1×10^{11}	9.0×10^{11}	0.34
100 kGy	1.6×10^{12}	1.5×10^{12}	1.7×10^{12}	1.3
500 kGy	1.7×10^{12}	1.6×10^{12}	1.7×10^{12}	2.2
1 MGy	1.8×10^{12}	1.6×10^{12}	1.8×10^{12}	2.5
5 MGy	1.7×10^{12}	1.5×10^{12}	1.7×10^{12}	3.0
10 MGy	1.6×10^{12}	1.4×10^{12}	1.5×10^{12}	2.7
100 MGy	1.6×10^{12}	1.4×10^{12}	1.6×10^{12}	1.8
1 GGy	2.5×10^{12}	2.3×10^{12}	2.0×10^{12}	1.5

Table A.6: Dose dependence of N_{ox}, N_{it} and J_{surf} for HAMA-04 (Hamamatsu-<100>-FZ) after annealing at 80 °C for 10 minutes. J_{surf} has been scaled to values at 20 °C.

	N_{ox} [cm^{-2}]	$C_{ox}V_{fb}^{1\,\mathrm{kHz}}/q_0$ [cm^{-2}]	N_{it} [cm^{-2}]	J_{surf} [μA/cm^2]
2.2 kGy	6.6×10^{11}	5.0×10^{11}	5.8×10^{11}	0.12
10 kGy	7.9×10^{11}	6.7×10^{11}	7.0×10^{11}	0.24
20 kGy	8.4×10^{11}	8.6×10^{11}	8.9×10^{11}	0.38
100 kGy	1.6×10^{12}	1.4×10^{12}	1.4×10^{12}	0.80
500 kGy	1.6×10^{12}	1.4×10^{12}	1.4×10^{12}	1.6
1 MGy	1.5×10^{12}	1.2×10^{12}	1.2×10^{12}	2.0
5 MGy	1.6×10^{12}	1.2×10^{12}	1.3×10^{12}	3.0
10 MGy	2.0×10^{12}	1.8×10^{12}	1.9×10^{12}	4.8
100 MGy	9.0×10^{11}	8.0×10^{11}	6.7×10^{11}	1.7

Table A.7: Dose dependence of N_{ox}, N_{it} and J_{surf} for Canberra-145/7 (Canberra-<111>-FZ) after annealing at 80 °C for 10 minutes. J_{surf} has been scaled to values at 20 °C.

A.5. Dose dependence of N_{ox} and J_{surf} before annealing

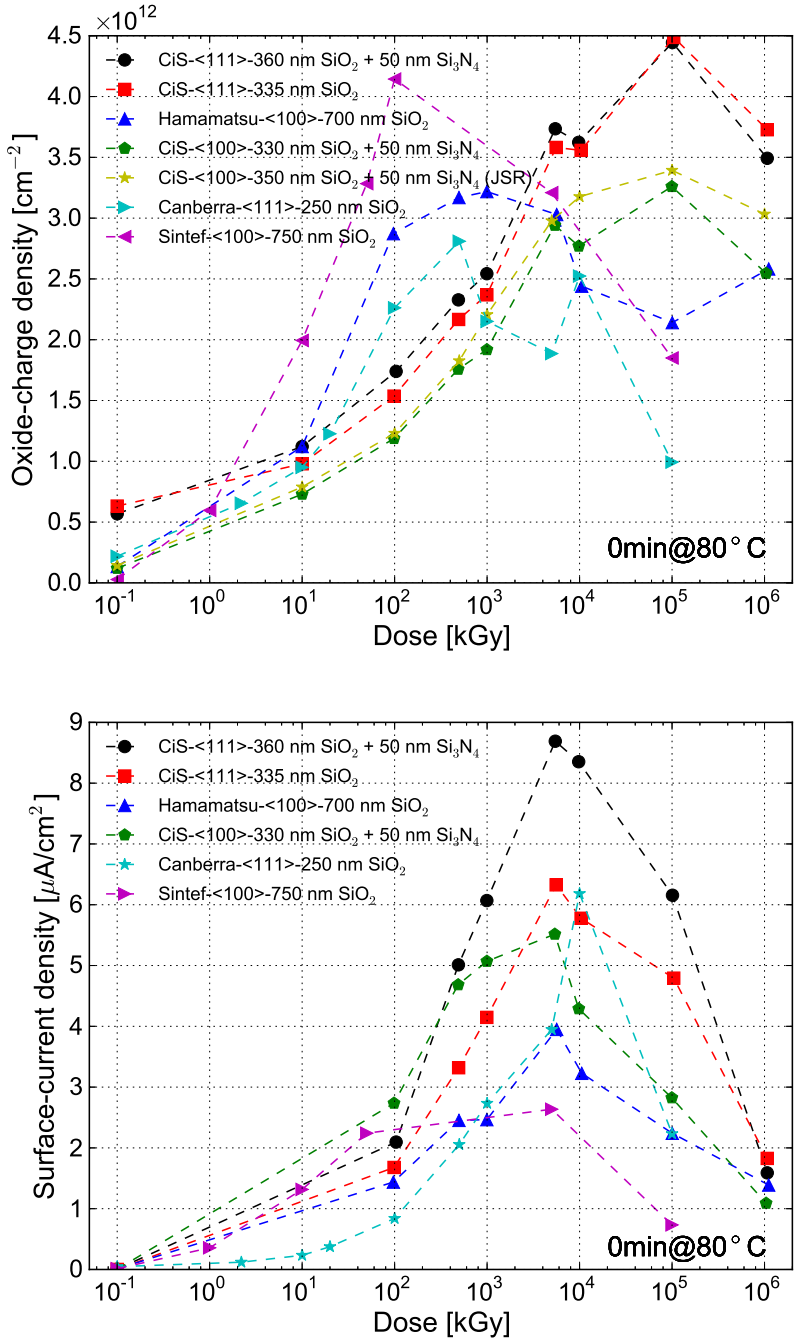

Figure A.10: Dose dependence of N_{ox} and J_{surf} before annealing. Results of N_{ox} and J_{surf} before irradiation are plotted at a dose of 10^{-1} kGy in the figure.

B. Extensive results of electrical properties of p^+n sensors

B.1. Sensor capacitance and resistance versus bias voltage

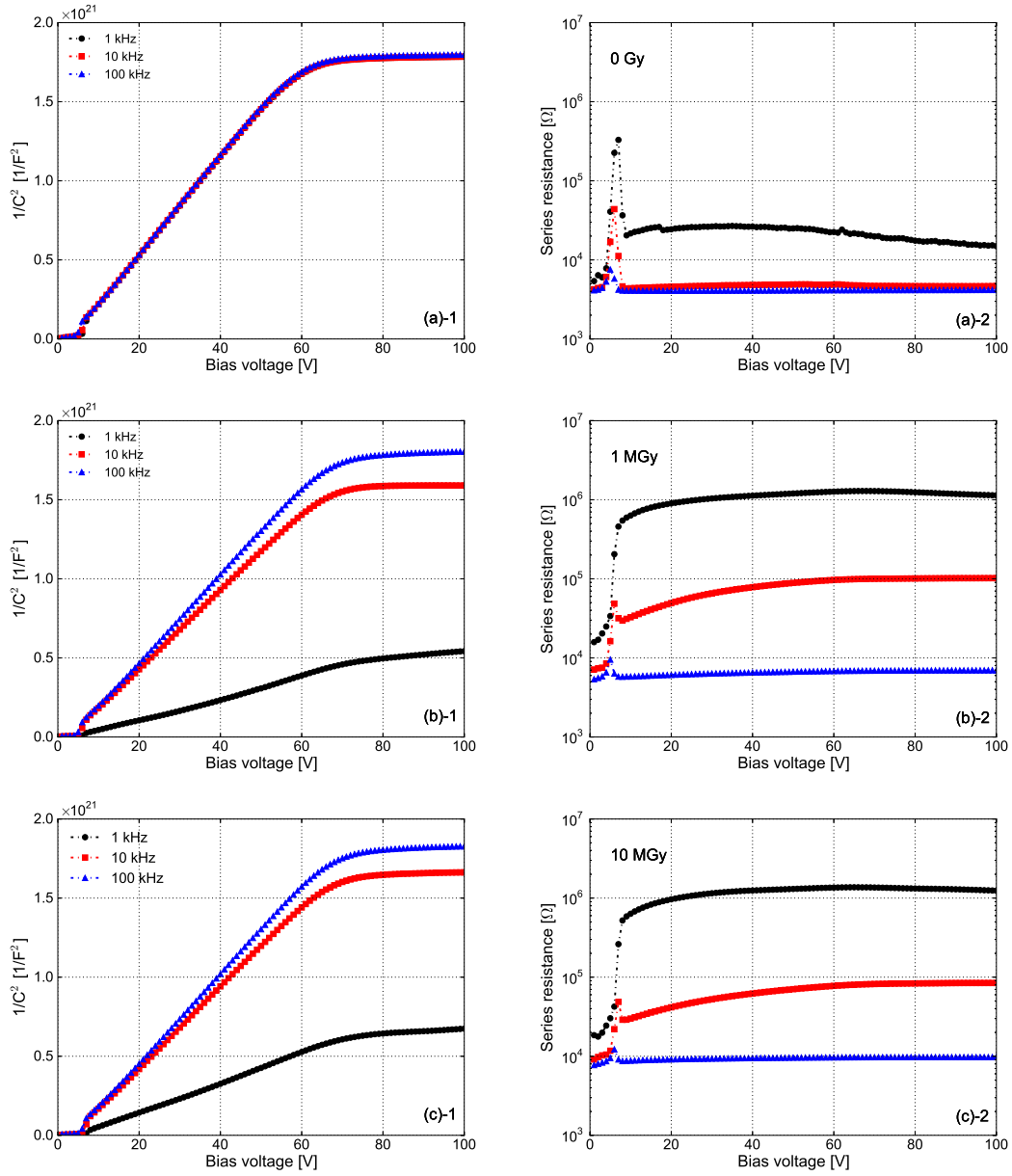

Figure B.1: Sensor capacitance and series resistance vs. bias voltage: (a) 0 MGy; (b) 1 MGy; (c) 10 MGy.

C. The mobility of minority carriers at the interface

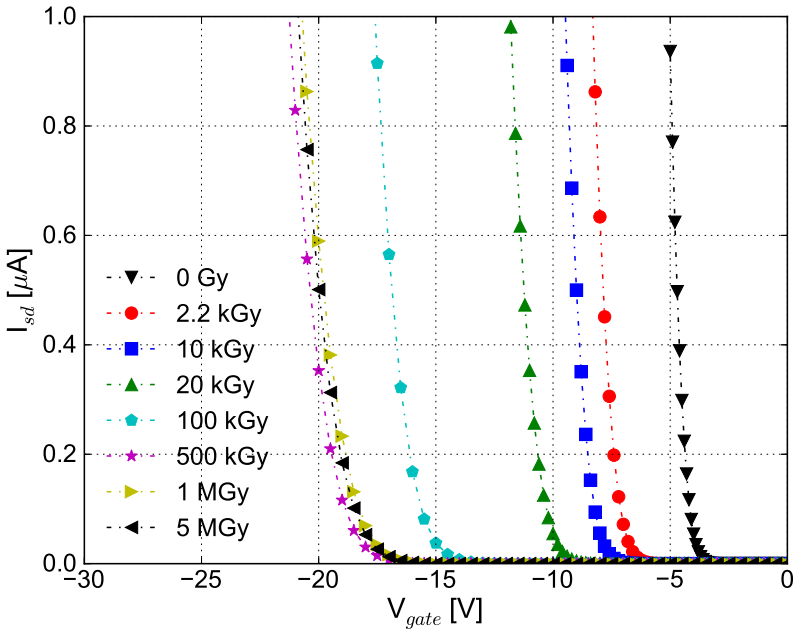

Figure C.1: The source-to-drain current I_{sd} as function of gate voltage V_{gate} of a p-channel MOSFET produced by Canberra for different doses. Measurements were performed after annealing at 80 °C for 10 minutes. The slope in the figure is proportional to the mobility of minority carriers below the Si-SiO2 interface.

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List of Publications

Publications as first/corresponding author

2013	*X-ray induced radiation damage in segmented p^+n silicon sensors*, *Proceeding of Science* (Vertex 2012), 019 (2013).
2012	*Investigation of X-ray induced radiation damage at the Si-SiO_2 interface of silicon pixel sensors for the European XFEL*, *Journal of Instrumentation*, Vol.7, C12012 (2012).
2012	*Study of radiation damage induced by 12 keV X-rays in MOS structures built on high resistivity n-type silicon*, *Journal of Synchrotron Radiation*, Vol.19, Issue.3, 340-346 (2012).
2011	*Study of X-ray radiation damage in silicon sensors*, *Journal of Instrumentation*, Vol.6, C11013 (2011).

Publications with major contributions

2013	*Study of high-dose X-ray radiation damage of silicon sensors*, to be published by *Nuclear Instruments and Methods* A.
2013	*Challenges for silicon pixel sensors at the European XFEL*, to be published by *Nuclear Instruments and Methods* A.
2013	*Study of the accumulation layer and charge losses at the Si-SiO_2 interface in p^+n-silicon strip sensors*, *Nuclear Instruments and Methods* A, Vol.721, 26-34 (2013).
2013	*Design of the AGIPD sensor for the European XFEL*, *Journal of Instrumentation*, Vol.8, C01015 (2013).
2013	*Charge losses in segmented silicon sensors at the Si-SiO_2 interface*, *Nuclear Instruments and Methods* A, Vol.700, 22-39 (2013).
2012	*Optimization of the radiation hardness of silicon pixel sensors for high X-ray doses using TCAD simulation*, *Journal of Instrumentation*, Vol.7, C01006 (2012).

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