AGIPD veto calibration

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Abstract

Calibration is one of the most critical aspects of the Adaptive Gain Integrating Pixel Detector, AGIPD. It is necessary in order to convert the measured voltage into the number of photons with precise accuracy to provide the single photon sensitivity. Also, calibration is important to determine the gain values and the corresponding thresholds and to make offset corrections, to provide the high dynamic range.

In some experiments on the European XFEL the veto implementation could be very useful to get more useful information. The aim of the project is to investigate the influence of the veto on the acquired signal and propose some ideas for further investigation for calibration development in the case of veto implementation.

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1. Introduction

AGIPD or Adaptive Gain Integrating Pixel Detector is a hybrid pixel array detector for measuring X-ray diffraction data from scattering/diffraction experiments.

The specific features AGIPD has are very large dynamic range (from single-photon up to 10^4 12.5keV photons), high sensitivity in the range of small signals, high frame rates, and radiation tolerance [1]. It is necessary to comply with the requirements of the European XFEL (see fig. 1).

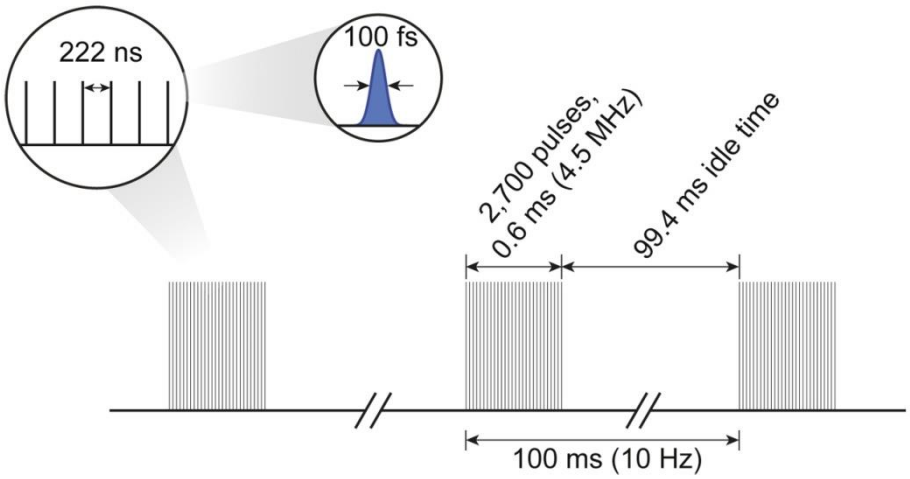

Fig. 1. Time structure of the European XFEL [6].

Due to its features AGIPD is used as an X-ray detector for the SPB/SFX instrument at the European XFEL. The Single Particles, Clusters, and Biomolecules & Serial Femtosecond Crystallography (SPB/SFX) instrument is a tool for studying the structure of biomolecules, atomic and molecular clusters as well as viruses, cells, and novel materials using a variety of X-ray scattering and diffraction techniques. Furthermore, the SPB/SFX instrument allows studying structural dynamics in these biological systems down to the femtosecond timescale.

AGIPD is capable to measure 2D diffraction patterns from single femtosecond X-ray exposure, which is essential for the diffraction-before-destruction approach of serial femtosecond crystallography. Due to its high dynamic range AGIPD allows capturing intense Bragg peaks from crystals as well as low scattering signals from non-crystalline samples [6].

1.1. AGIPD

The AGIPD 1M presented on figure 2 has four movable quadrants, each consisting of 4 modules (see. Fig.2). These can be arranged to form a hole for

the direct beam to prevent it from hitting detector components and damaging the system.

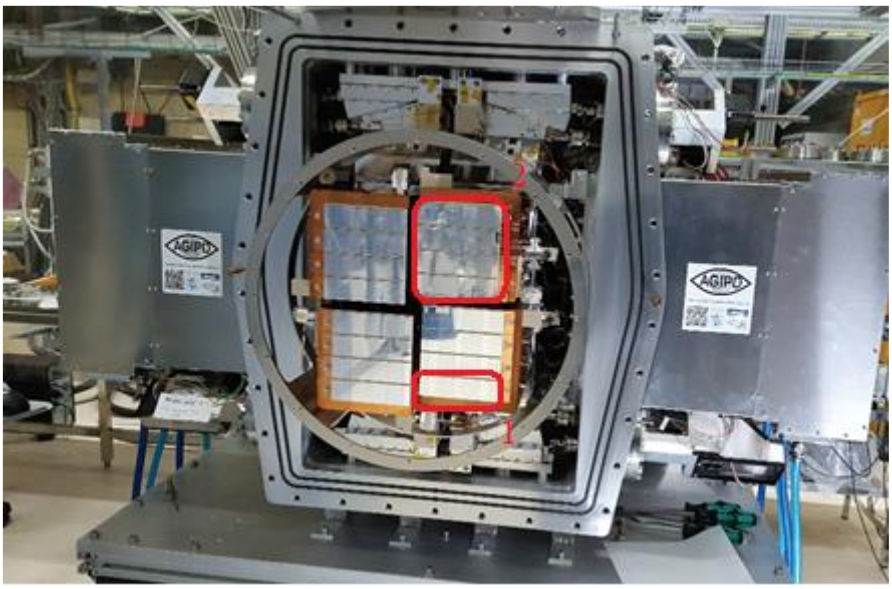

Fig. 2. The AGIPD 1M system installed at the SPB/SFX instrument. The red frames show a module (1) and a quadrant (2) [3].

On the front side of each module a 500 μm thick Si- sensor of 512×128 pixels is placed and to each sensor 8×2 ASICs are bump-bonded for the readout, i.e. each ASIC contains of the readout electronics for 64×64 pixels. The pixel size is 200×200 μm^2.

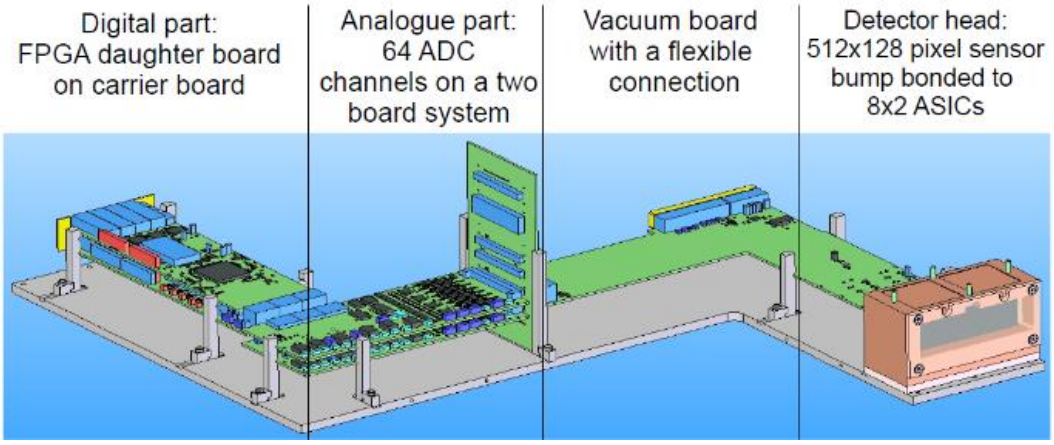

Fig. 3. Structure of the single AGIPD module [3].

1.2. ASIC

Circuit schematic of the Application Specific Integrated Circuit (ASIC) is presented in fig. 4.

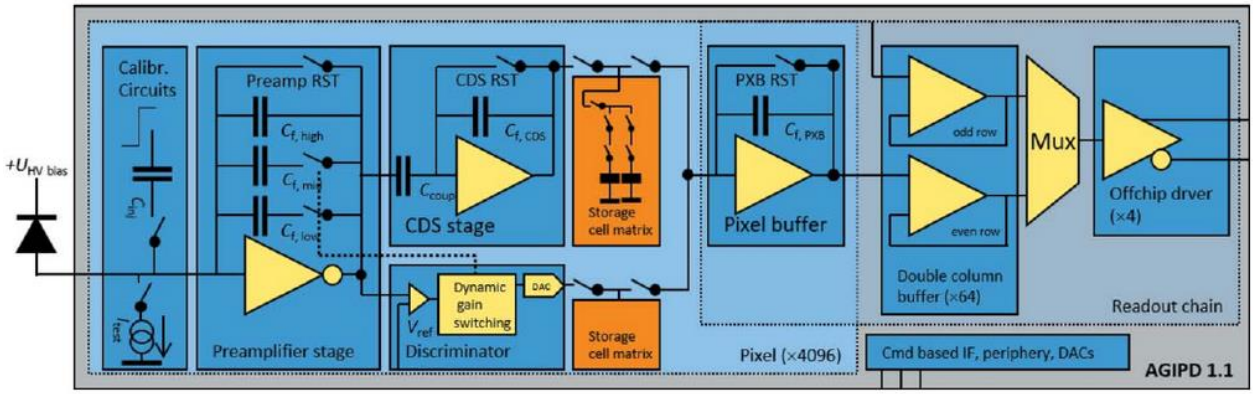

Fig. 4. Schematic of the AGIPD readout ASIC [1].

Charge generated by X-rays in the sensor is integrated by the pre-amplifier. The output of the pre-amplifier is connected to a discriminator which is used to add additional feedback capacitors to the preamplifier, if its output exceeds defined amplitude. This way the sensitivity of the preamplifier is adaptively decreased and the dynamic range is extended. The feedback capacitances provide three gain settings.

The output of the pre-amplifier is also connected to the correlated double sampling stage (CDS), which removes the reset noise and suppresses the low frequency noise contribution.

From the CDS output the signal is written to the analogue memory cell matrix. Since it is not possible to read out an image within 220 ns, the detector has to record as many images as possible during a pulse train and read these out during the 99.4 ms gap in-between the trains.

The ASIC incorporates two sets of 352 analog memory cells per pixel, allowing also to store 3 voltage levels corresponding to the selected gain. It is operated in random-access mode at 4.5 MHz frame rate, providing the option for overwriting images or a frame selective readout. Since the memory occupies about 80% of the pixel area (fig. 5) the number of cells was chosen as a compromise between pixel size and memory capability.

Between the bunch trains, the stored charges are read out via the pixel buffer, column buffer, multiplexer and off-chip driver.

Pixel buffers connect to one of the two readout buses per pixel column, which serve the pixels of even and odd rows respectively. The pixel matrix is subdivided in 4 blocks of 16×64 pixels, operating in parallel. Each of these blocks connects to a multiplexer and output buffer [1, 4].

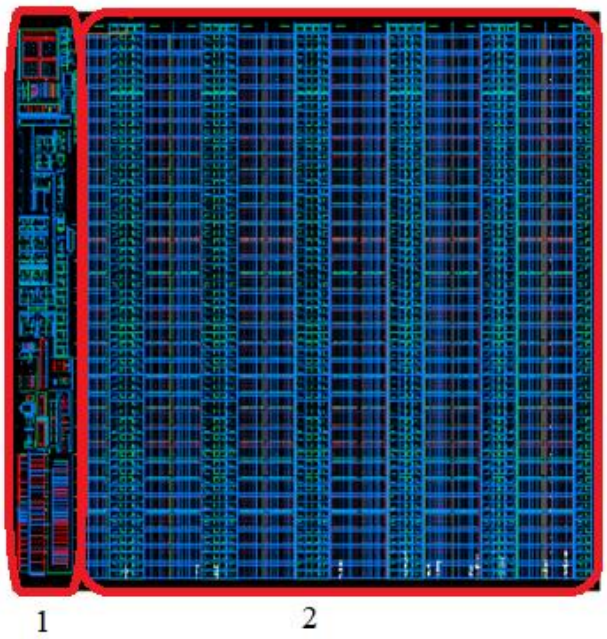

Fig. 5. Layout of the AGIPD's pixel. The red frames mark the analogue circuitry (1), and the matrix of 32×11 memory cells (2) [4].

1.3. Calibration

One of the most critical aspects of AGIPD is its calibration. In order to achieve the large dynamic range and enable single photon resolution, there are three different gains that are dynamically switched depending on the measured intensity. Therefore, each memory cell of each pixel contains two values: the analogue signal and the gain state signal.

The goal of calibration is to guarantee the accuracy and quality of measurements recorded using the detector. Since the measured value - voltage needs to be converted into the number of photons, it's very important to provide the precise calibration to be able to achieve single photon sensitivity in experiments with low photon density. The other issue is that signals recorded in the memory cells are influenced by different offsets and gain values for each gain state, and also by noise from the electronics. In order to get the real incoming X-ray signal from the value that is being read out from the pixels and memory cells, the calibration corrections have to be applied. For that purpose the ASICs include two internal calibration sources for electrical calibration – a current source and a pulsed capacitor. The internal current source allows sampling all three gain levels by injecting a constant current to the input of the pre-amplifier while changing the integration time.

The pulsed capacitor scans the dynamic range by gradually increasing the applied voltage while keeping the integration time constant. The encoded gain

state (three values) and the corresponding discrimination thresholds (two values) can be extracted from both current source and pulsed capacitor scans.

The absolute gain value of the high-gain state is measured for each pixel using characteristic X-rays, for instance X-ray tube Mo. Then the internal current sources allow extrapolation of the absolute calibration of the high-gain state to the others.

For each gain state the offsets (three values) also have to be determined. These measurements are performed without illumination (using dark frames).

All of these eight parameters are independent for each memory cell of each pixel and give in total for each module more than 23×10^6 calibration constants. Since it is possible to use on-chip calibration sources for relative cross-calibration, the gains within a pixel can be treated as correlated. It results in reducing the number of parameters and time needed for calibration.

1.4. Data acquisition

Data from the detector is acquired by sending commands to the ASICs and digitizing its analogue output. The analogue signal from each off-chip driver arrives at one of 64 ADC channels per module. ADCs provide digitization of the data with 14 bit quantization. After the conversion the data is acquired by the FPGA on the digital board. The digital board forms the TCP/UDP packets of the digitized data and sends them to the data acquisition system via a 10 GB ethernet link [1].

2. Calibration procedure

2.1. Veto implementation

The random access mode implemented in the ASIC allows rewriting selected memory cells. This is necessary for maximizing the amount of useful information read from the detector. Since the delivery of the samples is by means of a liquid jet injector, the X-ray beam sometimes misses the sample, causing an ‘empty’ image. In that case, the veto technique should be applied to overwrite this image.

2.2. Readout sequence

Due to the ASICs layout, the writing and reading of the memory cells is a complicated process and the neighboring cells influence each other. The vetoing of some memory cells can make this influence significant. Therefore the change in offset values after vetoing has to be studied.

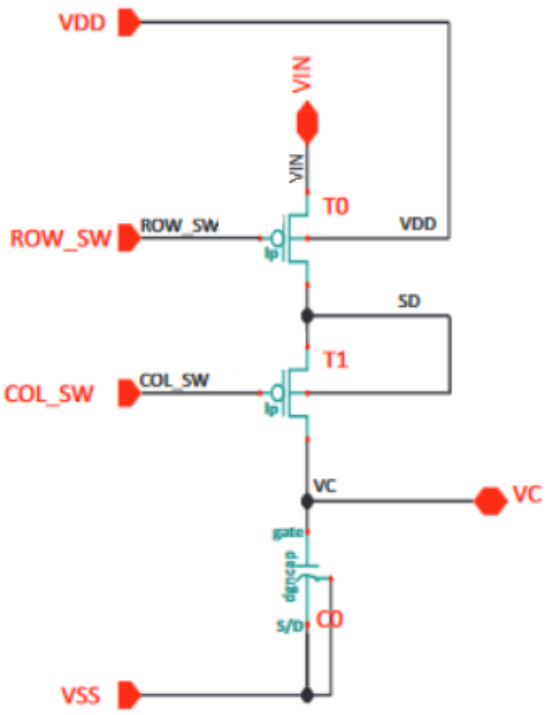

Fig. 6. Schematic of the storage cells in the analogue memory of AGIPD.

During the switching of row and column switches some charge can be lost on the node between ROW_SW and COL_SW.

The worst case is the last memory cell in the bottom pixel row, its column switch is operated (64×11) − 1 = 703 times and the row switch 32−1 = 31 times (due to column parallel readout), before the cell is finally read [5].

The memory access scheme is presented on the fig. 7. To get access to the specific memory cell, both – column and row switches have to be closed. It is called a wired-AND connection. This connection allows implementing the random access mode, but also due to operating the switches, the charge in the whole row and column can be partially lost.

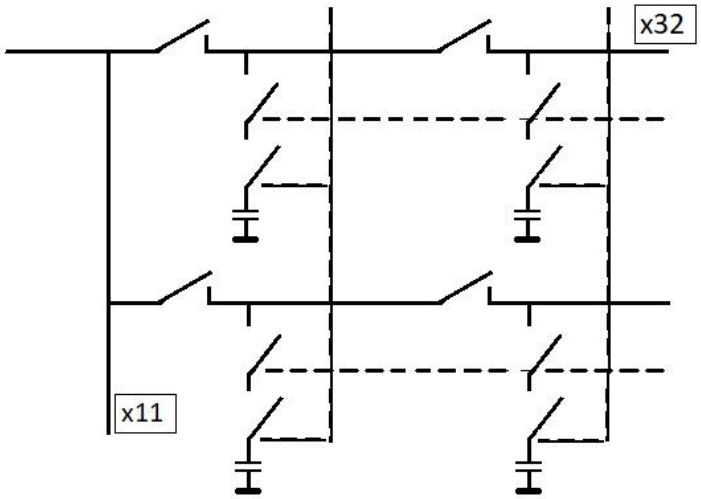

Fig. 7. Memory access scheme.

2.3. Normal acquisition

The dark frame is taken for 10 trains, for all 352 memory cells, and all 512×128 pixels. On the fig. 1 the memory cell matrix 32×11 is presented. The offset for each memory cell is the mean value for every train and every pixel.

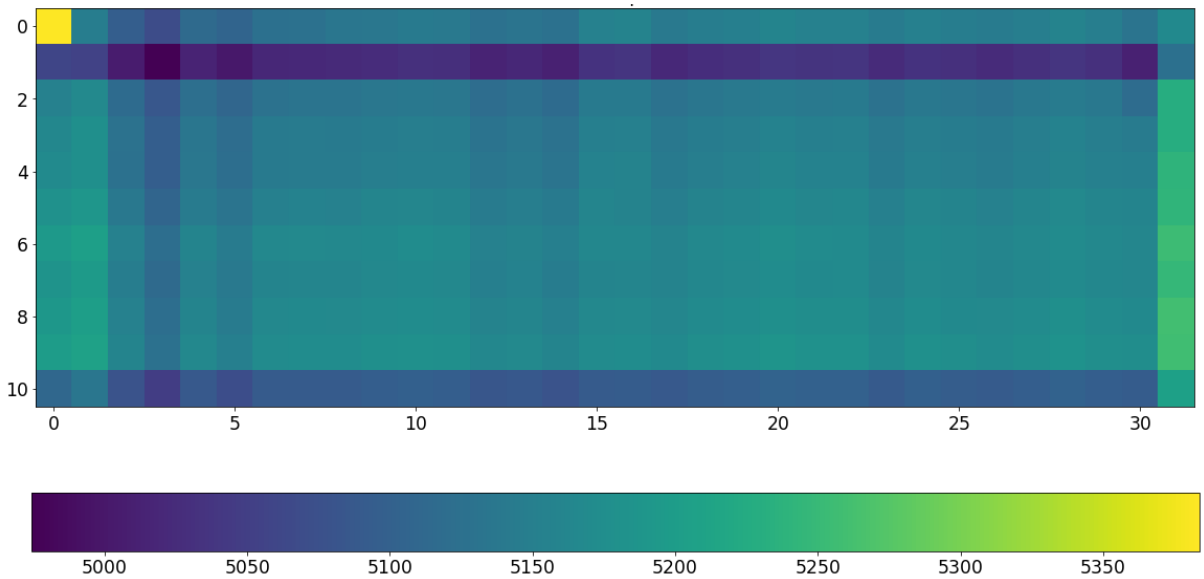

Fig. 8. Memory cell matrix 32×11 in the case of normal acquisition.

The normal acquisition means that all 352 memory cells were written in ascending sequence just once and read out straight after that.

For normal acquisition:

- The first memory cell has the highest offset which is + 200 ADU higher than the mean value.
  - It can be explained since for the 1st cell the charge on the node between row and column switches wasn't lost because the switches weren't operated yet.
- The whole second row of the memory matrix has a lower offset, by around -150 ADU.
- The last row has a lower offset, by around -50 ADU.
- The last memory cells in each row have a higher offset by about +100 ADU.
  - These effects happen due to the crosstalk between control lines in the pixel layout and memory readout lines.

In fig. 9 the offset values for each memory cell are presented.

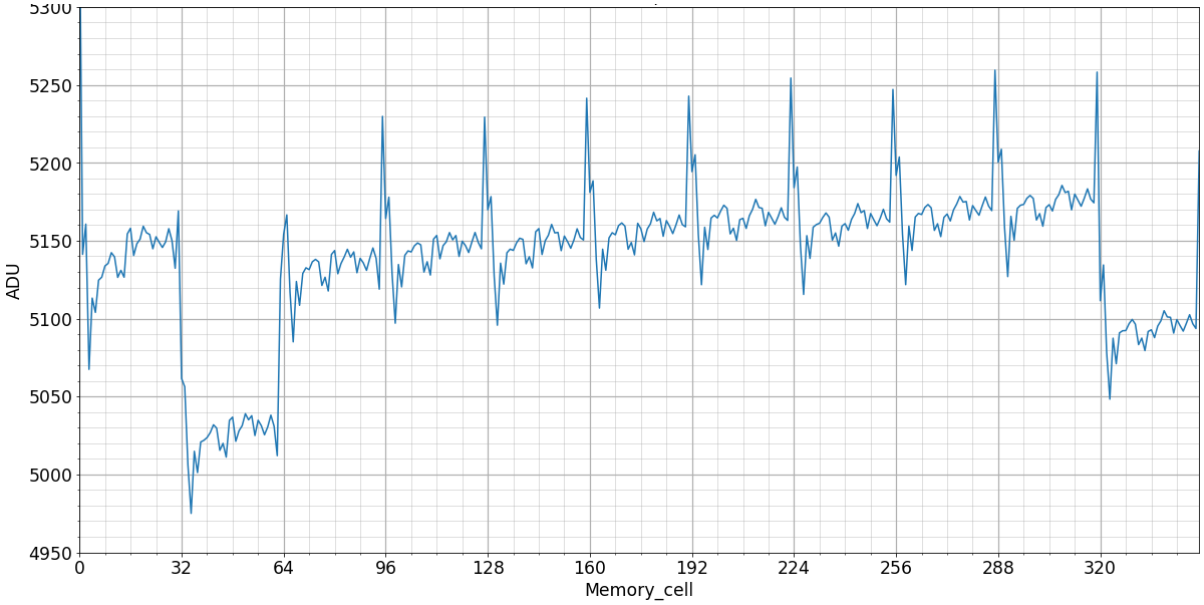

Fig. 9. The offset value (in ADU – analog-to-digital units) for each memory cell in the case of normal acquisition.

2.4. 1st experiment – Different number of bunches

Changing the number of bunches in train one can study how the acquired signal depends on the delay before the readout. It also can simulate the case of a different number of pulses during the experiments for implementing veto.

352 bunches is normal acquisition and since the time between 2 bunches is 222 ns, it takes 78 µs to write 352 memory cells. Straight after this, 352 memory cells are readout. So there is no delay before reading.

If one implements 2700 bunches during the train, the writing time is 2700 bunches × 222ns ≈ 0.6 ms. But one writes only 352 images, it means that before the readout there is a delay of ≈ 0.5 ms.

Table 1 – Delays before readout

No.	Number of images per train	Number of Bunches per train	Delay before read out, ms
1	352	352	0
2	352	2700	0.5
3	352	10 000	2
4	352	100 000	22

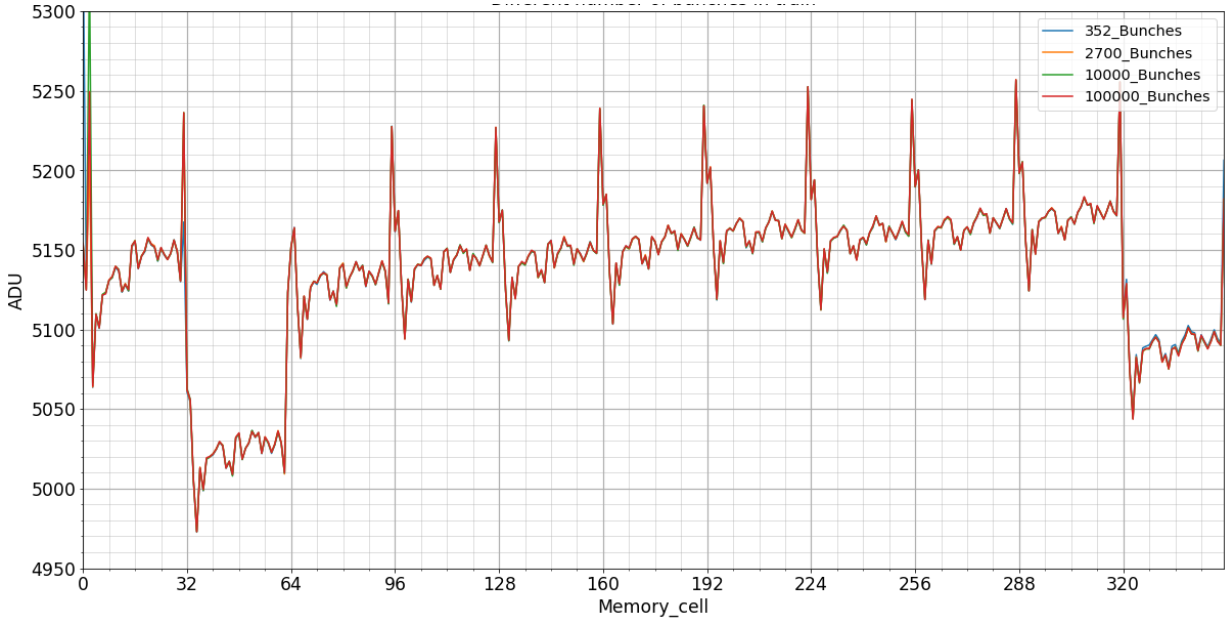

Fig. 10. The offset value for each memory cell for different number of bunches in a train.

- One can see that the delay before reading out (bigger number of bunches per train) has no influence on the acquired signal.
  - One of the reasons is that no additional switches were operated, and no charge was lost.
  - The droop effect should be significant due to the long waiting time (22 ms for the 4th experiment), but it wasn't observed.

2.5. 2nd experiment – Normal versus reverse acquisition

Simulating the reverse order of writing memory cells allows studying the droop effect and also the influence of the order of operating the switches.

During reverse acquisition, the writing in the memory cells starts with memory cell No. 352 and ends with memory cell No. 1. But the reading sequence is always the same – it starts from the 1st memory cell. This means that just after the writing memory cell 1, it is read out (no delays – should result in a higher offset). Conversely, the waiting time before the readout of the last (352nd) cell was twice as big compared to the normal acquisition (the offset should be lower). In Fig. 11 the cells in the top left and bottom right corners show this behaviour, while overall a gradient is observed for the cells in-between.

- Since the influence of waiting time before readout wasn't confirmed (see 1st experiment), one can suggest that the order of operating the row and column switches causes the observed difference in offsets.

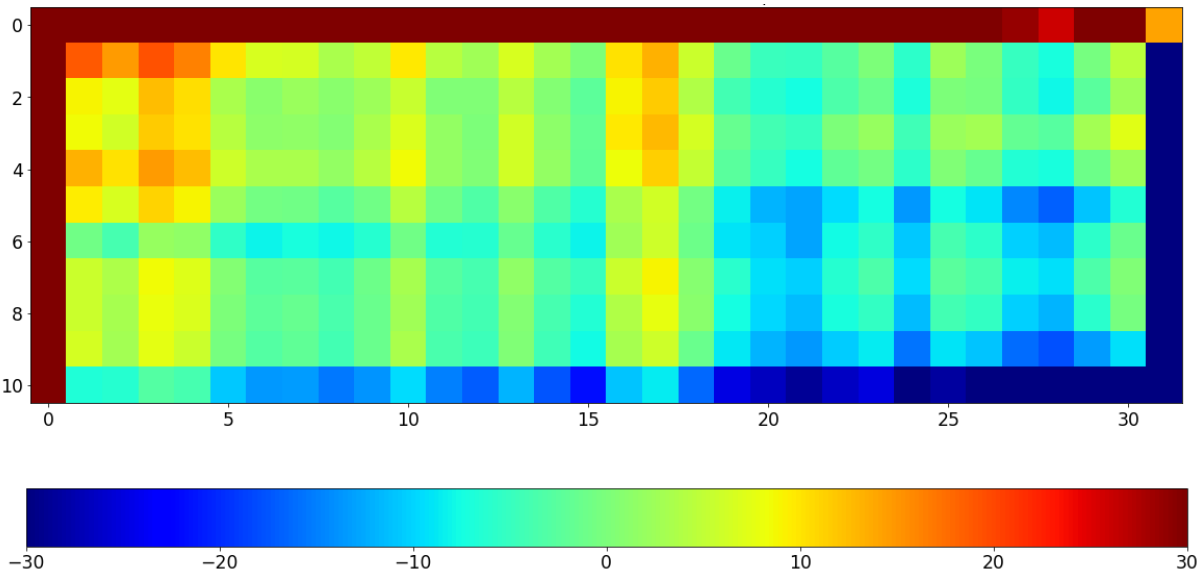

Fig. 11. Difference in offset between reverse and normal acquisition order.

2.6. 3d experiment – Veto a single cell

The veto a single cell experiment consists of taking one burst of 352 images, then rewriting one single cell and then reading out all images in normal (i.e. ascending) order.

The position of the vetoed cell doesn't matter. It always has the same influence on the offset values (as e.g. shown in fig. 16).

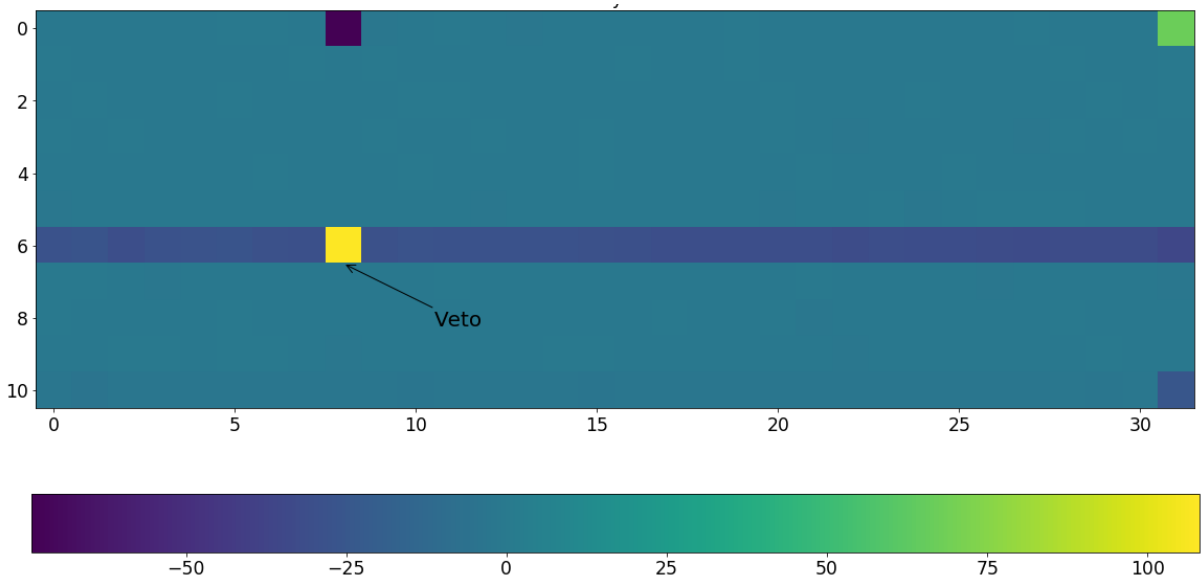

Fig. 12. Memory cell matrix representing the difference in offset between acquisition without veto and with veto of memory cell No. 200.

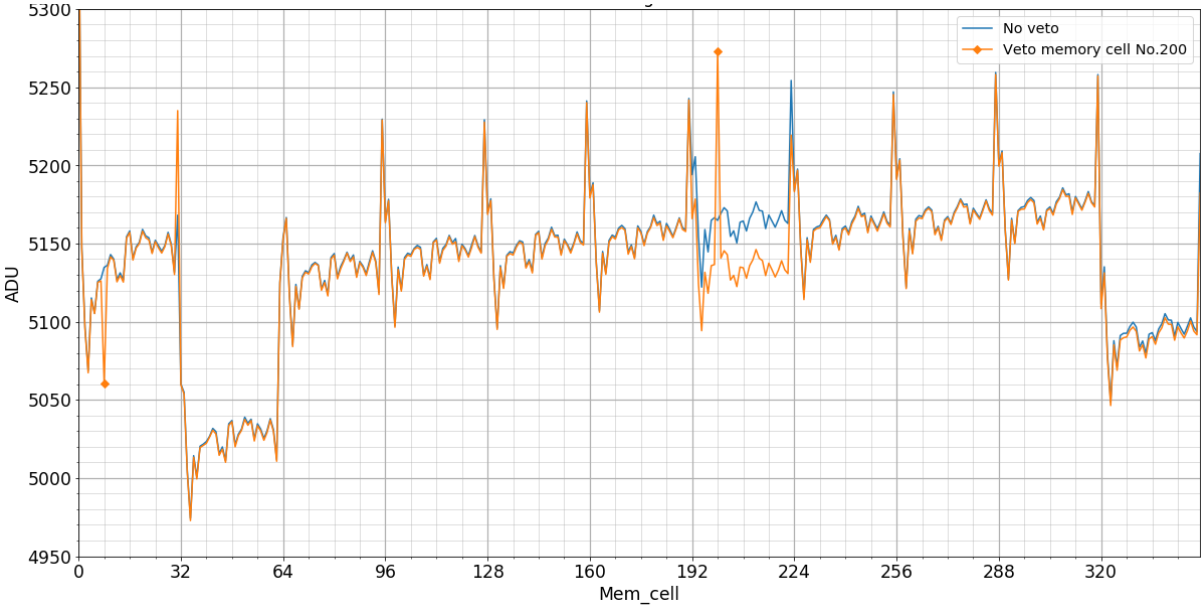

Fig. 13. The offset values for each memory cell for acquisition without veto and with veto of memory cell No. 200.

- The vetoed cell has a higher offset around +110…+120 ADU.
  - This effect still needs further investigation.
- The vetoed cell influences the whole row. The offset values are getting lower – by around -25 ADU.
  - This happens due to the additional operation of the row switch: some charge is lost in the whole row.
- The vetoed cell influences the 1st memory cell in the column. The offset value is also lower, around -75 ADU.

- Due to an additional operation of the column switch some charge is lost. But the reasons why it occurs just in the 1st cell have to be studied further.

For the vetoed cell No. 200 big dispersion of average offset value was observed. The ASICs of the vetoed cell has some gradient from the periphery to the center (see fig. 14).

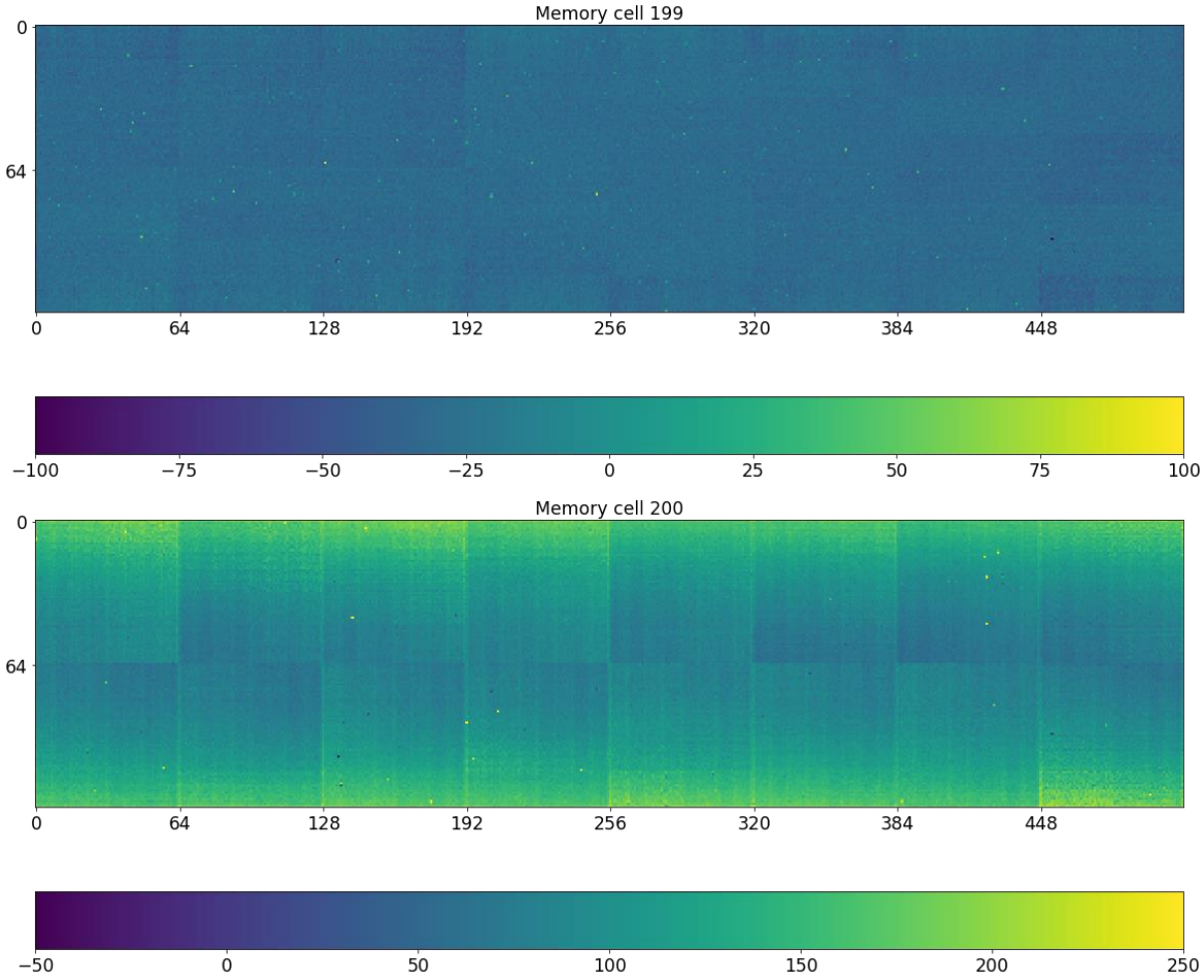

Fig. 14. Geometrical distribution of the offset change of the vetoed memory cells No. 199 (a) and No. 200 (b).

In comparison with non-vetoed cells, vetoed cells show in general a wider dispersion of the average offset value.

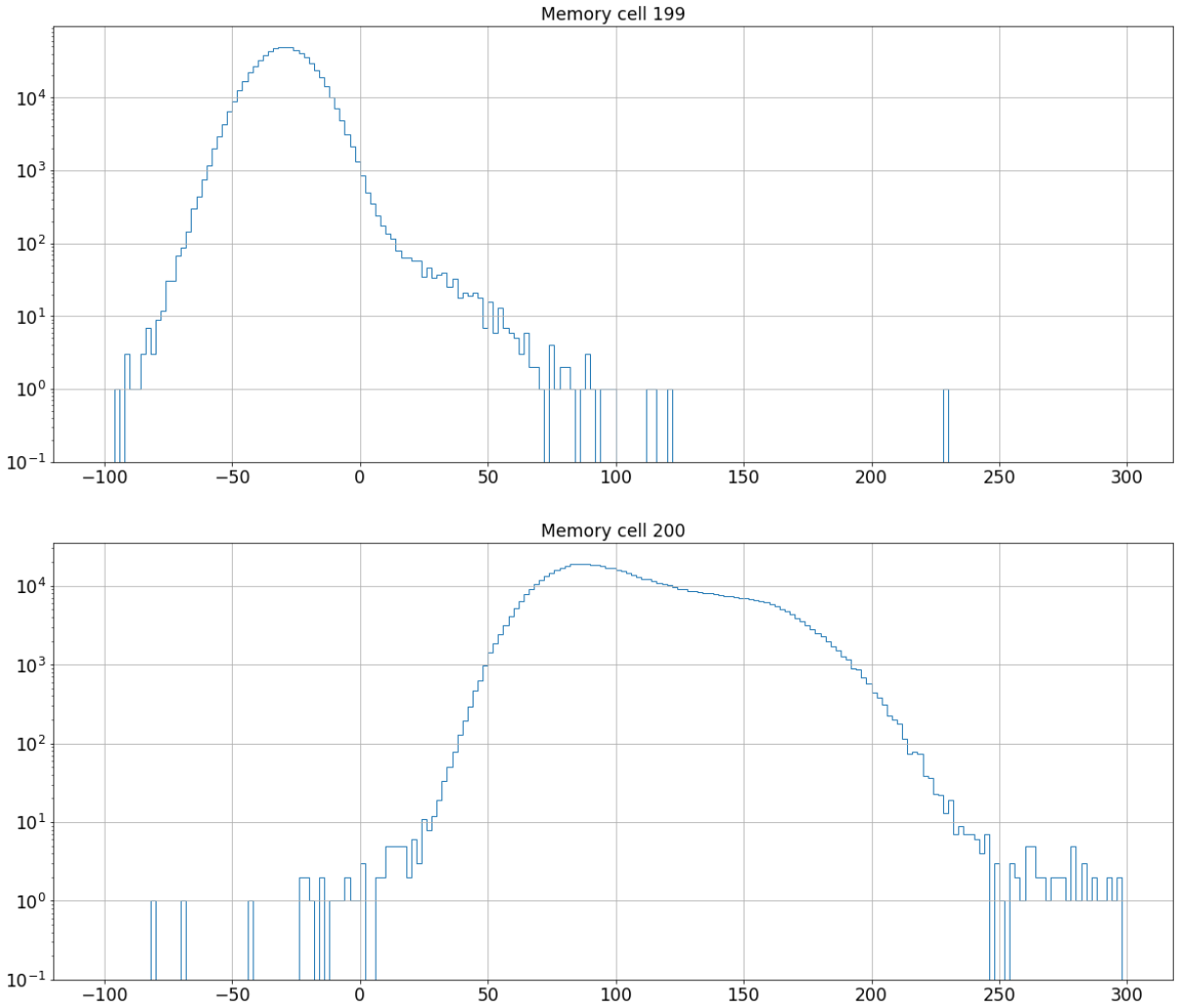

Fig. 15. The histograms of the offset values for each pixel, for memory cell No. 199 (a) and cell No. 200 (b).

The same behaviour is visible for an arbitrary vetoed single cell in each row, except for the last row (which even for normal acquisition shows an offset about -50 ADU lower than the average of all cells).

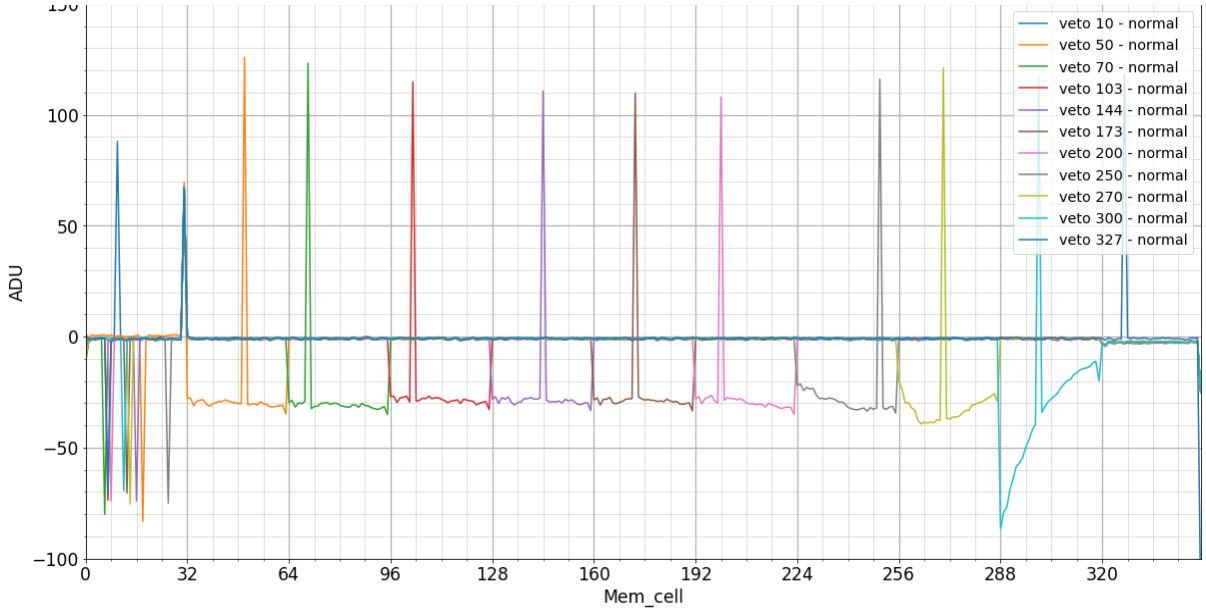

Fig. 16. The difference in offset values between acquisitions with and without veto.

2.7. 4th experiment – Veto 7 cells in a row

The veto experiment is performed by taking one burst of 352 images, then rewriting 7 adjacent memory cells of a single row in different directions (ascending – fig. 17 and descending – fig. 18) and then reading out all images in normal order.

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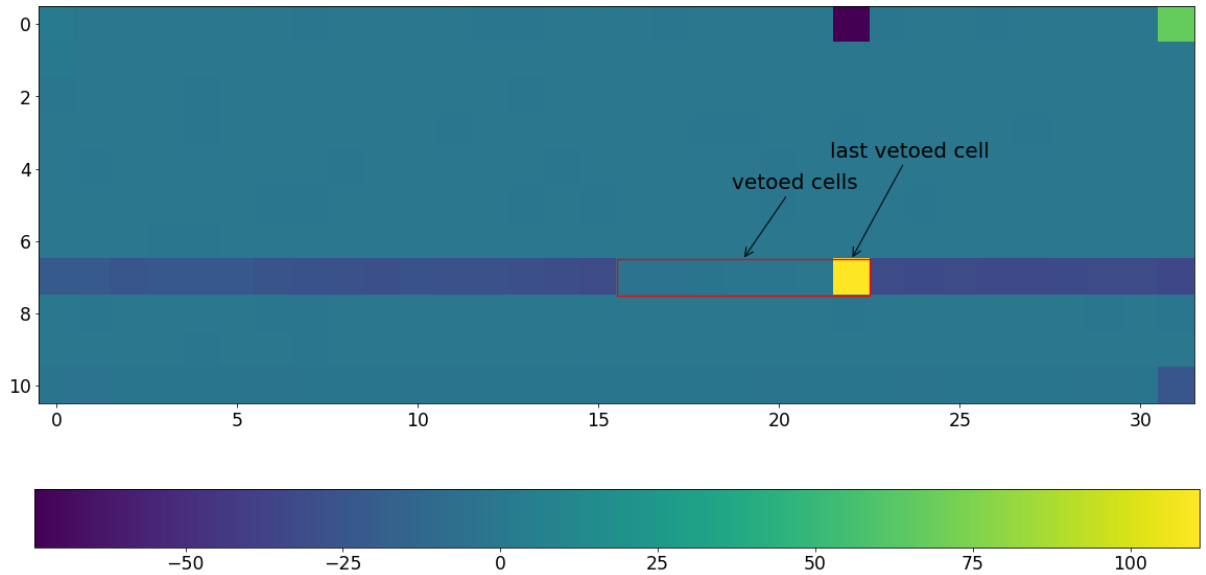

Fig. 17. The difference in offset between acquisitions without veto and with 7 memory cells vetoed in ascending order.

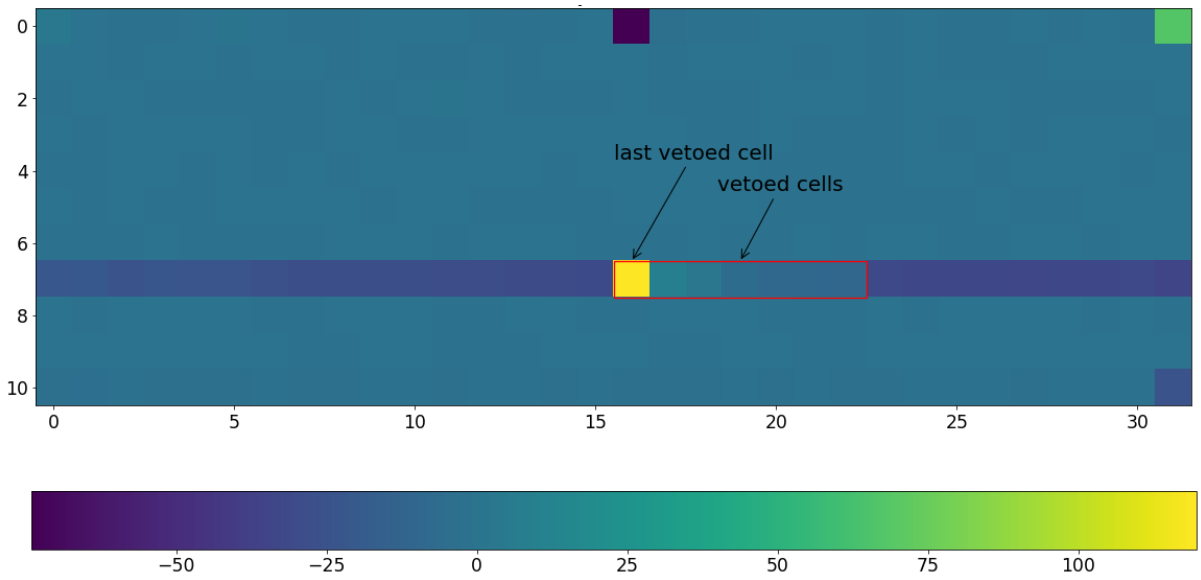

Fig. 18. The difference in offset between acquisitions without veto and with 7 memory cells vetoed in descending order.

- **Only** the last vetoed cell has a higher offset, around +110… +120 ADU).
- The other vetoed cells have no offset in the case of vetoing in ascending order and very low offset gradient – in the case of descending order.
- Vetoing influences the whole row. The offset of non-vetoed is getting lower by around -25 ADU. The offset difference is constant.
- The last vetoed cell influences the 1st memory cell in the column. The offset is also lower by around -75 ADU.

If one takes random memory cells from one row in the random or sorted order, the influence on the offset is still the same.

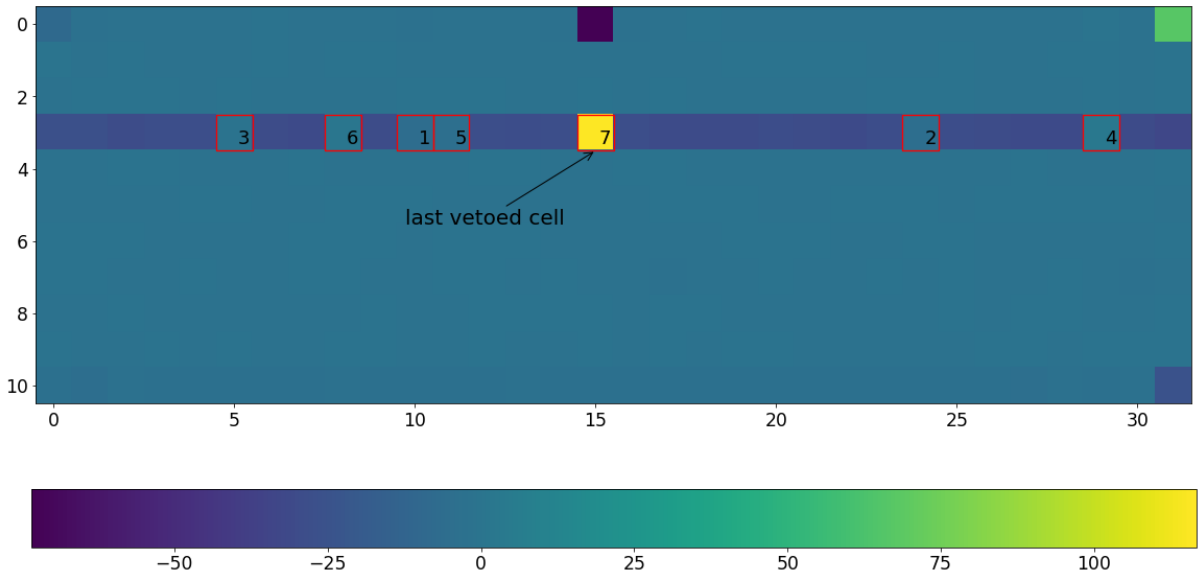

Fig. 19. The difference in offset between acquisitions without veto and with veto 7 memory cell in random order.

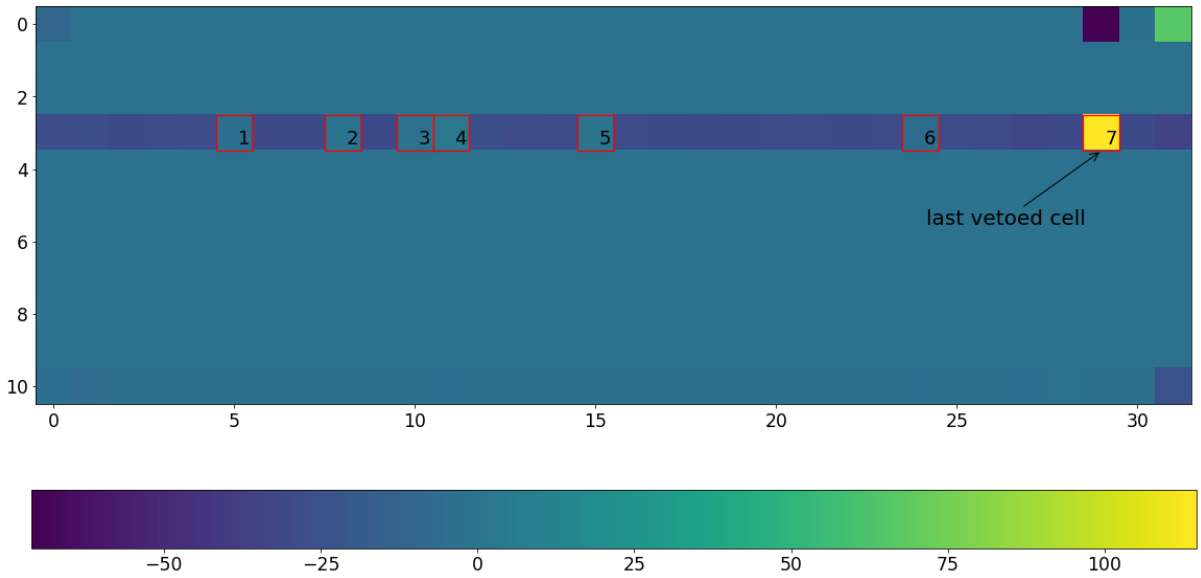

Fig. 20. The difference in offset between acquisitions without veto and with veto 7 memory cell in sorted order.

2.8. 5th experiment – Veto 7 cells in a column

In this experiment one burst of 352 images was written at first, then 7 memory cells in different rows were vetoed (in random order – fig. 21 and in one column – fig. 22) and then the memory cells were read out.

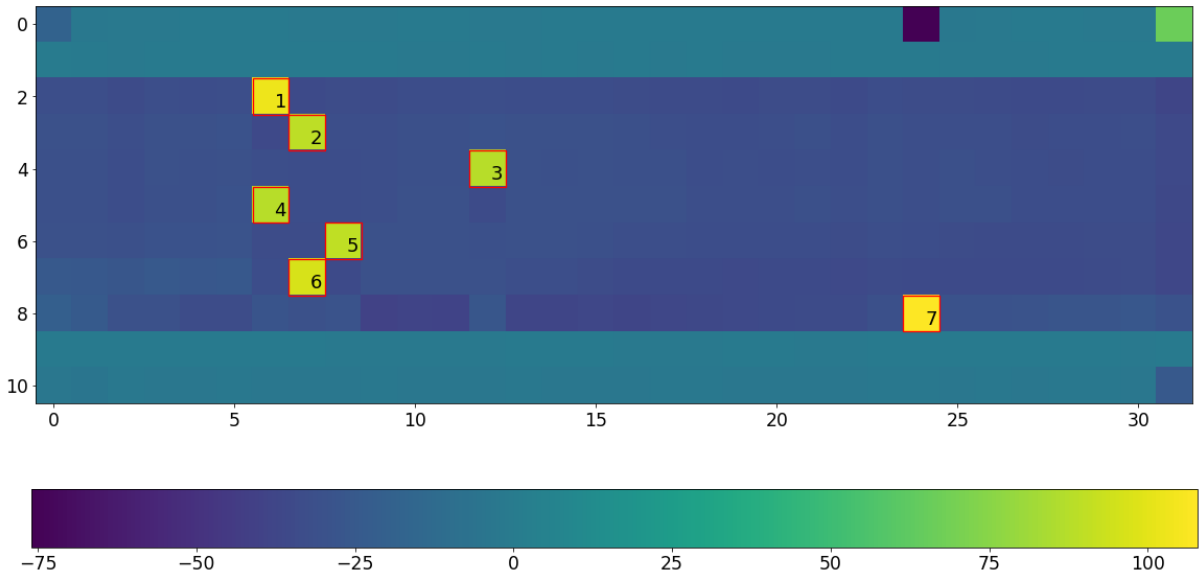

Fig. 21. The difference in offset between acquisitions without veto and with veto 7 memory cell in 7 different rows.

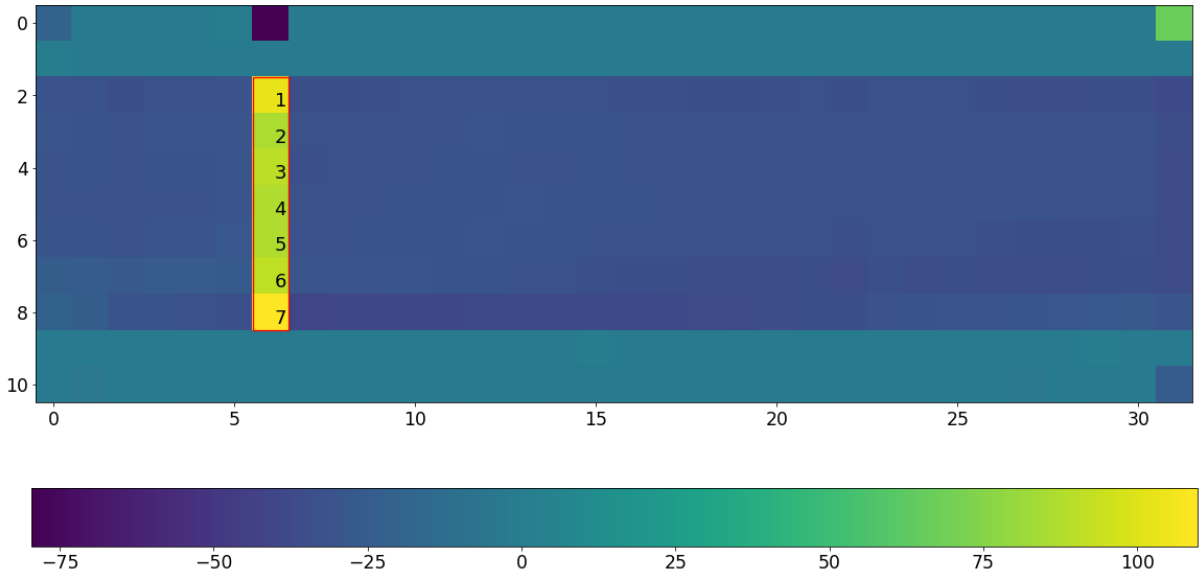

Fig. 22. The difference in offset between acquisitions without veto and with veto 7 memory cell in one column.

- The vetoed cells have higher influence on the offset value than in previous experiments, all of them around +100 ADU.

2.9. 6th experiment – Veto 21 arbitrary cells

After writing of one burst of 352 images, the 21 arbitrary memory cells were chosen and vetoed (in the random order – fig. 23 and sorted – fig. 24) and then the memory cells were readout. The resulting impact on the offsets value is more complicated but very similar.

- The maximum difference in offset values is -100…+120 ADU.

- The case of sorted order veto has a lower impact on the offset values.

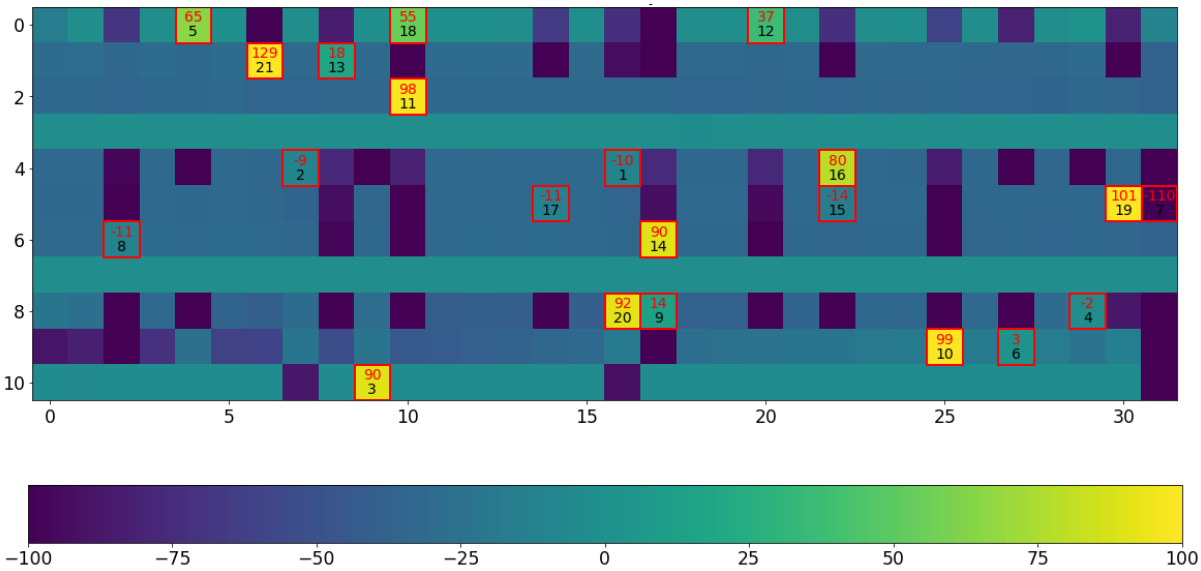

Fig. 23. The difference in offset between acquisitions without veto and with veto of 21 arbitrary memory cells in random order. The numbers indicate the deviation in offset (top) and the position in the veto sequence (bottom).

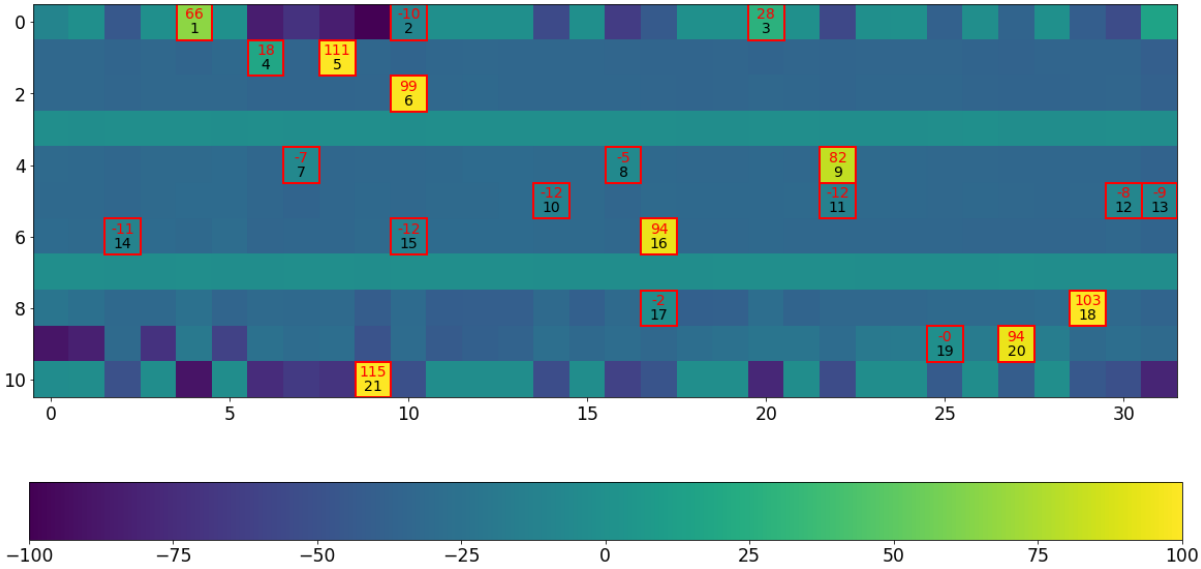

Fig. 24. The difference in offset between acquisitions without veto and with veto of 21 arbitrary memory cells in sorted order. The numbers indicate the deviation in offset (top) and the position in the veto sequence (bottom).

3. Summary

3.1. Results

1) The delays before readout doesn't influence the offset values.
2) The operation of the switches influences:
   - on the whole row which offset decreases by 25 ADU
   - on the 1st memory cell in the column which offset decreases by 75 ADU
3) In the case of vetoing of many memory cells:
   - the last memory cell has the highest offset: +120 ADU
   - the 1st memory cell in the column only for the last vetoed cell has the lowest offset: -75 ADU
4) The order of vetoing has to be taken into account.
5) The more vetoing cells the more complicated the scheme of calibration gets.

3.2. Conclusions

1) In the previous experiments [1] it was established that 6 ADU corresponds to the photon with energy 1keV. Since the AGIPD was developed for the experiments with photon energy 12 keV, what corresponds to 72 ADU, the veto implementation has a noticeable impact on the offset values of the memory cells – maximum around120 ADU – more than one photon energy.
2) The reasons for the influence of the veto need further investigation.
3) Next step: Study of charge dependency during veto implementation.

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