The Effect of Power Supply Noise on End-of-Substructure Card Behaviour

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Abstract

ATLAS detector will be upgraded for the HL-LHC, and several parts of the detector will be replaced. End-of-Substructure Card (EoS Card) is one part of ATLAS ITk that will be upgraded[3]. This work is to observe some of EoS outputs when an unusual supply voltage is present. Sinusoidal waveforms of supply voltage with different frequencies are considered as noise, and Clock Signal, DAC, ADC outputs are measured for each of noise frequencies.It turns out that noise do effect some of signals output, except ADC outputs–it can't distinguish whether noise is applied or not from ADC resolution.

To see what is happening when noise is applied, state of EoS are read in time sequence. And the result is noise will change the state off if it is presented for long period.

Contents

1 Introduction

My summer student project is to perform many tests on End-of-Substructure(EoS) Card which is a part in ATLAS Inner Tracker Upgrade. To observe EoS Card behaviour when power supply is not working normally and noisy signal is applied, Clock Signal, Input Signal, DAC output, ADC output, and machine states are recorded.

2 Background Knowledge

2.1 ATLAS Detector Overview

ATLAS is, in terms of dimension, the largest detector constructed at th LHC (Large Hadron Collider). It mainly use for detecting particles those come after $p-p$ colliding events. With 25 meters height and 44 meters length carrying approximately 7000 tons of weight, it probes proton-proton collision at the rate up to 40Mhz.

A toroidal magnet shape is wrapping around the detector providing the field strength of 4 Tesla for Muon Detector, and 2 Tesla superconducting solenoid magnet is used in the Inner Tracker. Between the two is the place for high granularity liquid-argon electromagnetic sampling calorimeters, and liquid-argon technology also use for hadronic calorimeter. The LHC has instanteneous luminosity of up to 10^{34} cm^{-2} s^{-1} for $p-p$, and even higher in the luminosity upgrade. In Figure 1 shows cut-away view of the ATLAS detector[1]

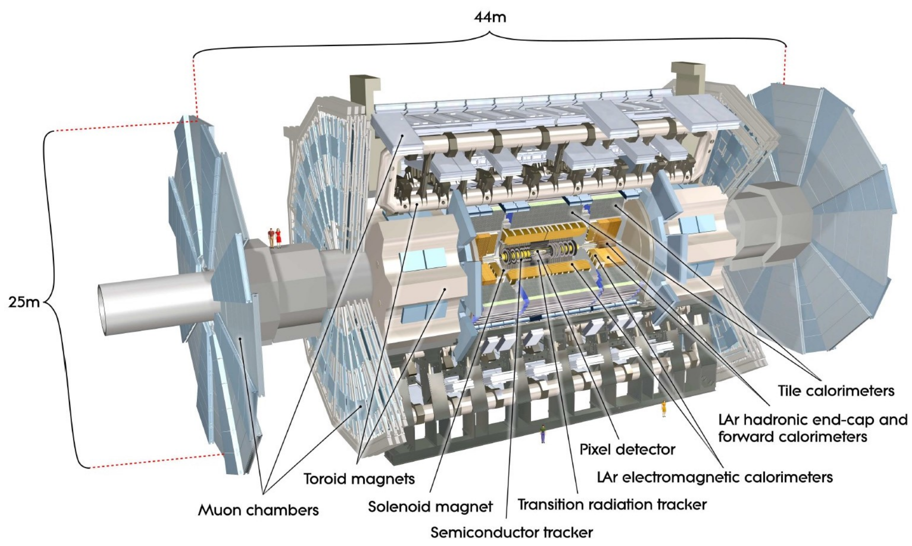


Figure 1: ATLAS detector[1]

2.2 ATLAS Inner Tracker Detector Upgrade

As plan in 2024, LHC will be upgraded to High-Luminosity Large Hadron Collider (HL-LHC), detector experiments will have to cope with higher environment. There are many plans of a lot of detector improvement during the upgrade. This work will specify on one of them–ATLAS Inner Tracker. In Figure 2, a model of ATLAS ITk shown.[3]

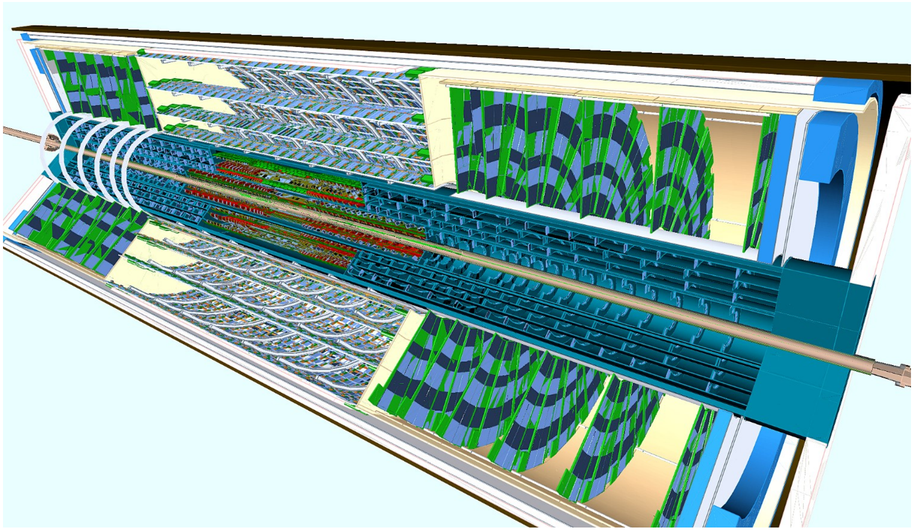


Figure 2: ATLAS ITk upgrade model[3]

2.3 End-of-Substructure(EoS) Card

In the part of the all-new upgrade of Inner Tracker, End-of-Substructure Card is essentially the data portal between inner component and off-detector component, as well as for control and delivery power to each part. Therefore, it is important to ensure that it will work smoothly during events operation because it will not be good to lose the data during measurement, and the repairing stage will be quite difficult since it sits very close to the interaction point. Where it is installed is shows in figure 3[3]

On to the EoS Card, there are several electrical component channels. Few of them are shown here.

2.3.1 Clock and Input Signal

To command instrument and handle the signals, the EoS needs clock signal at 40 MHz for data sender and data receiver. Here the gigabit-transceiver (GBTx) ASIC is used as a prototype of low-power gigabit transceiver (lpGBT) which will be used in EoS later on.

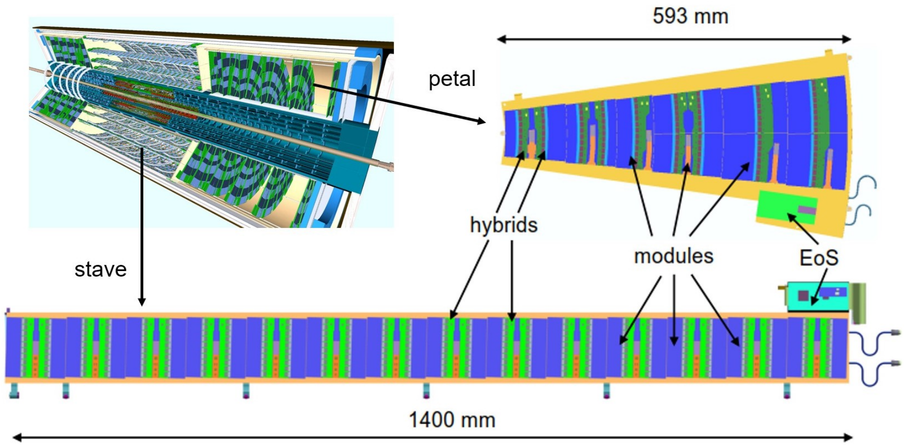


Figure 3: Petals and Stave detector component where EoS card sits on new Inner Tracker[3].

2.3.2 Digital to Analog Converter (DAC)

This device converts digital input “bit value” which we can input manually from the control unit to analog signal outputs. Generally, it wil be used for internal signal calibration.

2.3.3 Analog to Digital Converter (ADC)

This converts analog input to digital output. The output values–only from this component–are in hexadecimal numbers that correspond to an input voltage. Using in combination with the DAC to do self-calibration.

2.3.4 EoS Machine State

In figure 4, GBTx power-up state machine is shown. When the final state is “Idle”, it means that it is ready to operate. These states can be read in 5bit value on register 421[2]. The very first test is to find a lower limit of working voltage–meaning that it not“idle”. Turnouts that this can maintain “Idle” with the lowest voltage supply of 1.26 V, and surprisingly can come back to “Idle” if it is not lower than 0.2 V.

Table 1: Some states and their corresponding bits ID[2]

State	5 bits ID	Readable Value
reset	00000	0
waitDESLock	01010	40
waitSERLock	10000	64, 65
waitRXEPLLLock	01101	52
waitTXEPLLLock	10011	77
waitDllLocked	10101	85
waitPSpllLocked	11100	113
resetPSdll	11101	117
waitPSdllLocked	11110	121
Idle	11000	97

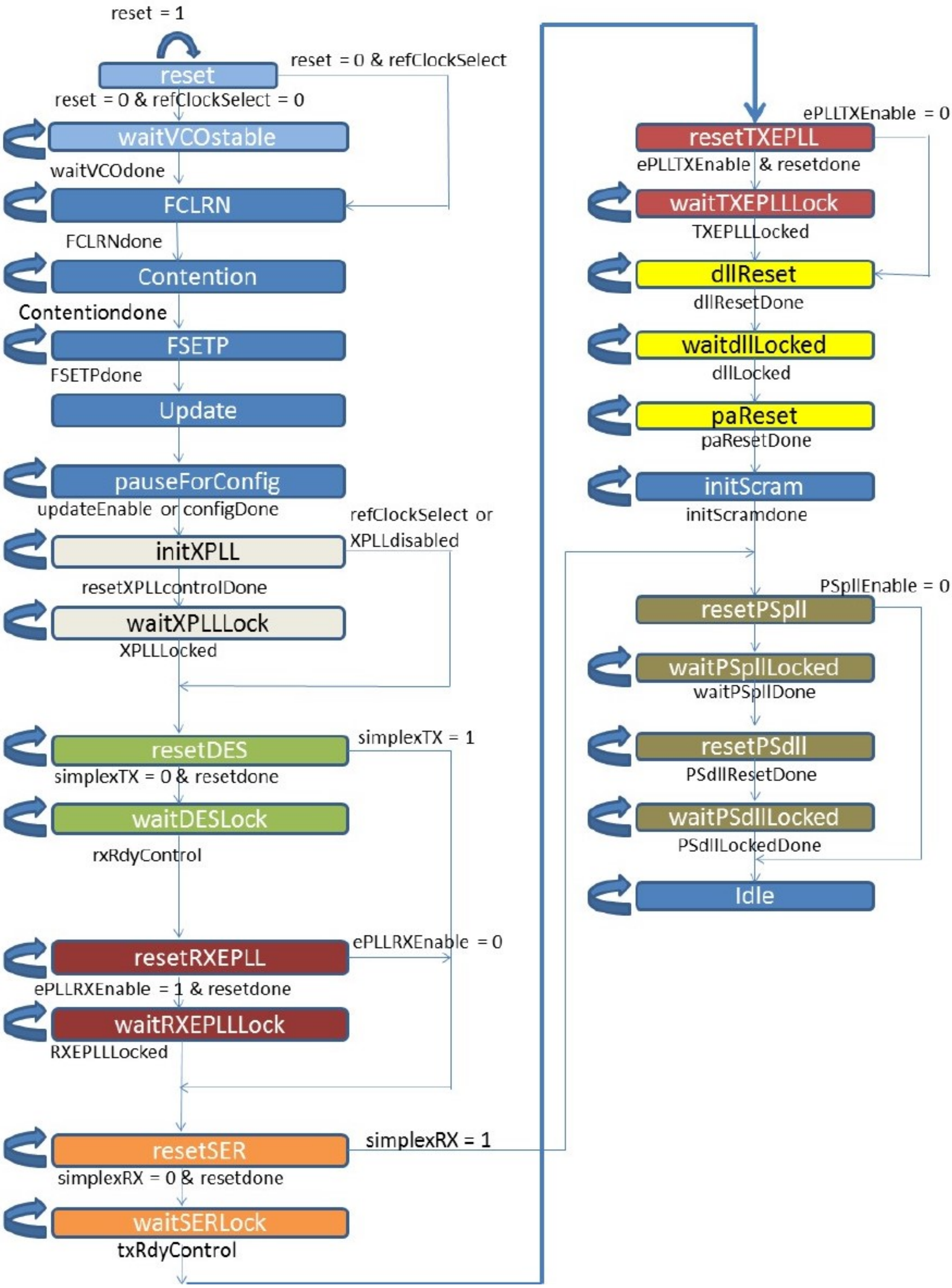


Figure 4: Power-up State machine flow diagram[2]

3 Experiment Setup

3.1 Power Supply Noise

The term“noise” here means the instability of power supply to the EoS Card. Keysight N6705C power supply can make an arbitrary function of voltage output. So, here we use the sinusoidal arbitrary function to represent the noisy environment of power supply. It can generate sinusoidal function up to 10 kHz which is the limit of this test. This assures the same noise pattern in every test.

Figure 5: Keysight N6705C Power Supply

3.2 Clock and Output Signal

In this test, I manually adjust supply voltage to 1.65 V, and the clock signal amplitude is enlarged. That extension is measured as V_0. Next, I generate sinusoidal noise with 150 mV amplitude centered at 1.5 V on normal working voltage and vary the frequency of the noise from 1 Hz to 10 kHz. The clock's amplitude also extends under noise environment, and now measures this extension as V_f for every frequency then calculate relative output as

$$RelativeOutput = \frac{V_f}{V_0}.$$

Then, I repeat the test with Output Signal

3.3 Digital to Analog Converter (DAC) Output

In this test, we use the same setup as in Clock Signal section, except the output is recorded directly. Because there are some other channels of DAC available, we repeat the test to check that the same phenomenon occurs.

3.4 Analog to Digital Converter (ADC) Output

In this test, external input is needed for it. Hence, 1 V constant voltage is applied here for input, and the output value is read one at a time. First, we need to see the distribution of output, then I can determine the output value for each noise frequency.

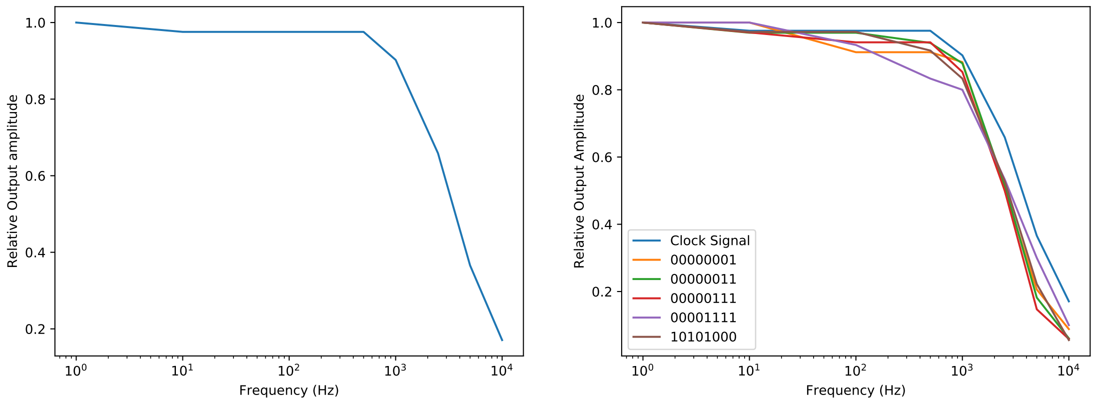
3.5 Machine State during Noise Period

In this test, I set the noise to 170 mA at 100 Hz. This can affect EoS state to break from "Idle" to some other states shown in figure 4. Next, I retrieve time sequence of machine states using a Python code I developed. Then, I the plot of what happened to it when noise is applied.

4 Results

4.1 Clock Signal and Output Signal

Both Clock Signal and Output Signal do follow low-frequency noise. But when noise frequency is increasing, these changes are reduced. This shows characteristics of a low-pass filter in the circuit.

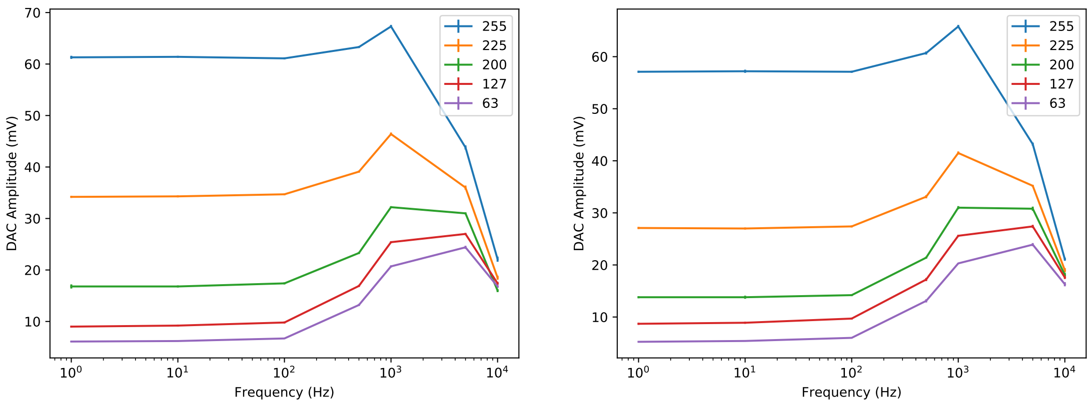


(a) Clock (b) Clock with Input

Figure 6: Effect of Noise on Clock and Input Signal

4.2 DAC Output

Signals of every input bit values on both channels still follow noise on low frequency, like in Clock Signal, but the effect increases at some frequency, then lessens. Drop-off behaviour implies there is a resonance frequency. This can be thought of as a combination of a high-pass and low-pass filter or multiple passive component characteristic.



(a) DAC channel 0 (b) DAC channel 4

Figure 7: Effect of Noise on Clock and Input Signal

Then, I test on 15mA of noise amplitude which equals to 1% of normal working voltage. The results also show the same effect.

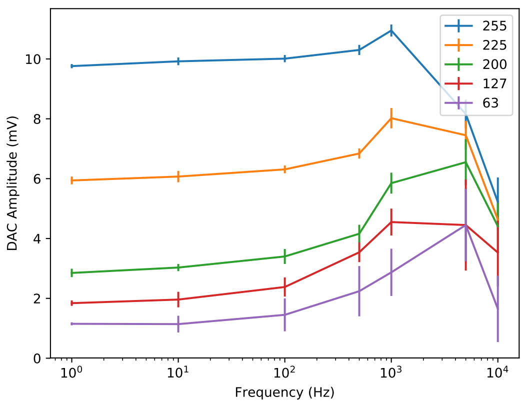


Figure 8: Effect of 1% noise on DAC output

4.3 ADC Output

From histograms in figure 9, all of the tests show gaussian distribution of ADC output value with left-skewed. So I use the mean value of output and standard deviation for each noise frequency.

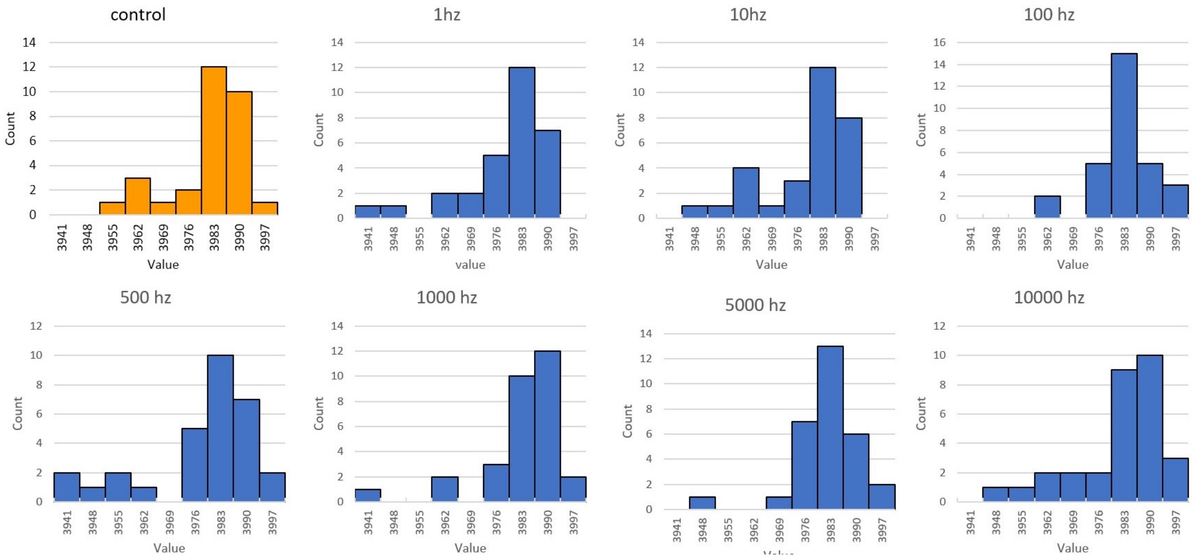


Figure 9: Histograms of ADC Output value with and without noise

In figure 10 each mean output values are plotted and standard deviation as error bar. This shows noise has no significant effect compared to the ADC's resolution.

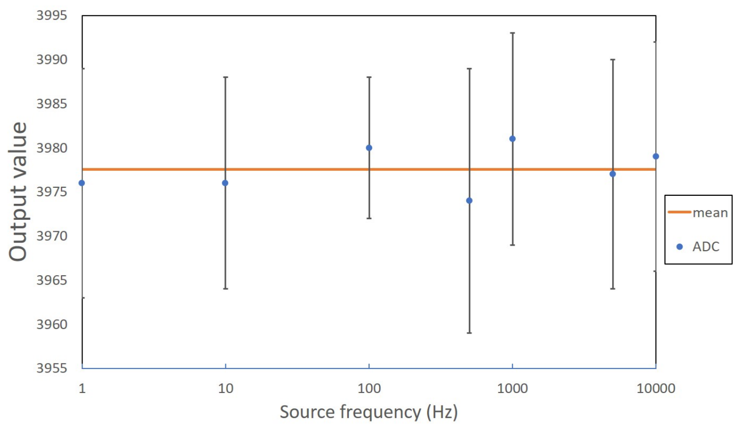


Figure 10: ADC output by noise frequency

4.4 Machine States During Noise Period

Figure 11 shows the values which represent the state at a time of reading. Here noise is applied for 1 minute from 10 s to 70 s. At the beginning of noise period, the state is jumping from 97 to 40 several times. From table 1 means that it is breaking from "Idle" to "WaitDESLock". After 30 seconds, the state falls slightly to 85 which is "waitDLLLock". Before noise ends, the state is more frequent on off "Idle" state.

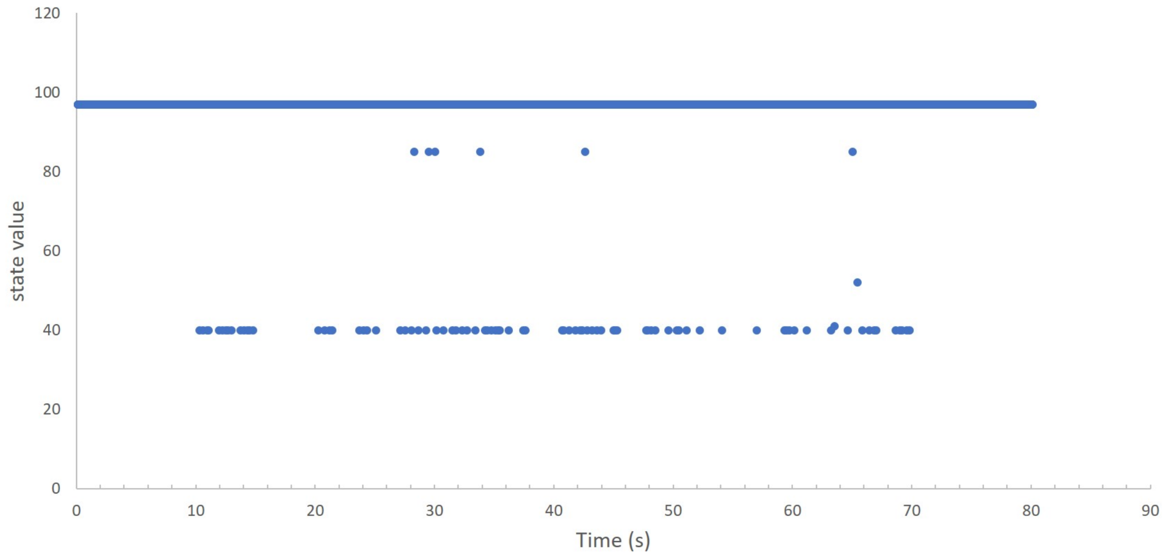


Figure 11: State Machine Sequence when noise is applied

5 Conclusion

From what I have done on EoS card, when sinusoidal noise present in EoS power supply, the component shows these effect;

- Clock and Output Signal would change due to gradually change in supply, however sudden change shows reduced effect.
- DAC shows characteristics of combinations of multiple passive components, and change would be greatest on a specific frequency
- ADC performance is largely uneffected under a noisy environment.
- EoS state will become unworkable after a large noise is applied.

What we know is that the change in supply can cause some of EoS outputs, and this should be considered in supply protection. Using sinusoidal waveform as a noise here for the simpliest noise, but the actual noise is still not known.

References

[1] The ATLAS Experiment at the CERN Large Hadron Collider *ATLAS Collaboration*

[2] GBTX Manual V0.16 DRAFT *GBT Project Team*

[3] The End-of-Substructure (EoS) card for the Strip Tracker Upgrade of the ATLAS experiment *Chaowaroj Wanotayaroj*