

Testing and characterization of power boards for PERCIVAL

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Abstract

PERCIVAL is a soft X-ray 2D imaging detector with back thinned and back side illuminated that yields high quantum efficiency and it will be used for Free Electron Laser's and Synchrotron radiation sources. The P2M version (1408 x 1484 Pixels) of the PERCIVAL system will use a setup that consists of a sensor which is placed on top of LTCC board, a power board which is used to supply the chip with the currents and voltages and contains the safety control that will sit close to the chip in vacuum and the carrier board. The characterization of a power board is required. The results of 7 power boards are presented here.

1 Acknowledgement

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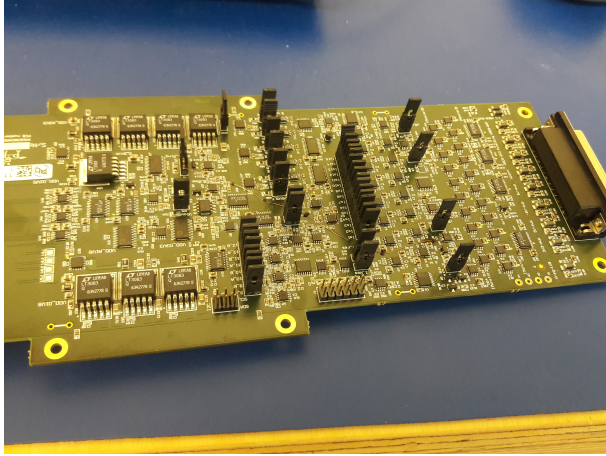
2 Introduction

PERCIVAL is a soft-Xray 2D imager which requires a power board (part of the front end electronics) to supply current and voltage biases to the CMOS sensor chip for its normal operation. It is back-thinned and it uses back-side illumination and back thinning to obtain a high quantum efficiency in the sub-keV range(250keV-1keV). The P2M version (1408 x 1484 Pixels) of the PERCIVAL system will use a setup that consists of a sensor which is placed on top of LTCC board. The operation of the sensor also depends on 100 control signals, voltage supplies and several biases. A raw data of 50Gbit/s is transported away from the sensor[1]. These voltages and currents are monitored along with various temperatures in the system. Wire-bonding of passive LTCC periphery boards to the sensor route the control signals, output data lines as well as required currents and voltages to the CMOS sensor chip[2]. The carrier board interfaces these LVDS lines and acts as a bridge to the outside world in terms of control, monitoring and timing interface. So, elaborate measurements were done to 7 Power boards which were characterized.

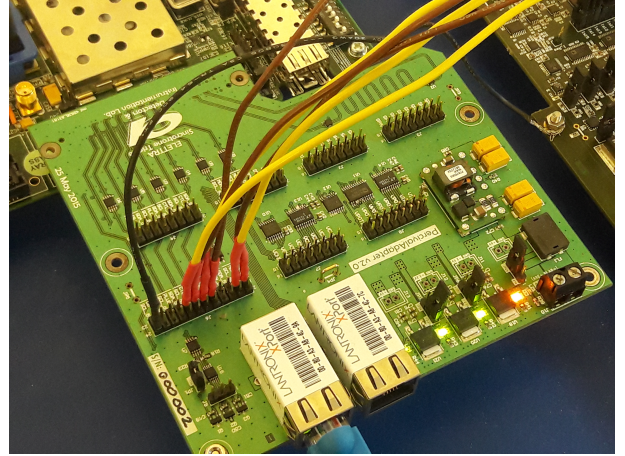
3 Measurement setup for Testing and characterization

The measurement setup for testing and characterization requires a power board with different voltage and current biases as shown in Figure 1 (a), an adapter board which is used to communicate with the power board using the communication lines is shown in Figure 1 (b), an evaluation board which has a FPGA (Field Programmable Gate Array) which sends the signal to the power board through the adapter board as shown in Figure 1 (c) and Weiner power supply 1(d) used to power up the power board. The full measurement setup is made as shown in Figure 2 with above three boards explained in Figure 1. With this measurement setup we measure current and voltages were measured in different configurations which will be discussed in detail in the next section.

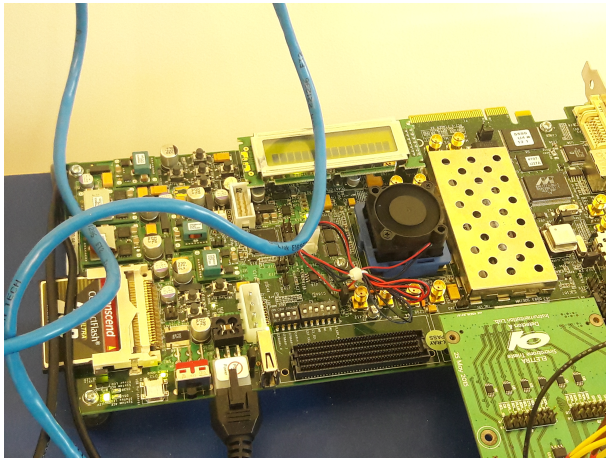
(a)



(b)



(c)

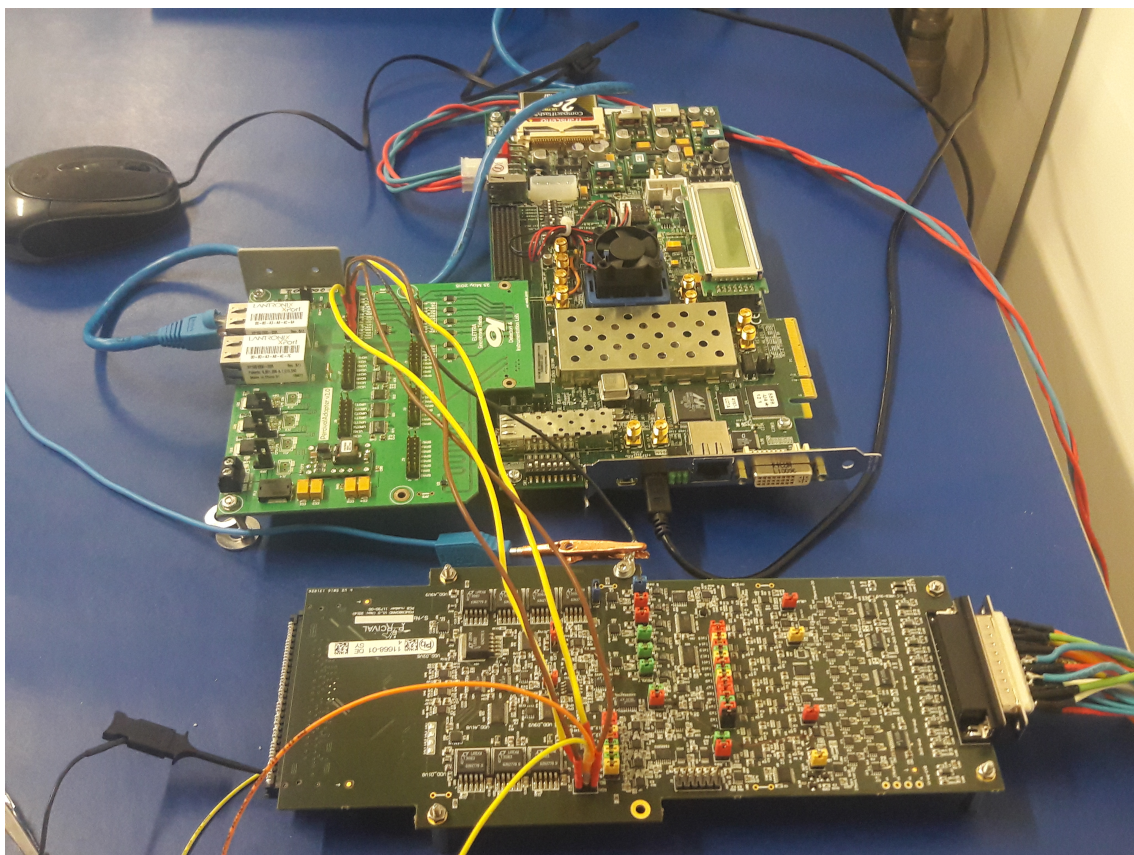


(d)



Figure 1: (a) Power board .(b) Adapter board .(c)Evaluation board. (d) Wiener power supply.

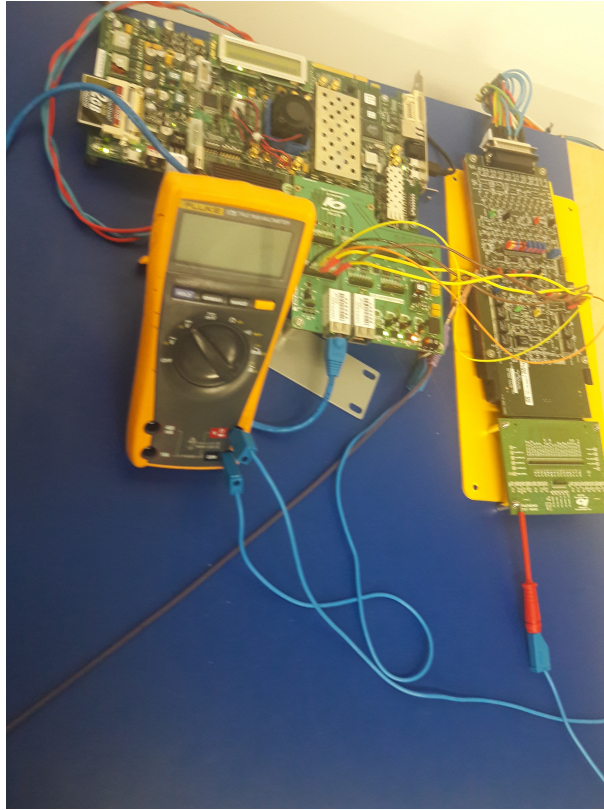
Figure 2: Full measurement setup with Evaluation board, adapter board and the power board.



3.1 Voltage bias measurements

For the voltage bias measurements, an external auxiliary board was used with pin outs for different voltage biases. This can be seen from Figure 3.

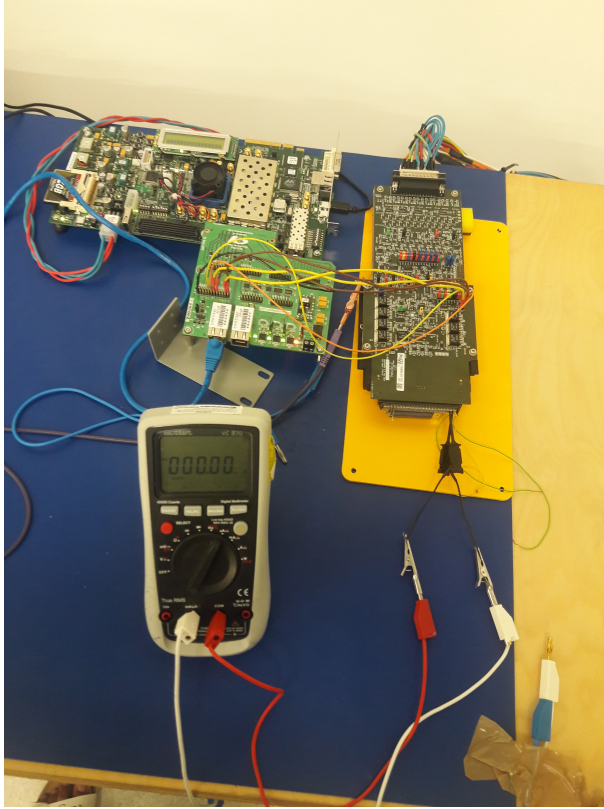
Figure 3: Voltage bias measurement setup.



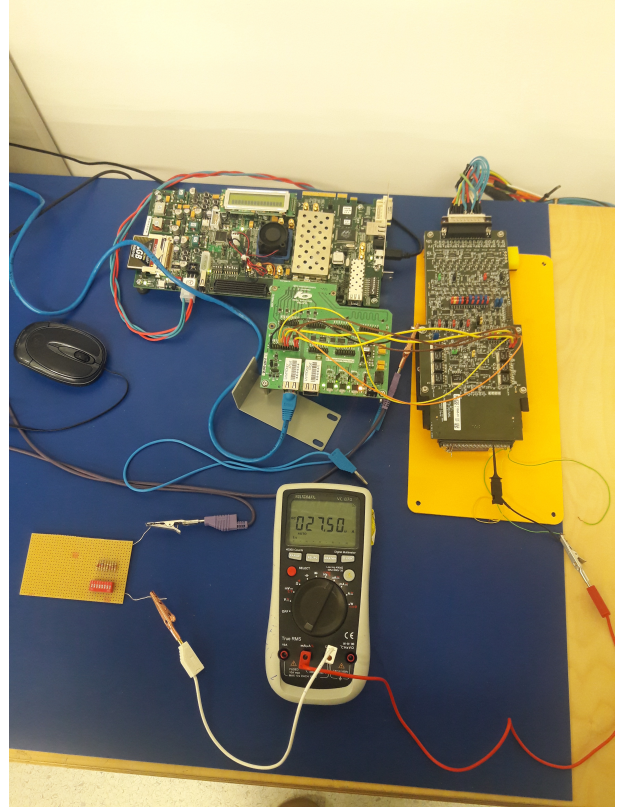
3.2 Current bias measurements

Two setups are used for measuring override 3.2 (a) and Readback currents 3.2 (b). Override currents are those currents which are generated by the power board and they are sent out before measurement and readback currents are generated and sent out and again comes back to the system.

3.2(a) Override current measurement.



3.2(b) Readback current measurement setup.



Also, the current monitoring was measured using a setup as shown in Figure 4. This measurement was done by ramping up the voltage source to highest value and then using resistors in the circuit to get the output current at a particular nominal range of the voltage. By using this setup, it was possible to monitor different biases.

Figure 4: Current monitoring setup.



3.3 Sources measured

The following Table 1 and Table 2 show the list of voltage sources current sources with their nominal values, supplies and current monitoring that were measured.

Bias	Nominal value [V]	Suggested Range [V]
VrefDBH0	1.8	0 - 3.3
VrefDBH1	1.8	0 - 3.3
VrefADCH0	1.9	0 - 3.3
VrefADCH1	1.9	0 - 3.3
VrefPGAH0	1.9	0 - 3.3
VrefPGAH1	1.9	0 - 3.3
VCASCH0	1.2	0 - 3.3
VCASCH1	1.2	0 - 3.3
VCM	1.25	0 - 3.3
Vin	-	0 - 4
VRST	1.8	1 - 3
VHIGH	4	0 - 5
Pixel Ring	-	-2-0
Vlow	-1	-2 - 0.5
Vmid1	0.7	0 - 1.2
Vmid2	3.3	0 - 3.3
VDD D2V5	2.5	2 - 3
VDD A3V3	3.3	2 - 4
VDD N	2.3	0 - 3.3
VDD A1V8	1.8	1 - 3
VDD D1V8	1.8	1 - 3
VDD D3V3	3.3	2 - 4
PSvolt	2	0 - 3.3
Vspare	-	0 - 5

Table 1: Voltage biases with Nominal values [V] and suggested range of values [V].

Bias	Nominal value[uA]	Suggested Range [uA]
IRESERVE	100	0 - 500
IBIASSFH0	100	0 - 500
IBIASSFH1	100	0 - 500
ICBIASPH1	90	0 - 500
ICBIASPH0	90	0 - 500
ADCBIAS2H0	100	0 - 500
ADCBIAS2H1	100	0 - 500
IBIASCALIBCH0	100	0 - 500
IBIASCALIBFH0	100	0 - 500
IFBIASNH0	30	0 - 150
ADCBIAS1H0	100	0 - 500
ADCBIAS1H1	100	0 - 500
IBIASPLLH0	20	0 - 100
IBIASPLLH1	20	0 - 100
IBIASLVDS1	450	0-2500
IBIASCOMPH0	100	0 - 500
IBIASCOMPH1	100	0 - 500
IFBIASNH1	30	0 - 150
IBIASLVDS2	16	0 - 100
IBIASTAILH0	100	0 - 500
IBIASTAILH1	100	0 - 500
IBIASCOLTOP	75	0 - 350
IBIASCALIBCH1	100	0 - 500
IBIASCALIBFH1	100	0 - 500
IBIASDACH0	100	0 - 500
IBIASDACH1	100	0 - 500
IBIASDACD	100	0 - 500

Table 2: Current biases with Nominal value [uA], suggested range [uA].

The Supplies and current monitoring of different voltage sources which are shown in table 3 were measured.

Supplies	Current Monitoring
3V3	VDD D3V3
5V	VDD D1V8
8V	VDD A1V8
-8V	Psvolt
Vreg 0v7	Vmid2
Vreg 2v3	VDD N
Vreg 1v8	Vmid1
Vreg 3v3in	Vlow
	VDD D2V5
	Pixel Ring
	Vhigh
	VDD A3V3
	VRST

Table 3: Supplies and current monitoring of voltage sources.

4 Results

4.1 Power board 2.2 characterization

Terminologies used in the measurement of voltage and current sources. To study the behavior of power board we need these terminologies.

- DAC- It is Digital to Analog converted values that is used to give input to the system in terms of Analog to Digital units (ADU).
- ADC- It is just the opposite operation of DAC i.e. Analog to digital converted values that we obtained as output in terms ADU.
- Linear regression- This is done with Linear fit using regression function as $y=A*x+B$ with fitting parameters(A and B) to see how linear the particular current source or voltage source operates in the linear region of their operation.

4.2 Voltage bias measurement plots

4.2.1 Voltage Output vs DAC input plot for voltage sources

The Figure 5 shows the Voltage output vs DAC input of the voltage regulator source VDD D1V8 and other voltage regulator sources VDD A1V8, VDD D2V5, VDD A3V3 VDD N show a similar behavior.

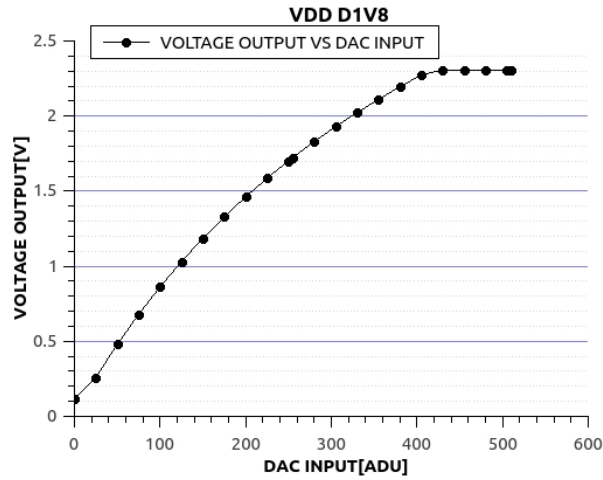


Figure 5: Voltage output vs DAC input of the voltage regulator source VDD D1V8.

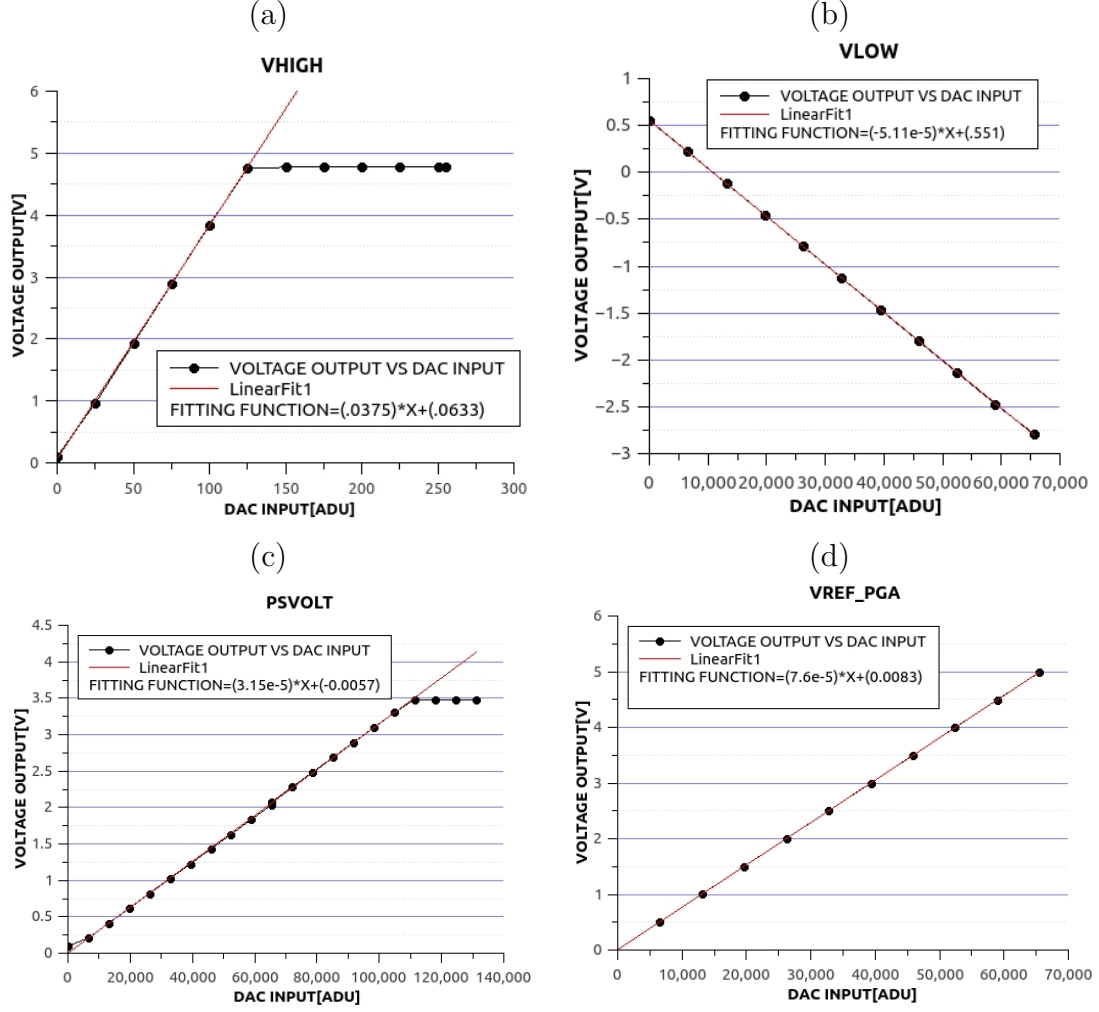


Figure 6: (a)Plot of voltage output vs DAC input for VHIGH.(b)Plot of voltage output vs DAC input for Vlow.(c)Plot of voltage output vs DAC input for PSvolt. (d)Plot of voltage output vs DAC input for VrefPGA.

In Figure 6 (a) The voltage output vs DAC input plot for Vhigh is shown with linear regression with fitting parameters. VHIGH saturates at about 4.5 volts. A similar behavior is obtained for Vmid 1, Vmid2, VRST, PSvolt. In Figure 6 (b) The voltage output vs DAC input plot for Vlow is shown linear regression with fitting parameters which shows the linear behavior for Vlow. A similar behavior is obtained for Pixel Ring. In Figure 6 we have the voltage output vs DAC input plot for PSvolt with linear regression and the fitting function with fitting parameters is shown. A similar behavior is obtained for Vmid 1, Vmid2, VRST and VHIGH. In Figure 6 we have the voltage output vs DAC input plot for VrefPGA0 with linear regression and the fitting function with fitting parameters is shown. A similar behavior is obtained for VrefDBH0/H1, VrefADCH0/H1.

4.2.2 ADC Output vs Voltage output plot for voltage sources

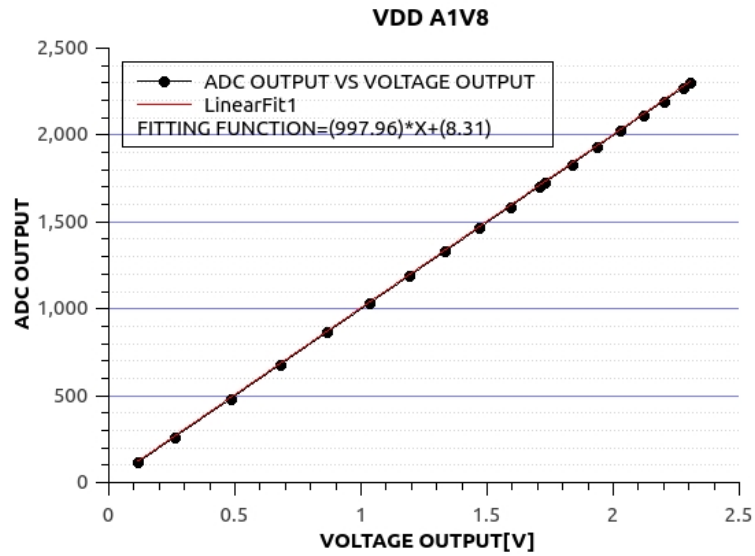


Figure 7: ADC output vs voltage output of the voltage regulator source VDD A1V8.

In Figure 7 describes the plot of ADC output vs voltage output of the voltage regulator source VDD A1V8. The linear regression and the fitting function with fitting parameters which shows the linear behavior. A similar behavior is obtained for other regulator sources are shown VDD D2V5, VDD A3V3, VDD D3V3, VDD N.

4.3 Current bias measurement plots

4.3.1 Override current measurement

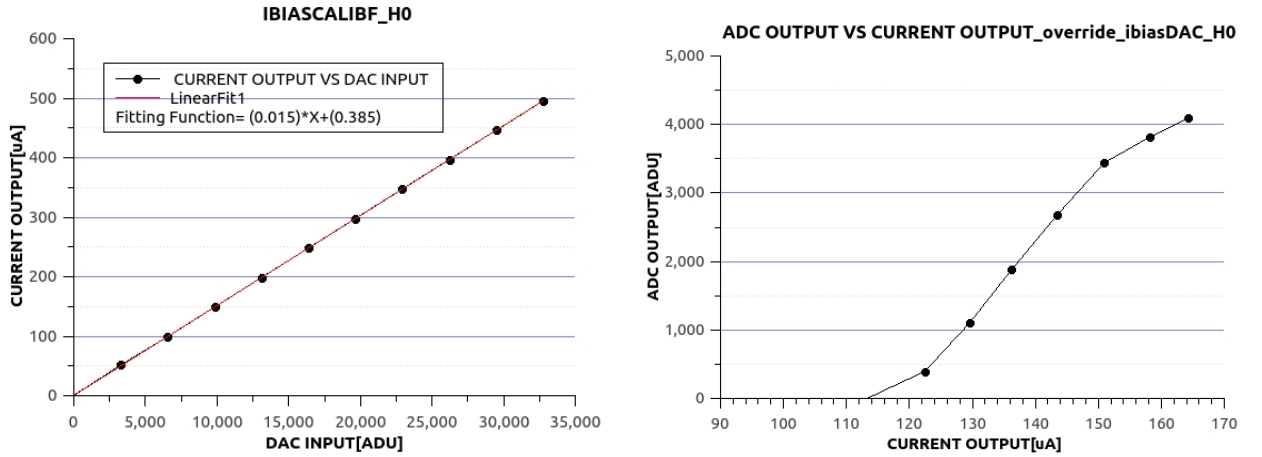


Figure 8: (a)Current output vs DAC input of override current IBIASCALIBFH0. (b) ADC Output vs current output of IBIASDACH0

In Figure 8 (a) The Current output vs DAC input plot of IBIASCALIBFH0 is shown with linear regression and fitting parameters. A similar behavior is obtained for other current sources like IBIASCOMPH0, IBIASCALIBCH1, ICBIASPH1, IBIASCOLTOP and most of the current sources mentioned in the Table 2. Figure 8 (b) Describes the plot of ADC output vs current Output of the current source IBIASDACH0 which shows a problematic behavior as it can be seen from the plot of this current source in the **100 μ A** range its not giving any output. This behavior for power board **2.2** was unusual. This in future and need to be solved. **This behavior was not seen in any of the power boards from 2.1 to 2.7.**

4.3.2 Current monitoring and Readback current measurement

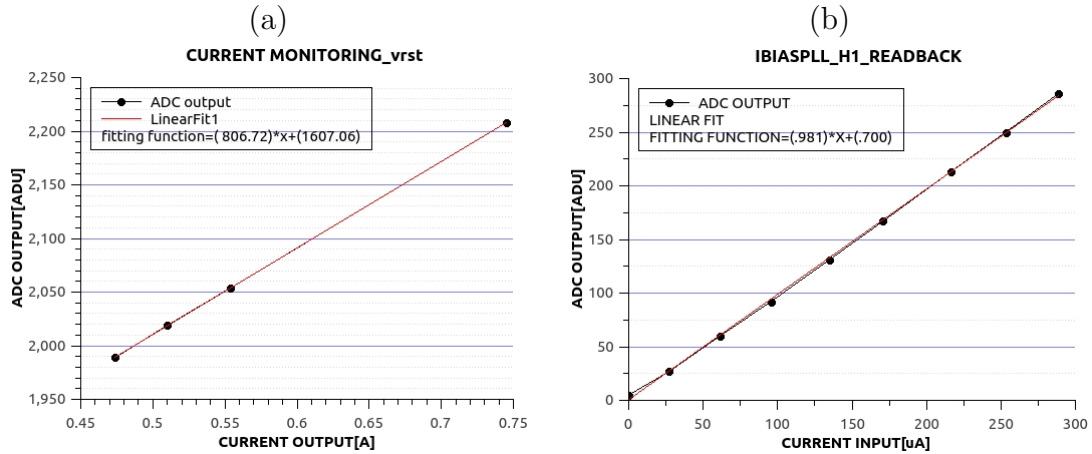


Figure 9: (a)ADC Output vs current output of VRST. (b) ADC Output vs current output of IBIASPLLH1.

In Figure 9 (a) The ADC output vs current input plot for VRST is shown with linear regression with fitting parameters. A similar behavior is obtained for other current monitoring of sources such as VDD A1V8, VDD D2V5, PSvolt, Vmid1, Vlow and other sources mentioned in Table 3. In Figure 9 (b) The readback current measurement for IBIASPLLH1 is shown.

4.4 Overall result of the characterization with 7 power boards

The overall result which is obtained after charecterisation from seven power boards 2.1 to 2.7 is shown below. For different power boards every voltage source and the current source which is listed in the previous measurement section was measured. The major problem found was the current source IBIASDACH0/H1 in which the ADC output vs current output plot does not show any output at 100 uA which is the operational region. Also, the current monitoring of the LVDS1 was not functional during all sets of measurement from power board 2.1 to 2.7. There current monitoring of VHIGH on power board 2.4 and 2.7 is not behaving linearly with the nominal range.

Power Boards	2.1	2.2	2.3
Voltage biases	TEST OK	TEST OK	TEST OK
Override currents	TEST OK	Problem with ibiasDACH	TEST OK
Readback currents	TEST OK	TEST OK	TEST OK
Supplies	TEST OK	TEST OK	TEST OK
Current Monitoring	Problem with LVDS1	Problem with LVDS1	Problem with LVDS1

Power Boards	2.4	2.5	2.6
Voltage biases	TEST OK	TEST OK	TEST OK
Override currents	TEST OK	TEST OK	TEST OK
Readback currents	TEST OK	TEST OK	TEST OK
Supplies	TEST OK	TEST OK	TEST OK
Current Monitoring	Problem with LVDS1 and Vhigh	Problem with LVDS1	Problem with LVDS1

Power Boards	2.7
Voltage biases	TEST OK
Override currents	TEST OK
Readback currents	TEST OK
Supplies	TEST OK
Current Monitoring	Problem with LVDS1 and Vhigh

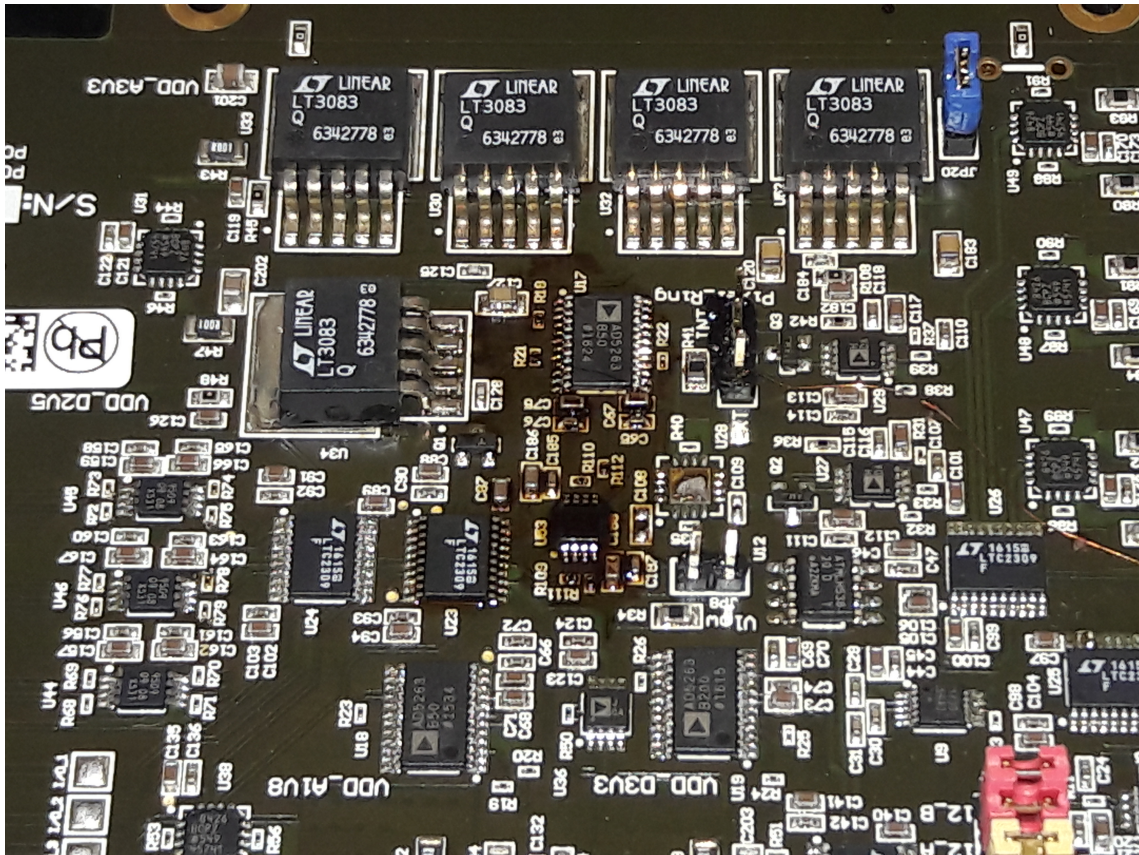
5 Problems Found during the measurements and their solutions

- Analog output of the voltage source VDDA3V3 and VDDD2V5 were stuck at zero value inspite of the fact that there was a full range scan. As it can be seen on Figure 10.
- After inspection it was found that the potentiometer that was related to vary the resistance of these two sources was not functioning properly.
- After replacement of this component from the power board measurement was taken and problem was resolved.

6 Conclusions

After characterization it was found that most of the power boards function well within the desired range. Also, the current monitoring of LVDS1 was not operational. The current source IBIASDACH0/H1 has issues in the monitoring for power board 2.2. In power boards 2.4 and 2.7 there were some issues with VHIGH . Some problems were also encountered such as Analog output of the voltage Regulator sources VDDA3V3 and VDDD2V5 were stuck at zero value inspite of the fact that there was a full range scan. After inspection it was found that the potentiometer that was related to vary the resistance of these two sources was not functioning properly. After replacement of this component problem was solved. With this characterization we can go for future power up while using any three out of seven of the best power boards that we have in hand. So, power boards 2.3, 2.5 and 2.6 can be used in future for powerup.

Figure 10: Picture taken after replacing potentiometer integrated chip.



7 Appendix

This is the format of the output files of the voltage and current sources.
This is one Of the output file of VDD D2V5 as shown in Table.

0	1959
1	2097
2	2229
3	2353
4	2473
5	2585
6	2694
7	2798
8	2898
9	2993
10	3085
11	3102

Commands used to initialise power boards.

```
1.)# If you are not already in the percivalui dir:  
cd Percival/percivalui
```

```
2.)source venv27/bin/activate
```

```
3.)# Set an environment variable with the IP address of your Carrier Board Xport  
export PERCIVAL_CARRIER_IP=192.168.0.2 (ethernet cable connected to xport com 1)
```

```
4.)percival-control --init  
(takes a while: initializing board, adding (scrolling) )need Cntrl-C.
```

```
5.)python ./sandbox/systemcommand.py --action fast_disable_control_standby
```

[devices are by default turned on in standby mode (output off, min pow consumption)].

6.)python ./sandbox/systemcommand.py --action disable_startup_mode

[devices are by default turned on in startup mode mode (output = min). This command d

7.)python ./sandbox/systemcommand.py --action disable_device_level_safety_controls

[enables check of the limits]

8.)python ./sandbox/systemcommand.py --action enable_global_monitoring

[enables monitoring]

9.)python ./sandbox/systemcommand.py --action fast_sensor_powerdown

[bring all deviced to standard low value situation.

10.)command used for run the scan for voltage is of the form:

Percival-scan-devices--range''0,65535,6550''--outputdata/scan_vs_Vref_ADC.h5--period'

Where the range of the scan start from 0 to 65535 and with steps of 6550.

We can have the similar scan for currents.

References

- [1] C.B.Wunderer et al.,Percival:An international collaboration to Develop A MAPS-based soft X-ray Imager,Synchrotron Radiation News,2014,Vol.27,no.4.
- [2] C.B.Wunderer et al.,The Percival soft X-ray Imager,JIST,2014.