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**Hit time calibration using Beam Interface information**

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19<sup>th</sup> July - 8<sup>th</sup> September 2016

## **Abstract**

This report describes methods of timing calibration for an analogue hadronic calorimeter (AHCAL) design in development for the International Linear Collider. Programs have been written in C++ which analyse hit-time data from the calorimeter and from an external clock, the Beam Interface. These programs are used to convert the TDC readouts from the calorimeter to real time measurement, and this time calibration functionality has been implemented in the online monitor for the AHCAL technological prototype. A discussion of this timing calibration method is offered, and suggestions for further developments of this TDC calibration are described.

# Contents

<b>1</b>	<b>Introduction</b>	<b>3</b>
1.1	The International Linear Collider . . . . .	3
1.2	The International Large Detector . . . . .	4
1.3	The Analogue Hadronic Calorimeter . . . . .	5
1.4	The AHCAL Technological Prototype . . . . .	5
<b>2</b>	<b>TDC Measurement and Calibration</b>	<b>7</b>
2.1	TDC Measurement . . . . .	7
2.2	Calibration of the AHCAL . . . . .	8
<b>3</b>	<b>Methods of TDC Calibration</b>	<b>9</b>
3.1	Data Set . . . . .	9
3.2	Correlation of TDC and BIF time . . . . .	9
3.2.1	Miscorrelation of Hit Time and BIF Time . . . . .	10
3.2.2	Saturation of Memory Cells & Wrong Validation Signal . . . . .	10
3.3	Relating TDC to nanoseconds . . . . .	10
3.4	Identification of Poor Channels in the AHCAL . . . . .	12
3.5	Future Developments . . . . .	12
<b>4</b>	<b>Conclusions</b>	<b>13</b>
<b>5</b>	<b>Acknowledgments</b>	<b>14</b>
<b>6</b>	<b>Bibliography</b>	<b>14</b>

# 1 Introduction

## 1.1 The International Linear Collider

The *International Linear Collider* (ILC) is a project for a future high-energy lepton collider based in Japan. It will be capable of energies up to 500 GeV, with the possibility of upgrading to 1 TeV. As shown in Figure 1, it will consist of an electron source, damping rings into which electrons and positrons will be injected, and two opposing tracks along which the particles will be accelerated towards a single interaction point. Positrons will be produced by colliding synchrotron radiation with a tungsten absorber and filtering the positrons from the resulting  $e^+e^-$  pairs.

The ILC project will continue the search for new physics performed at the LHC. Through the exploitation of the relatively low background for lepton-lepton collisions and its ability to control the spin of electron bunches, the ILC will allow for interesting research opportunities. For example, searches for evidence of supersymmetric particles and investigation into Higgs self-coupling will be possible, in addition to highly precise measurements of the properties of known particles.

There are two concepts in development for the ILC: the Silicon Detector (SiD) and the International Large Detector (ILD).

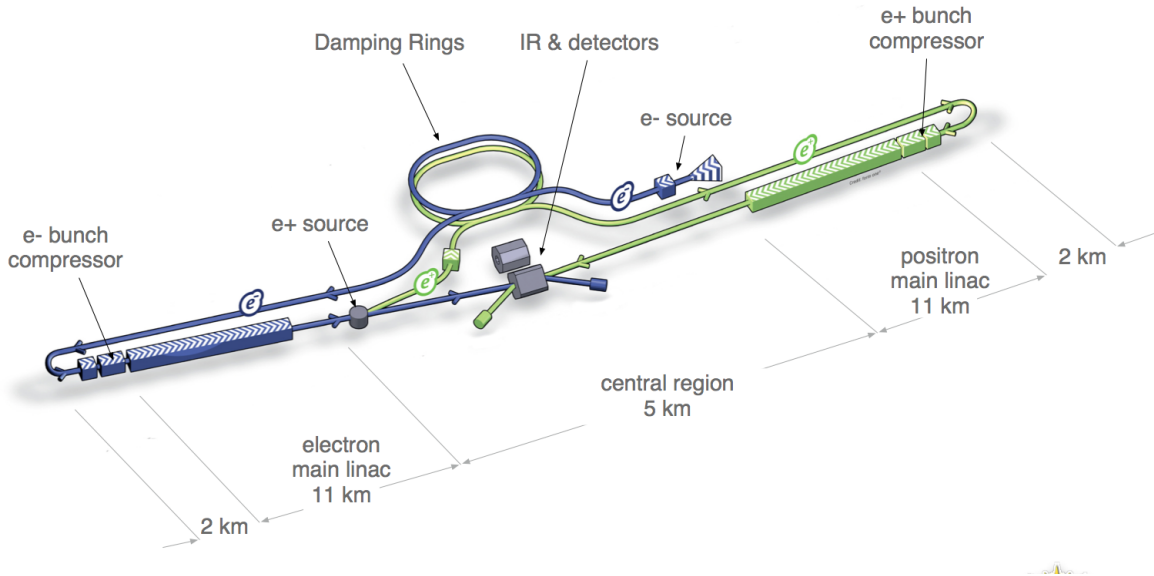


Figure 1: Schematic layout of the International Linear Collider

## 1.2 The International Large Detector

The *International Large Detector* (ILD) is a "barrel and endcaps" detector concept for the ILC consisting of several dedicated subdetectors arranged in layers around the beam axis. The detector, up to the calorimeters, will be contained within a superconducting magnetic field and will be able to reconstruct the energy of single particle jets through sophisticated tracking and highly granular calorimeters.

There are several parts of the detector, which are:

- **Vertex Detector (VTX)**

Used to measure the origin of the interaction point, this pixel detector can achieve a very high spacial resolution. Proposed designs include five single layers or three double layers of silicon around the beamline with an extra silicon strip around the endcaps to cover most of the solid angle.

- **Time Projection Chamber (TPC)**

The time projection chamber will contain a gas maintained at precise conditions. Anodes at each endcap and a central cathode will allow for the measurement of momenta of charged particles as they ionise the gas whilst traversing the chamber, enabling full 3D reconstruction of particles paths.

- **Electronic Calorimeter (ECAL)**

There are two designs in development for the ECAL; one of which consisting of layers of scintillator strips and tungsten absorbers to measure energy of electrons and photons, and another comprising of silicon pads.

- **Hadronic Calorimeter (HCAL)**

Layers of steel absorbers will be used to absorb energy of hadrons. Two methods of readout are in consideration: semi-digital and analogue. For the analogue approach, scintillator tiles and silicon photo-multipliers will be used.

- **Muon Sytem & Yoke**

An integrated iron yoke and muon system will track muons traversing the detector as well as catching hadronic showers that spread outside of the HCAL.

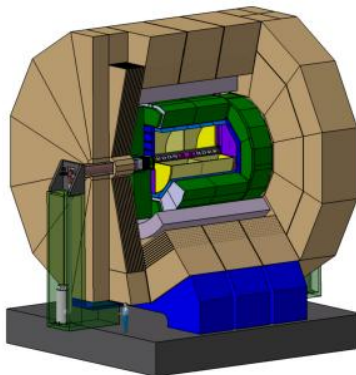


Figure 2: Design of the International Large Detector, showing concentric layers

### 1.3 The Analogue Hadronic Calorimeter

As mentioned previously, two design concepts for a hadronic calorimeter are considered, among which is the *Analogue Hadronic Calorimeter* (AHCAL). In development by the CALICE collaboration, it is a sandwich calorimeter combining 48 layers of steel absorber material and scintillator tiles. The scintillator tiles, which measure  $3 \times 3 \text{ cm}^2$ , are made from polystyrene and doped with a scintillating material. Photons colliding with the scintillating tiles will be captured and guided towards a silicon photomultiplier (SiPM), which is capable of detecting single photons, and a signal given off. Signals from triggered SiPMs are fed into a central chip, mounted on the readout electronics which fit in the constraint between the active layer and the absorbing material, and stored in analogue memory cells before being read out.

The steel layer (thickness 17 mm) along with the scintillator tiles and electronics (combined thickness of 8 mm) will give an overall thickness of each layer in the AHCAL of 25 mm. One layer in the full-scale AHCAL will comprise of 18 HCAL Base Units (HBU), shown in Figure 3. They are connected with flex-leads which carry voltage and read out signals between HBUs. These flex-leads connect the end of the layers to the Detector Interface (DIF) which is responsible for applying voltage to, and reading the signals from, the complete layer of HBUs. Each layer contains 2592 channels, giving a projected figure of  $\sim 8$  million channels for the full AHCAL.

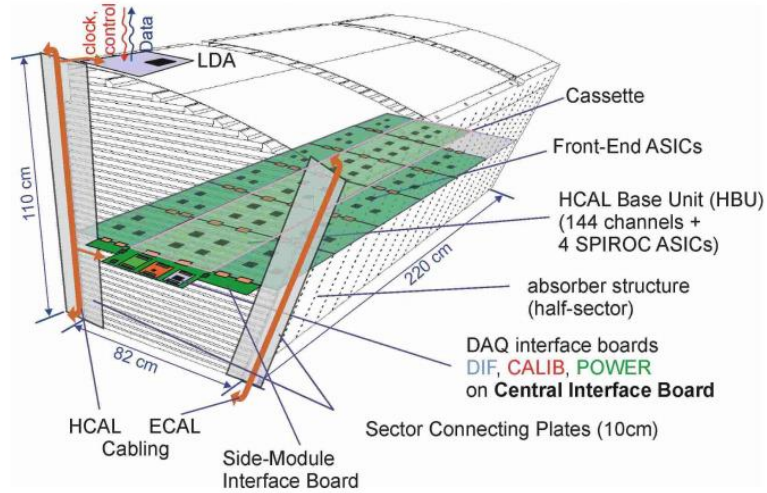


Figure 3: Design of the AHCAL, highlighting a single layer comprising of 3 slabs of 6 HBUs each

### 1.4 The AHCAL Technological Prototype

In order to demonstrate the physics principles of the AHCAL design, a *physics prototype* was developed. Comprising of 39 layers of absorbing material between layers of scintillator tiles, it has demonstrated that the AHCAL is capable of delivering the desired physics. The design is now into a second stage: the *technological prototype* (TPT). The TPT's purposes are several: to demonstrate the scalability of the AHCAL, the possibility of the components to be mass-produced, and to show how the electronics can be integrated fully into the layers of the calorimeter.

The prototype is complete with front-end electronics to control and read out information from the layer. This design of having electronics mounted at the front of the layers will serve to reduce dead material inside the calorimeter.

Mass production of the AHCAL is shown to be feasible with the inclusion of surface mounted

SiPMs which are attached directly on top of the electronics board. This will vastly increase production rates. Additionally, advances in SiPM technology have removed the requirement for wavelength-shifting fibres inside the scintillator tiles, which were necessary in previous designs to shift the photon wavelength into a region to which the SiPM was sensitive. To showcase this is another purpose of the TPT.

To demonstrate how the AHCAL design can be scaled up to full size, various tests have been carried out with different configurations. The purpose of these tests were to show that the flex leads connecting the HBUs were capable of delivering the correct voltage to each HBU and reading out correct signals. These arrangements of HBUs also prove that it was possible for the DIF to connect to more than one HBU and perform to required standards. In addition to this, further tests have been carried out with single HBUs arranged in layers to explore the AHCALs ability to read out signals from layer to layer. With the TPT demonstrating the scalability of the AHCAL in each dimension it can be shown that the full scale AHCAL will function well.

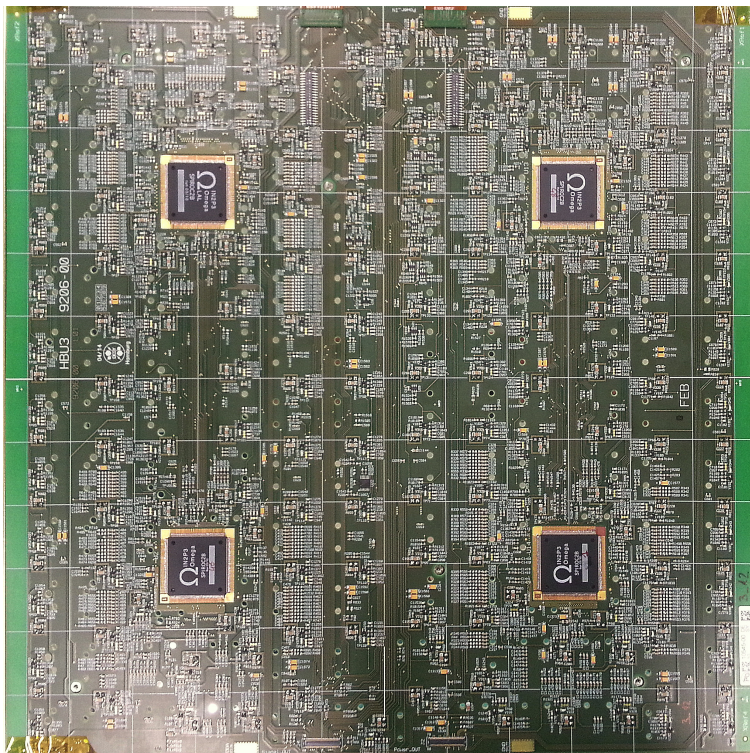


Figure 4: A single HBU, showing four SPIROCs and grid onto which 144 scintillator tiles are placed



## 2 TDC Measurement and Calibration

### 2.1 TDC Measurement

Each HBU in the AHCAL hosts four grids of 36 scintillator tiles with a central SPIROC TDC chip. The SPIROC is known as an application specific integrated circuit (ASIC) and has been designed to read out the signals from the 36 SiPMs on the board. It operates by utilising a capacitor which is charged with a constant current. This induces a voltage ramp in the chip which is switched off and stored in a memory cell when a signal is triggered from a SiPM. This amplitude can be converted to units of time (TDC), in order to produce a timestamp for each trigger, and read out by the SPIROC.

The capability of the AHCAL to produce a timestamp with each trigger will be of crucial importance to the analysis of events within the calorimeter. This allows showers to be separated by time during the reconstruction of events meaning that overlapping showers can be identified individually. It will also provide tool to analyse the nature of hadronic showers within the calorimeter.

The DIF operates on a clock cycle, represented in the top row of Figure 5. After each clock cycle the voltage in the SPIROC has to be reset. This causes *deadtime* in the chip when the capacitor is discharging, during which it cannot operate to interpret the SiPM signals sufficiently. In order to combat this issue, a second voltage ramp is introduced. Shown in Figure 5, this *dual ramp TDC* method addresses the issue of deadtime in the SPIROC by charging and discharging the two voltage ramps out of phase. The result, in theory, provides a continuously operating voltage ramp with no deadtime.

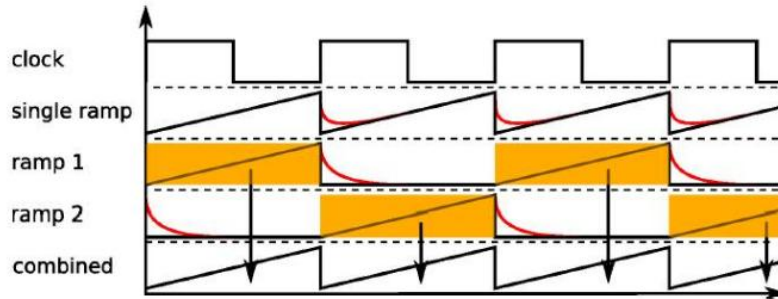


Figure 5: Working principle of the dual ramp TDC

There are two available frequencies of operation for the voltage ramps in the SPIROC chip, being *ILC mode* and *testbeam mode*. These modes match the frequency of the voltage ramp with the collision frequency of the ILC and testbeam. The switching between the two voltage ramps in the SPIROC is realised by a *multiplexer* which itself induces some dead time in the SPIROC, currently limiting its operation to frequencies similar to that of the testbeam mode.

Another aspect of the of the AHCAL design is the *external validate* feature. This limits those signals received and retained within the SPIROC to ones that have also been matched by a validation signal. If a channel in the AHCAL is triggered this signal will be stored in the memory of the SPIROC, and then either kept or discarded after the clock cycle of the DIF if a validation signal was or was not also received. In order for this feature to be effective precise timing of the validation signal is crucial.



## 2.2 Calibration of the AHCAL

From May 4<sup>th</sup> - 9<sup>th</sup> 2016, testbeams were carried out with a prototype of four "big" modules, which were made up of 2 x 2 HBUs per layer. Each scintillator tile in the setup is labelled with a unique set of coordinates (I, J & K) describing the layer to which each tile belongs, and their position within each layer. The focus of these testbeams were to perform the *Minimum Ionising Particle* (MIP) calibration and TDC calibration.

MIP calibration involves measuring the energy deposit of a particle, such as a muon, as it traverses the calorimeter. Its interaction with the calorimeter is so minimal that its energy deposits can be considered constant throughout each layer. This is the basis for calibrating the energy readouts of each tile in the AHCAL.

The TDC calibration, which is the subject of this project, was realised by the inclusion of the *Beam Interface* (BIF) which operates in parallel and independently from the AHCAL. It provides a timestamp of each hit in the calorimeter in units of nanoseconds which can be used to calibrate the data read out of the SPIROC in TDC units. The voltage ramp in operation during the acquisition of the SiPM signal will have a bearing on the relationship between the TDC readout and the real time value. This is addressed by generating a number, called the *Bunch Crossing ID* (BXID), and assigning it to the voltage ramp in operation each time the ramps alternate. The BXID allows for the identification of the voltage ramp belonging to any particular hit in the calorimeter, leading to greater accuracy in the conversion of TDC to nanoseconds and a more effective calibration. This method of calibration can be developed even further by considering the memory cell from which the hit data was acquired, as this will also affect the relationship between the TDC read out and the value in nanoseconds.

### 3 Methods of TDC Calibration

#### 3.1 Data Set

The data used for the analysis during this project is electron data, obtained from the May testbeam (merged runs 41145 & 41175) with the prototype set up described in Section 2.2. Each HBU contains 12 x 12 scintillator tiles, and the "big" layers are made from 2 x 2 HBUs. As such the chip coordinates describing the position of each tile, which are referenced in the following sections of this report, range from 1 to 24 in two dimensions (I & J) and from 1 to 4 in the third dimension (K).

#### 3.2 Correlation of TDC and BIF time

Correlation plots were generated with the data from May testbeam, with channel by channel separation. Data with even or odd BXIDs were also separated, such that each correlation plot is labelled by tile coordinates I, J and K along with a BXID of 0 or 1 (corresponding to even or odd bunch crossing ID respectively). Cuts on data were made in the initial stages of analysis in order to perform further analysis only for channels with a sufficient number of entries. Due to this cut, some channels within the AHCAL will not undergo any analysis, and will not be calibrated. So, by combining runs to get more statistics a more comprehensive analysis of the prototype can be achieved.

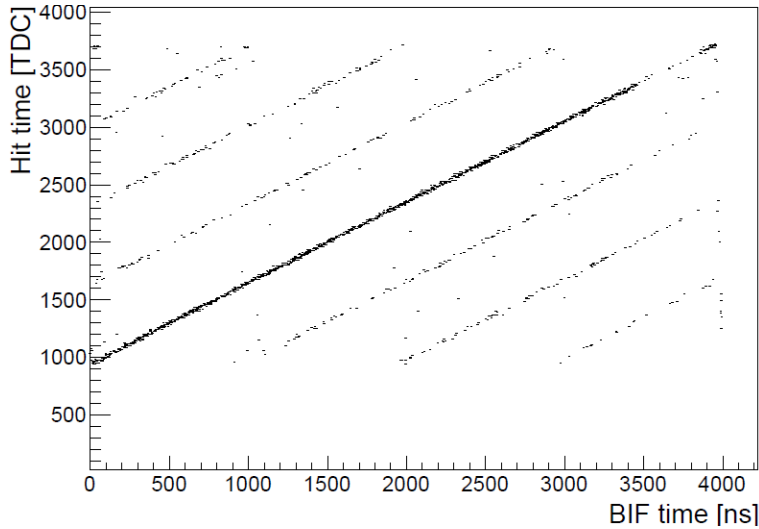


Figure 6: Correlation of hit time & BIF time for channel [I=12; J=19; K=4; BXID=0]

The resulting plots have some features of note. One can notice extra, fainter, lines on either side of the main line, as well as a strange distribution of hit time values in the region of 3500 to 4000 nanoseconds. Both phenomena are described in §3.2.1 & §3.2.2. These effects may be circumvented by making a cut to the data in order to eliminate the miscorrelations as well as disregarding the region of 3500 to 4000 nanoseconds when applying a linear fit to the data.

### 3.2.1 Miscalibration of Hit Time and BIF Time

The appearance of the extra lines in the correlation plots indicate miscalibration of the hit times in the calorimeter and the BIF. An explanation for this comes from the 1 MHz DESY testbeam structure, meaning that one can expect a hit in the calorimeter every micro-second. Coupled with the fact that one cycle of the BIF (one BXID) corresponds to four micro-seconds, this means that there will be up to four hits in the AHCAL for every BIF cycle.

When a SiPM is triggered in the AHCAL, a signal is sent both to the SPIROC and to the BIF, which provide timestamps in TDC and ns respectively. On occasions, a signal is missed by the SPIROC but is recorded by the BIF. If the SiPM is triggered again in the same BXID and both the SPIROC and the BIF receive the signal and record timestamps, then both recorded BIF timestamps will be attributed to the same hit in the AHCAL. The result is the appearance of the additional lines above the main correlation line. Conversely, if the signal from a triggered SiPM is received by the SPIROC but missed by the BIF, this also results in a miscalibration indicated by the extra lines below the main correlation line.

### 3.2.2 Saturation of Memory Cells & Wrong Validation Signal

The second phenomenon exhibited in the correlation plots was the saturation of the memory cells in the SPIROC. Signals in the SPIROC are read out by a 12-bit ADC, which allows for 4000 counts. For small signals corresponding to  $<4000$  TDC counts the signal size is related linearly to the TDC readout. For signals exceeding this upper bound, however, the memory cells in the SPIROC experience saturation and a readout of  $\sim 4000$  counts is observed, regardless of the true signal size. The values in the region close to 4000 ns are therefore unreliable and should be disregarded.

## 3.3 Relating TDC to nanoseconds

The next stage in the analysis of the May 2016 testbeam data was to perform a linear fit to the data using the correlation plots. Profile histograms were created for each channel (and BXID) and a straight line fitted to the data, with the aim of determining the slope and offset of the correlation. Initially the binned likelihood method was adopted when fitting the data as this seemed to give

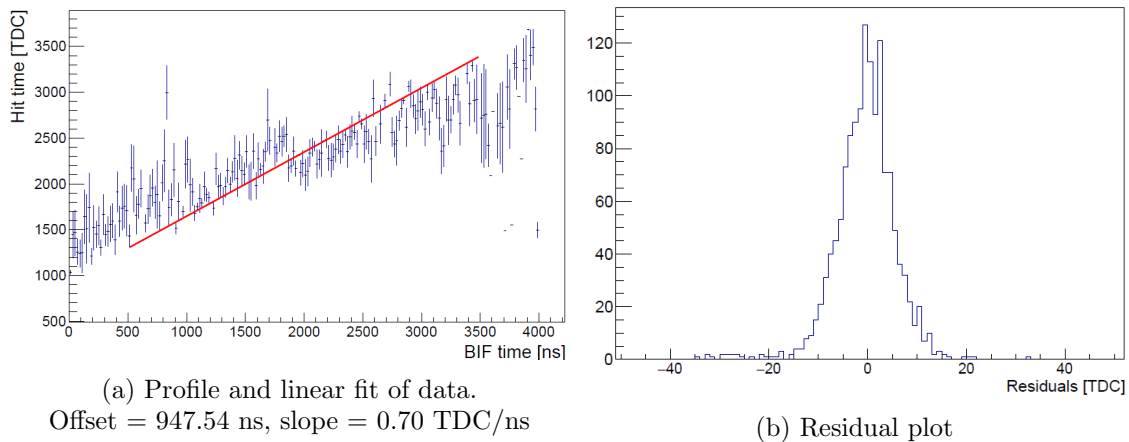


Figure 7: Profile histogram, linear fit and residual plot for channel [I=12; J=19; K=4; BXID=0]

a more accurate fit when judged by eye, however upon reflection of the residual plots which were subsequently generated this method was disregarded and a  $\chi^2$  method of fitting was used.

Upon an initial inspection the linear fits, such as the example in Figure 7, appear to be reasonably inaccurate. The residual plots however confirm that the fits are reasonable. One must also account for the miscorrelations of hit time and BIF time, which contribute to many of the outlying points in the profiles. The fitted polynomial intersects a distinct line of points with very low errors, which correspond to the main correlation in Figure 6, for which there are many entries.

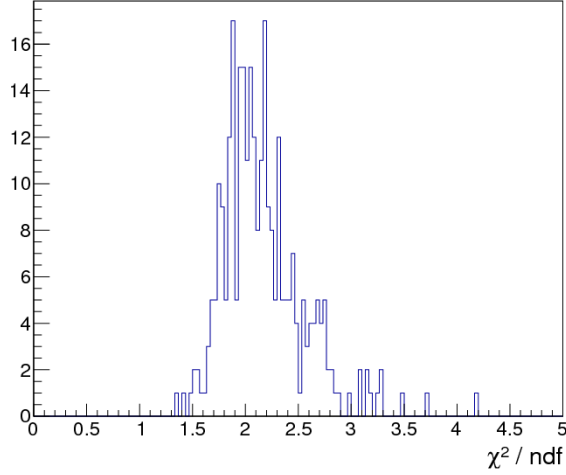


Figure 8: Distribution of reduced  $\chi^2$  for combined runs 41145 & 41175 (May 2016)

The parameters of the linear fits, being the gradient of the straight line and the intercept with the Y-axis, were recorded for each channel and stored in a text file for use in later analysis. These parameters could then be used to convert the hit times in the AHCAL from TDC to nanoseconds channel by channel. Calculations of the difference between the hit time in the AHCAL and the trigger time in the BIF were carried out, and a spectrum of the time difference for each channel was produced. Analysis of each channel could then be carried out, which included fitting the spectra

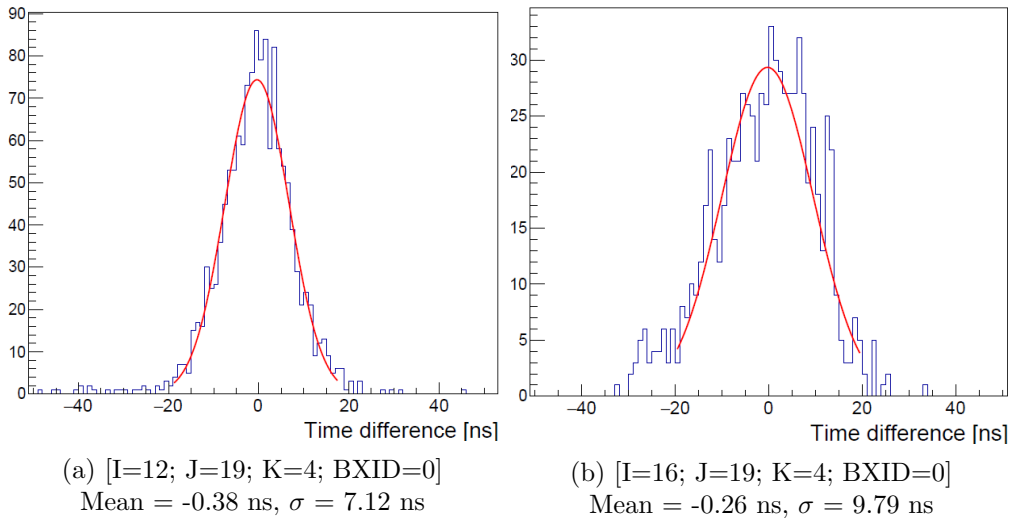


Figure 9: Plots of hit time (ns) – BIF time for two channels

with a Gaussian curve and counting the number of channels that had a reasonable value for the variance of the Gaussian. Each plot was fitted in the range of  $\{\text{mean value} \pm \text{rms value}\}$ . For the data from combined runs 41145 & 41175, the total number of channels analysed (channels with over 1000 entries, see §3.2) was  $\sim 300$ . Of these channels there were  $\sim 200$  that, when fitted with a Gaussian, had a sigma value of less than 20 nanoseconds.

### 3.4 Identification of Poor Channels in the AHCAL

Another aspect of these calibration methods is to identify channels within the AHCAL that are performing badly or may be faulty.

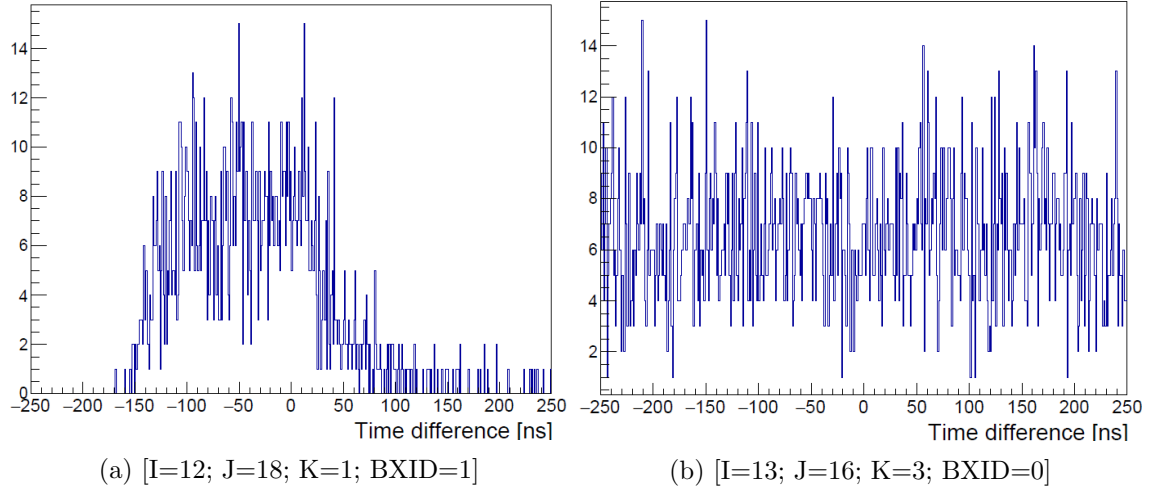


Figure 10: Plots of hit time (ns) – BIF time for two faulty channels

These occurrences are indicative both of possible hardware faults within the AHCAL, and the need for refinements to the time calibration procedures. These improvements, such as cutting data entries corresponding to the miscorrelations described in §3.2.1 and considering memory cells in the SPIROC, are described in further detail in §3.5. Hardware faults such as continuously triggering SiPMs can be detected by the appearance of chaotic plots, such as Figure 10 (b).

### 3.5 Future Developments

The methods of TDC calibration for the AHCAL explained in this report can be extended upon. One way by which this can be realised is by considering individual memory cells within the SPIROC. The SPIROC hosts 16 memory cells, in which the data from the SiPMs is stored. The chip will be filled with data which is then read out; this process being referred to as a *readout cycle*. Data belonging to different memory cells within the SPIROCs will result in different slopes when a linear regression is performed. Analysis performed with the assumption that each memory cell is identical will result in a spreading of the correlation plots, and a smaller degree of accuracy when the spectra of hit time(ns) – BIF time are drawn. Ultimately this will lead to a less meaningful calibration of the AHCAL, and so this extension should be considered in the future. Whilst effort has been spent during this project to make this extension to the calibration, more work is required before it can be implemented in the online monitor for the AHCAL.

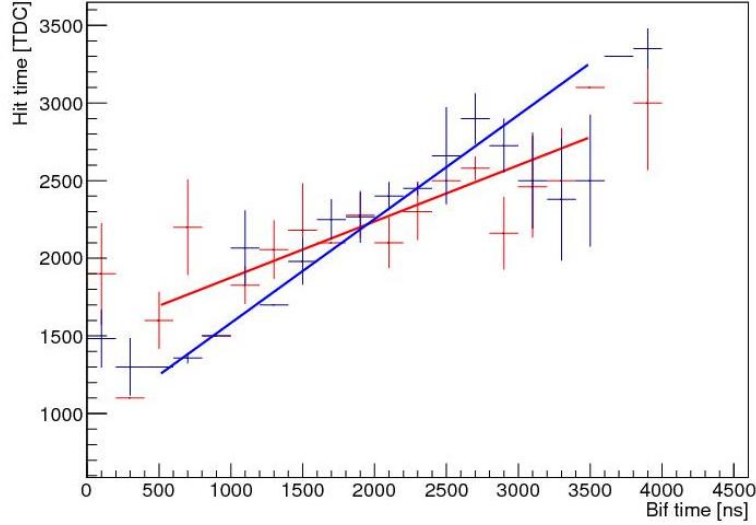


Figure 11: Profile histogram and linear fit for  $[I=12; J=19; K=4; BXID=1]$ , memory cells 2 & 3 for run 41145 data

Another area which will bring about an improvement to the procedure of calibrating the AHCAL is to make a selection on the data to cut out the miscorrelations, such as the ones shown in Figure 6. This has also been explored over the duration of this project however more work is required to design a method of performing this automatically to each channel before this implementation in the online monitor.

## 4 Conclusions

During the past 7 weeks TDC calibration functionality has been implemented in the online monitor for the AHCAL. This has involved writing C++ scripts with the function of performing analysis of the data from testbeam at DESY and investigating the relationship between TDC values and nanoseconds. Reconstructed runs from the May 2016 testbeam session have been used which contain additional data from the external beam interface.

The programs create correlation plots of hit time (TDC) and BIF time according to the chip coordinates I, J and K and bunch crossing ID associated with the hit time values. Profile histograms are then generated from these plots and a straight line fitted to the data. Analysis of the linear fits is performed by means of residual plots and the fit parameters, being the slope and offset of the straight line, are recorded for each channel. Further analysis is then carried out by using the fit parameters for each individual channel to convert the hit time values from TDC to nanoseconds and producing plots of hit time (ns) – BIF time values. These plots are used to evaluate the number of channels in the AHCAL performing to a acceptable standard, and identifying those which require attention.

During the process of writing the scripts, two particular reconstructed runs from May 2016 testbeam at DESY (combined runs 41145 & 41175) were used. Analysis of this data suggested that around 65% of channels were functioning to a high standard. This value can be improved upon by extending the programs such that memory cells are considered within the SPIROCs. Additionally, the data can be cut in order to eliminate miscorrelated data. Both of these improvements should yield a higher and more accurate value of the fraction of channels performing well.

## 5 Acknowledgments

My sincerest thanks goes to Huong Lan Tran, my supervisor, as well as Eldwan Brianne for their continued support, kindness and patience during my time at DESY. They have helped me to learn an incredible amount, for which I am hugely grateful.

I would also like to offer my thanks and appreciation to Katja Krüger, Doris Eckstein and Olaf Behnke for their help and support during this summer program.

The DESY summer student program has been an invaluable experience for me, allowing me to broaden my horizons academically and beyond. Thanks to everyone who made it special.

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