Design and Simulation of Time-to-Digital Converter for Readout Electronics of SiPM Detector

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This report presents the design of a high-resolution Time-to-Digital Converter (TDC) to be used as one component in readout electronics of Silicon Photomultiplier (SiPM) based digital imaging system. The architecture consists of 6-bit digital counter as a coarse counter and 6-bit Delay Locked Loop (DLL) as a fine counter to further increase resolution up to 76 ps. Design consideration, DC, Timing, and Monte Carlo simulation results, and suggestion for further improvements have been reported.

Table of Contents

1. Introduction to SiPM Imaging System

DESY FEC group, in collaboration with MPG-HLL Munich, is currently developing Silicon Photomultiplier (SiPM) based digital imaging system for application in high energy physics and photon science. The idea is illustrated in Figure 1. SiPM is actually an avalanche photodiode (APD) operated with reverse bias voltage above the breakdown voltage or Geiger mode. Low intensity signal, down to the single photon, can generate carrier that triggers an avalanche current up to mA range, due to the impact ionization mechanism. The fast increasing edge of current pulse can be marked as arrival time of detected photon. The next photon detection can only be done after the avalanche is quenched by lowering the bias voltage, and restoring back to operative level. Our system uses SiMPl developed by MPG-HLL, which has quenching resistor integrated into silicon bulk on each sensor pixel.

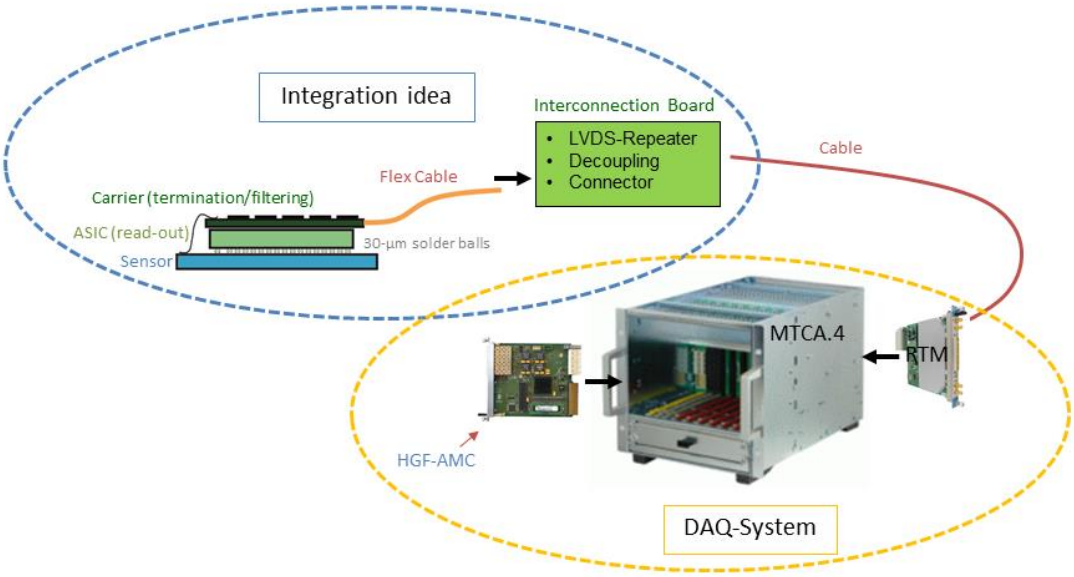


Figure 1 Digital SiPM Imaging System

In order to digitize pulse signals and convey information about energy and time, we need readout electronics or ASIC. Each pixel is bump-connected with cell electronics, consist of active quenching and recharging circuit (AQRC), hit counter, pixel masking, and serializer. Each sensor pixel is biased with AQRC that helps to speed up quenching and recharging process, or in other words, to decrease dead time. The intensity of the photon is obtained from hit counter within fixed measurement time slot. The first firing pixel draws current from wired-OR connection to all pixels in one quadrant, generating fast trigger for timing information. Additional validation logic is added with adjustable comparator threshold in order to suppress undesirable events such as thermally generated carriers. Initial key parameter for this system is given as follows.

- Tracking and photon detector, 50x50 um pixel area, 16-by-16 pixel unit per quadrant
- 3-MHz frame rate (bunch clock), 204 MHz system clock
- 100-ps timing resolution
- 1 ns fast trigger (1 of 256 wired-OR connection) to record timing data

- 0.7s 21-bit bunch-counting depth
- ns-range combinational trigger (validation logic with N-of-16 row comparators)
- Adjustable veto-window size providing Dark Event suppression
- Continuous readout of hit matrix and timing data

Proposed scheme of readout electronics of each quadrant is shown in Figure 2.

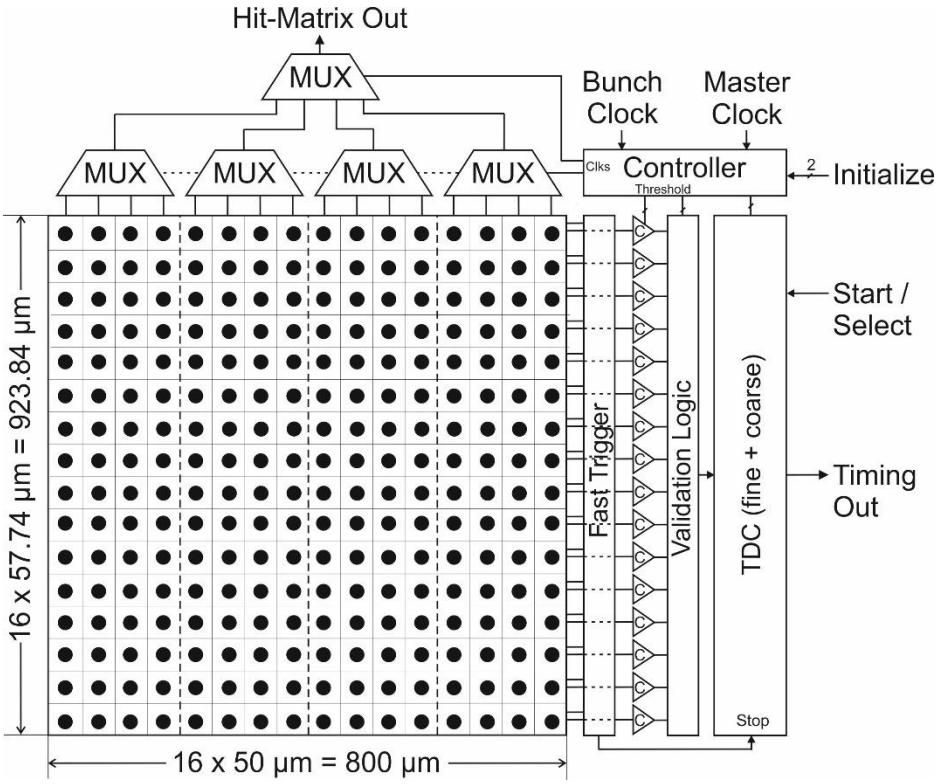


Figure 2 Readout Electronics for Each Quadrant

2. Time-to-Digital Converter

2.1. Theory

In order to measure arrival time of the photon in accurate way, we need a component that can quantize the time difference between clock reference and trigger pulse coming from the pixel electronics. There are two general ways to achieve that, either analog or digital approach. In analog way, we can generate voltage signal proportional to time difference, and then the voltage signal can be measured using Analog to Digital Converter (ADC). But, as an impact of CMOS technology scaling, analog signal processing is not preferable anymore due to dominant physical noise in deep-submicron technology. Therefore, nowadays, Time-to-Digital Converter (TDC) has been employed widely to do accurate measurement of time interval between two physical events, since it works generally faster, less supply voltage needed, and less prone to noise.

TDC is usually designed in ASIC methodology, which has specific requirements of each types of application. There are several parameters that characterize the TDC performance, shown in Table 1.

Table 1. TDC Performance Figures

Parameter	Definition	Initial Spec
Resolution	Minimum change of input interval that can be resolved by TDC	100ps
Dynamic Range	Maximum time interval to be measured	64*resolution
Offset Error	Digital output word for zero time interval	Near zero
Gain Error	Deviation of actual slope from ideal converter characteristics	Near zero
Integral Nonlinearity (INL)	Absolute deviation of midlevel of each step from straight line between first and last step (accumulated)	Less than 1 LSB
Differential Nonlinearity (DNL)	Deviation of actual step width from ideal one	Less than 0.5 LSB
Single Shot Precision	Standard deviation of measurement values acquired for several measurements of the same constant time interval inputs	Less than 1 LSB
Conversion Time (latency)	Time required to compute the measurement value after a start (stop) event is captured	As small as possible
Dead Time	Inert period after a measurement before the TDC can be used for further acquisitions	As small as possible

The target specification for resolution is already given, 100ps, although improving it is always appreciated. Since we will have continuous readout of hit matrix and timing data, we should have, without considering dead time, maximum delay to be measured around 1/204MHz = 4.9 ns. Since we will implement it in form of integrated circuit, power and silicon area consumption can also

be added as design limitation. But, in this case, if there is no specific limit, then smaller power and area consumption is always preferable.

There are various method to implement TDC, some of which will be discussed in following section, such as digital counter and tapped delay line. With using digital counter, the start signal enables the counter and stop signal disables it. Since it is digital circuit, it is very fast, stable, and provides wide dynamic range. But, the achieved resolution is exactly equal to 4.9ns, the period of the system clock. Hence, there is delay error between asynchronous trigger signal and rising edge of the clock. Increasing the clock frequency will give rise to more power consumption and clock jitter. In order to achieve 100ps delay range, we need a component that can generate that delay. The easiest way to generate such short delay is by using inverter or buffer gates.

Resolution can be increased to below period of system clock by using delay line. The system clock signal as reference is used as the start signal, to generate its skewed version. The stop signal then performs as sampling trigger using flipflop to 'tap' the state of delay lines. At the arrival of stop signal, all delay stages which have been already passed by start signal will have '1' output, and next following stages will have '0' output. This creates thermometric code at the output of flipflop proportional with time difference between start and stop signal. The illustration of the tapped delay line operation can be seen in Figure 3.

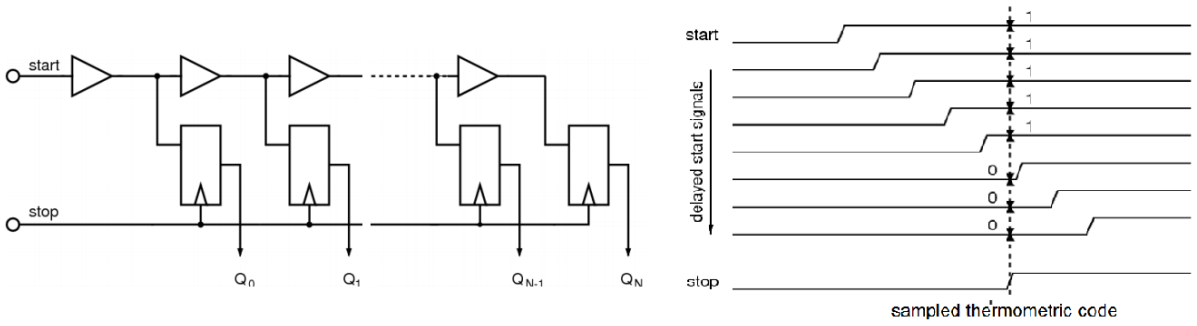


Figure 3 Tapped delay line structure and operation

In this case, the resolution is defined by propagation delay of buffer or delay elements (DEs), while the dynamic range is defined as total delay generated by delay stages. Since we need 100ps delay range, we can use 64 DEs, so the resolution can reach 4.9ns/64 = 76ps. Although this approach seems to be straightforward, there are some problems, for example, nonlinearity of propagation delay on each elements. Process, voltage, and temperature variations can deteriorate the accuracy of the delay, as well as different loads suffered on each point in delay line. Also, long chained delay elements tend to have more nonlinearity than the short chain, as deviation from ideal measure always accumulate. We need some feedback mechanism to create more stable propagation delay during various conditions.

Negative feedback control can be employed in an implementation so called Delay Locked Loop (DLL). The concept of DLL is quite similar with Phase Locked Loop (PLL) to generate synchronized signal. The idea is to force the delayed start signal at the end of the delay line to have the same phase as the original start signal. If, for example, the signal phase on the end of delay line is faster than on the beginning, the feedback tries to act by increasing propagation delay of each delay element, hence, signal phase now should be closer to each other. The feedback

action is done by phase detector and charge pump. Also, this approach needs more sophisticated delay elements, since we need to control the propagation delay by means of controlling bias voltage, varying capacitances, or other ways. Illustration of DLL can be seen in Figure 4.

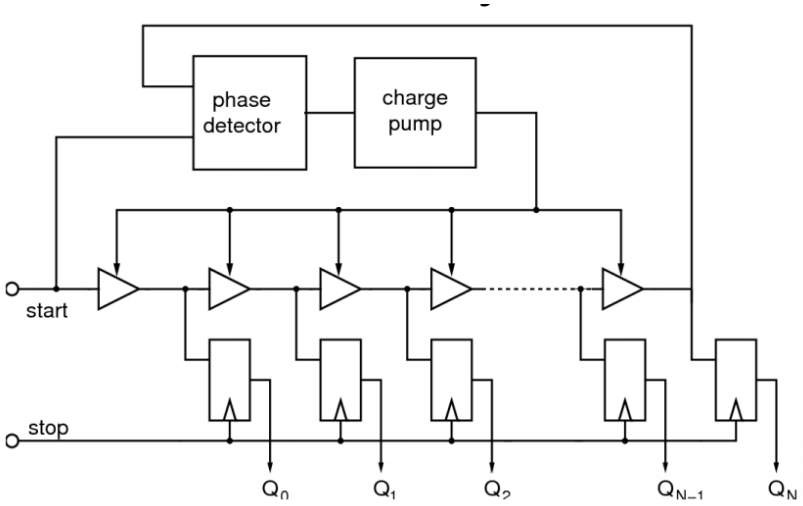


Figure 4 Delay locked loop structure

In this topology, small variations due to PVT variations may be acceptable because of the negative feedback action, but still, the ability to synchronize is always limited by delay range variations of each delay element. Therefore, delay element with wide delay range is preferred. However, the problem of nonsymmetrical load on different points in delay stage is still unavoidable, in this case.

2.2. Proposed Architecture

The hierarchical TDC that combines digital counter as coarse counter and DLL as fine counter, may be sufficient enough to meet the specification of our system, since it has wide dynamic range but can provide sufficient resolution. Our proposed TDC architecture is shown in Figure 5. In the following section, each components that constitute above architecture will be explained in detail.

2.2.1. Delay Elements

The chain of delay elements, commonly couple of inverters creating delay lines, are the basic building blocks of DLL. In order to react with phase difference between signal in the beginning and end of delay lines, we should have variable delay elements (DEs). According to how we can control the delay time, there are two types of DEs, namely digitally controlled (DCDE), which we have discrete change of delay time, and voltage controlled (VCDE), which is rather continuous. In this feedback system, VCDE is preferred, since it may have faster response and more flexible delay change. Also, the digital one usually employs a branch of transistor for each delay change, which might takes up a lot of silicon area. Figure 6 shows example of DCDE.

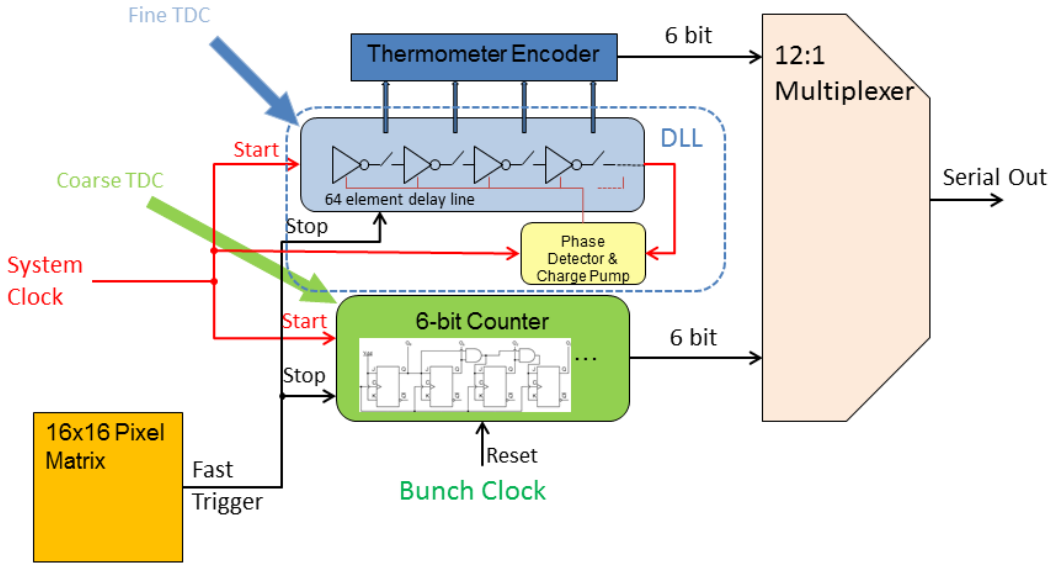


Figure 5 Proposed TDC architecture

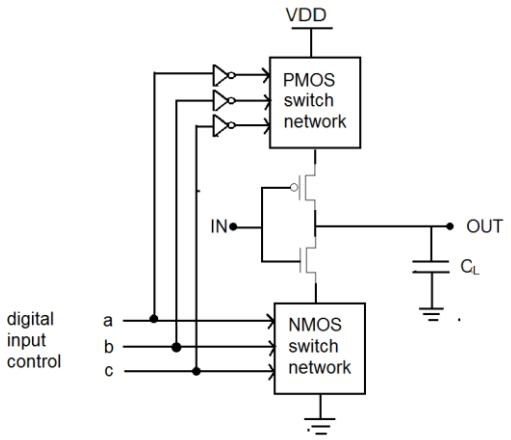


Figure 6 Digitally controlled delay element

There are two common technique to realize the VCDE, which are current starved DE and shunt capacitor DE. We should bear in mind that rising and falling time of inverter is proportional with equivalent resistance and capacitance seen from output node. The idea of current starved DE is that, we try to regulate maximum current allowed in each of inverters, or in other words, control equivalent resistance seen from the output node. Equivalent resistance can be controlled by adding transistor in series with the core transistor, and biasing that transistor directly or by using current mirror structure. On the other hand, in shunt capacitor DEs, we try to regulate (internal) capacitance seen from the output node. Several of the basic configuration can be seen in Figure 7. Both of the approach even can be seen in one design. In the range of ~100ps delay, usually MOS internal capacitor is employed in delay element instead of dedicated capacitor. But, this approach takes up more area compared to current starved elements, and capacitance itself has

nonlinear characteristics and very narrow tuning range. Therefore, current starved element is preferred in this application, although the delay-voltage relationship may not be completely linear due to natural I-V characteristics of MOSFET and it may take more power due to dc current.

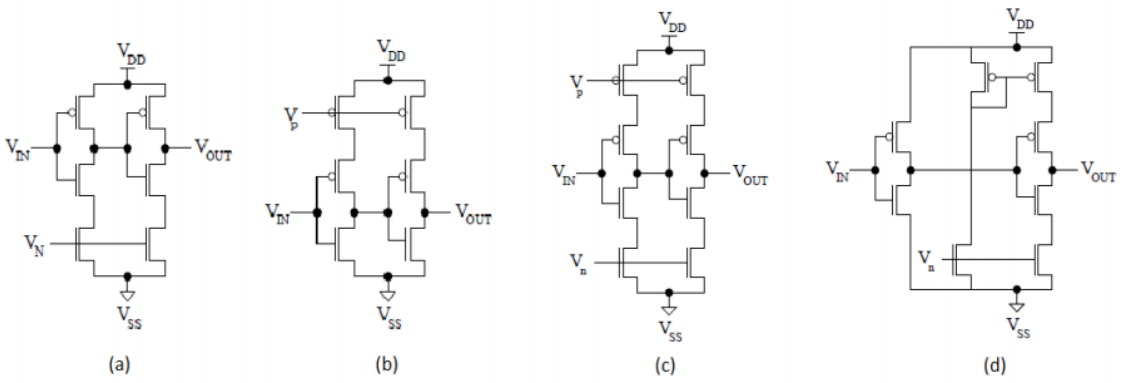


Figure 7 Some basic examples of voltage controlled delay element

In addition to basic topology, we need also to consider PVT variations that can lead to huge deviation from target delay range. In this project, we try to use several approach to suppress these effect, particularly due to process corners. One approach is to inject additional current directly on the delay element, another approach is to inject additional current on the bias circuit for delay lines. The obvious effect of both approach is that, when additional current branch is activated, minimum delay time will decrease, therefore will adapt better in slower process corners. In application, the compensation can be digitally controlled from control register of external interface, in case of process variations that indeed happens. Both proposed topologies can be seen in Figure 8.

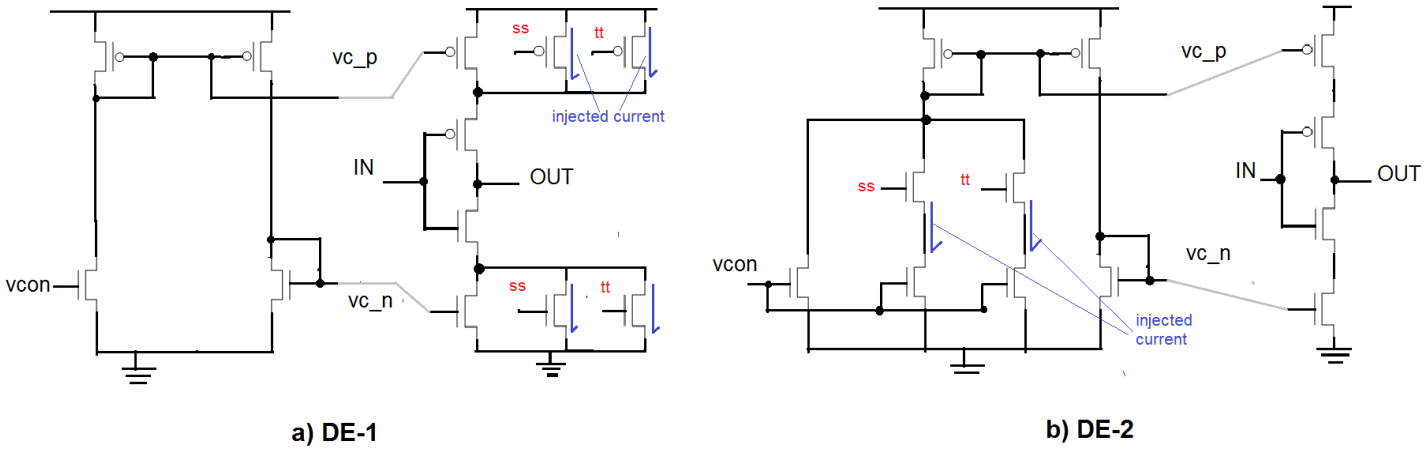


Figure 8 Proposed DE 1 (left) and DE 2 (right)

In this case, we use single ended delay element, rather than differential delay element. The differential delay element is not presented in this report.

2.2.2. Phase Detector

Feedback mechanism in DLL is implemented using phase detector and charge pump. Recalling the concept of phase locked loops, output phase of Voltage Controlled Oscillator (VCO) can be aligned with phase of reference using phase detector. The PLL is said to be locked when there is negligible change of phase difference between output and reference through time, hence, have the same frequency. The phase difference itself might be zero or finite. In DLL, basically VCO is replaced by voltage-controlled delay line. In this case, phase detector is used to determine when output of delay line and reference signal, which is system clock, are aligned or not. In this case, we will use so called Phase and Frequency Detector (PFD), the improved version of phase detector, having more lock acquisition range. The basic scheme of PFD is shown in Figure 9.

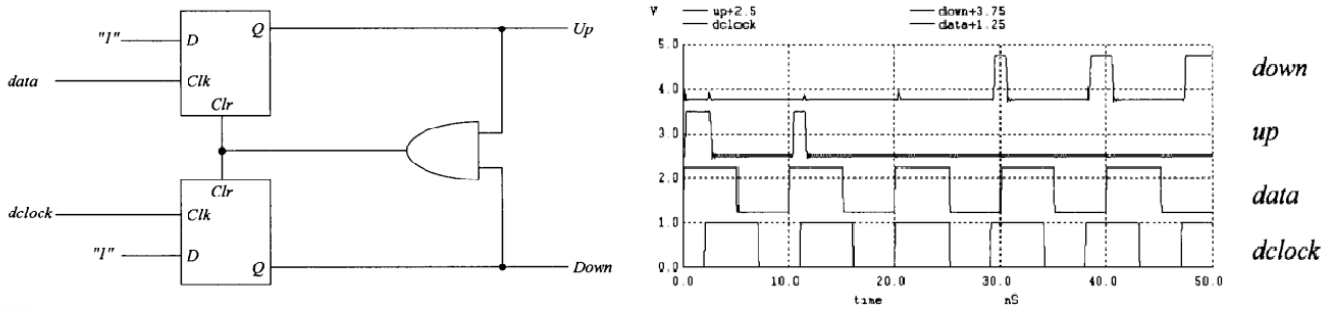


Figure 9 Basic scheme of phase and frequency detector and its operation

Some of the parameters for PFD are width of up/down signals, jitter, and dead zone. Width of up/down signals will be proportional with locking time or response time of the closed loop system. Jitter in this case is unwanted output false due to component mismatch, noises, or asymmetrical circuit topology that can give false up and down signal to charge pump. Dead zone is a range which the phase difference is so tiny that PFD doesn't give any output corresponding to that input. This parameter relates to static phase error.

There are several circuit topologies to implement PFD, which three of them will be compared in this report, namely Bangbang PFD, Static PFD, and Dynamic PFD. In Bangbang PFD, up and down signals are changed periodically when inputs have tiny phase difference due to the two-state detection mechanism. This results in higher width of output pulses, but have periodical ripples during locking condition, wasting power. Other two types of PFD has three-state detection mechanism, which there is no output pulses when the phase difference is inside deadzone. This results in smaller width of output pulses but more stable system. The schematics will be presented in another section. In static configuration, the delay through two inverters can be used to set how up and down behave as the PFD inputs move close together, therefore, controlling the deadzone.

2.2.3. Charge Pump

In PLL, loop filter is generally needed in order to remove high frequency behavior from phase detector, since VCO input should have rather stable input. In DLL, charge pump (CP) is widely used as indirect loop filter. Charge pump acts as a control for voltage-controlled delay line. Using information from PFD, charge pump tunes control voltage, either it needs to be increased or

decreased, to get proper delay for each delay element and achieve 'delay lock' condition. Figure 10 illustrates charge pump scheme.

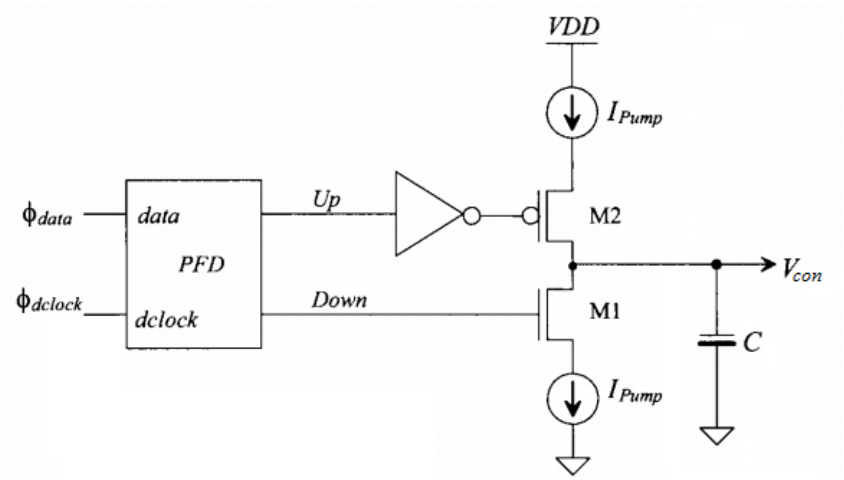


Figure 10 Charge pump scheme

We can also see that the choice of current source and capacitance is important in determining response time and behavior of its negative feedback. Current source must be matched between pull up and pull down network to ensure linearity. The performance can be made better by using mirror structure, in order to make fixed current independent of the input signals. Commonly, we can use ratio of current pump (I) and capacitance (C) to determine the behavior. High I/C ratio (higher current source and less capacitance) implies faster response but tends to fluctuate during lock condition. Low I/C ratio (less current source and higher capacitance) implies slow response and limited lock acquisition range, but more stable and less jitter.

2.2.4. Other Components

We need 6-bit counter synchronized with system clock that acts as a coarse counter. The counter should be enabled with the rising edge of the system clock and sampled by stop signal in order to find number of clock period in between hit signals. The thermometric-to-binary encoder is also needed to generate binary-coded output from buffered delayed signals from delay line and save output bits. In addition, multiplexer is needed at the output side to convert 12-bit parallel output bits to 1-bit wide serial stream of timing data.

3. Circuit Design and Simulation

Circuit design and simulation are all done under Cadence Design Environment, particularly Virtuoso Analog Design Environment L/XL/GXL. After implementing circuit topology for each component, sizing its transistor, and constructing the overall feedback system, we need DC and timing simulation to investigate operating points of each transistors and define typical timing operation. In addition, we also need Monte Carlo simulation to consider effect of process and mismatch variations to circuit performance, especially for delay elements, which is very crucial in determining accuracy and resolution of time measurement.

3.1. Components

3.1.1. Delay Elements

The circuit schematics of two delay elements and its bias circuit are shown in Figure 11 and 12.

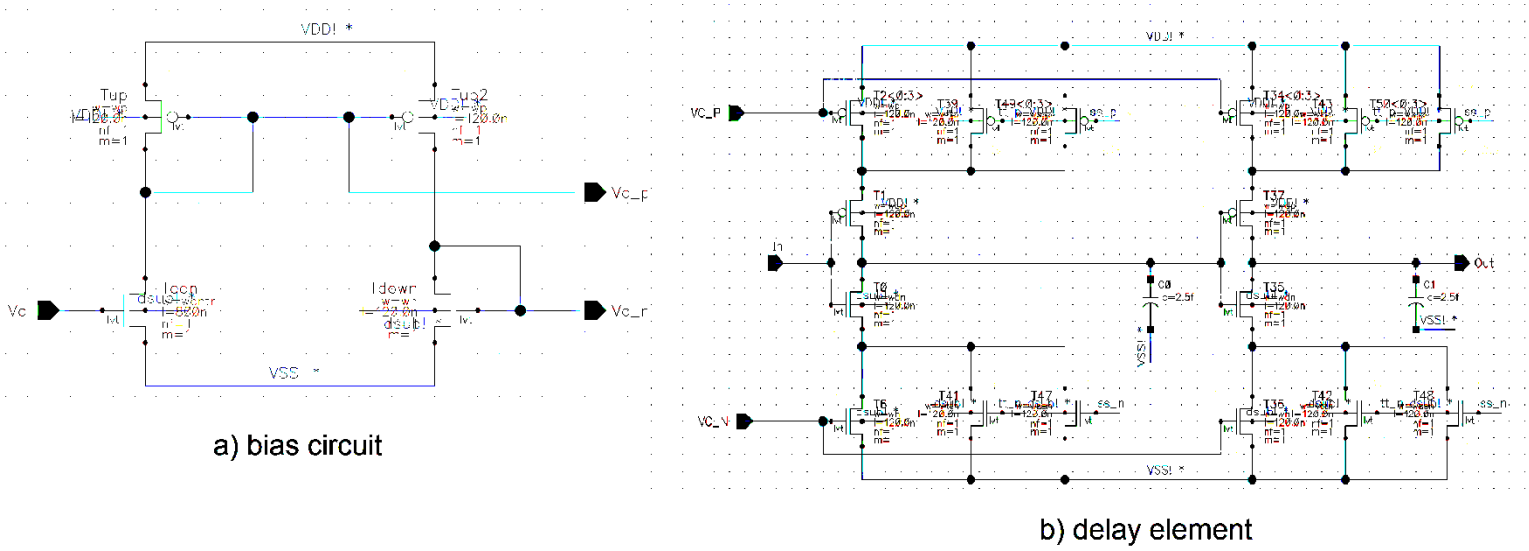


Figure 11 Schematics of DE-1 and its bias circuit

wcntr	wp	wttp	wssp	wdp	wn	wttn	wssn	wdn
1.2u	4u	360n	800n	1.5u	3u	280n	600n	1.5u

There are several sizing rules followed in this design. First, the basic design starts from the worst process corner (ss = slow PMOS, slow NMOS), then proceeds to the better process corner (typical and ff = fast PMOS, fast NMOS) by adding compensation based on each topology. In the end, we can evaluate the delay range of each condition and make sure that it includes the target of nominal delay 76.5 ps. Transistors in mirror structure are set to be the same aspect ratio, even though it has different fingers, in order to ensure saturation region and create strong current mirroring effect. PMOS and NMOS transistors must be sized accordingly in order to achieve same maximum current on pull up and pull down network, since equal rising and falling time is important in this application. Also, the size of mirror transistors are bigger than transistor near

the output node of inverter, in order to dominantly control maximum current in inverter structure, therefore, better delay control. Inverter transistors width are sized properly, too small will limit delay range and minimum delay possible, too big will result in lower delay compared with target delay. Additional model capacitance of 2.5fF is added on each stage of inverters, taking into account parasitic capacitance that might be dominant after layout design is extracted.

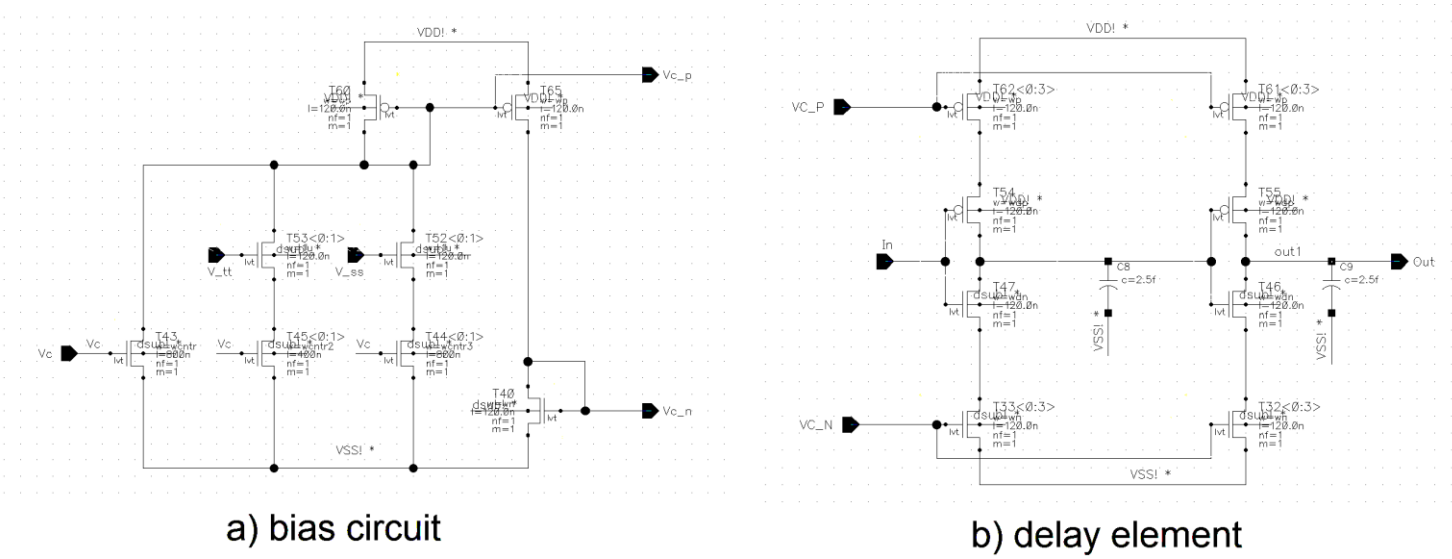


Figure 12 Schematics of DE-2 and its bias circuit

wcntr	wcntr2	wcntr3	wp	wn	wdp	wdn
250n	250n	1.2u	2.6u	2u	1u	1u

Simulation of delay range on each delay element is run in delay line consisting of 8 delay elements in series, considering that the load suffered is more or less the same with actual design of 64 delay elements in series. The transient data are taken from delay element in the middle of the line. The relationship between delay and control voltage can be obtained, like in Figure 13 and 14.

As we can see, there is no significant difference between rising and falling time of the signal, thanks to the ratio between PMOS and NMOS. The delay-control voltage relationship is rather nonlinear. When the control voltage is nearby threshold, the delay is very sensitive to control voltage, resulting in huge possible fluctuation during lock acquisition. On the other hand, when the control voltage is off from threshold, the delay trend has rather linear. This is common relationship in current-starved configuration. During transistor sizing, the target is to put the bias voltage in around middle of VDD, 0.6V, in order to get maximum possible delay deviation from target value. In DLL, wide delay range is more preferred than perfect linear response. In addition, we always find that delay range decreases as we move to slow process corner. This is because process corner change mobility of carriers, less mobility means that applying voltage on gate-source affects less current modulation on transistors, then less current modulation means less

delay range. Moreover, inverter transistors are unchanged in every process corners, even creating more restricted delay range.

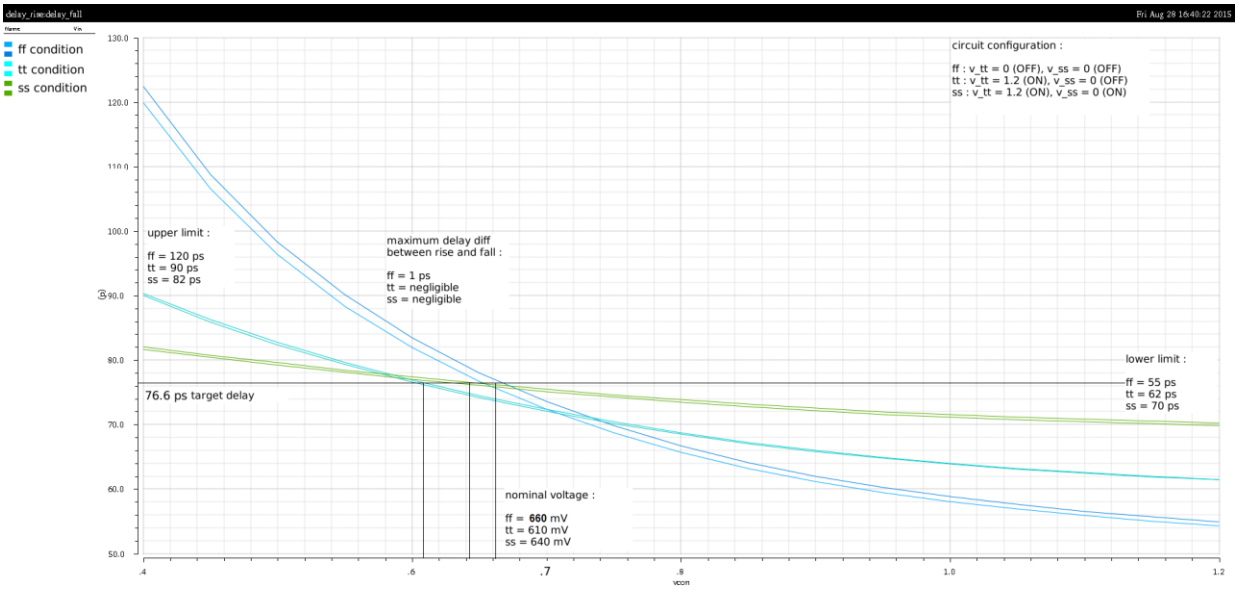


Figure 13 Delay range of DE-1

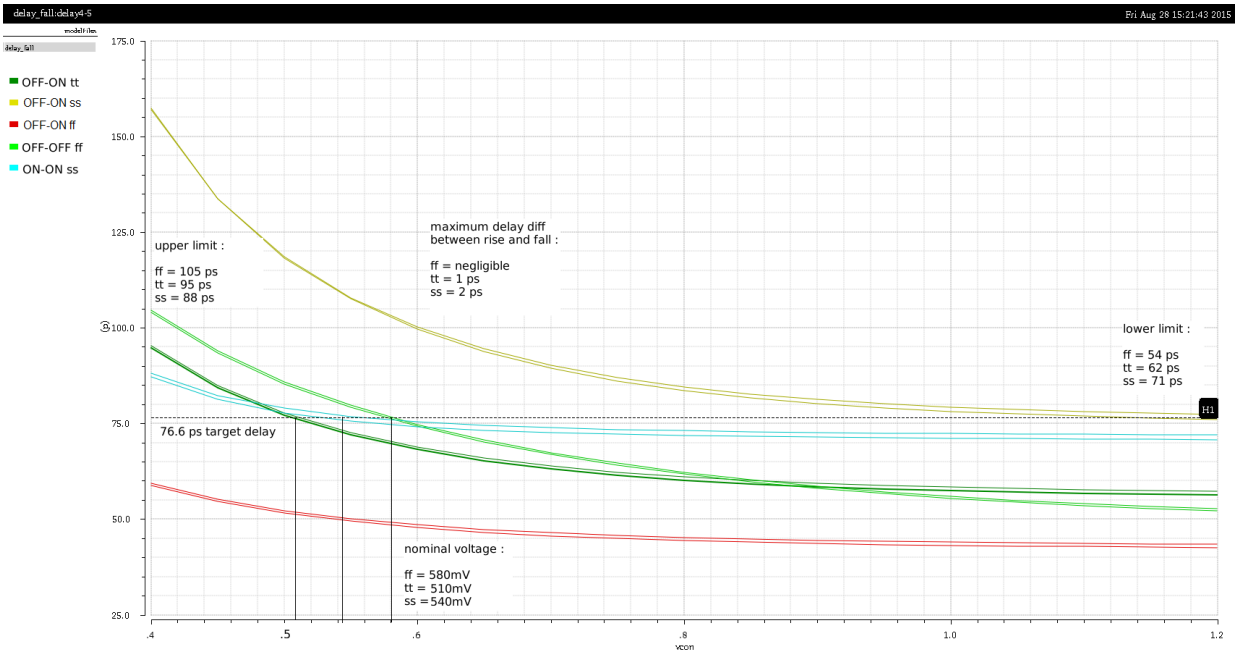


Figure 14 Delay range of DE-2

In DE 1, we can see even huge amount of delay range decrease between ff (120-55=65ps range), tt (90-62=28ps range), and ss (82-70=12ps). This is because of the fact that only portion of currents in inverter directly controlled by external voltage. This is different in case of DE 2, while

injected current in bias circuit is still controlled by external voltage, resulting in slightly better delay range.

In this configuration, we can also evaluate the uniformity of propagation delay by comparing delay from each of delay elements in the line, in every process corner condition. In this simulation, 64 delay elements in series are used, in both DE types and three process corners. The simulation results and summary are given in Figure 15.

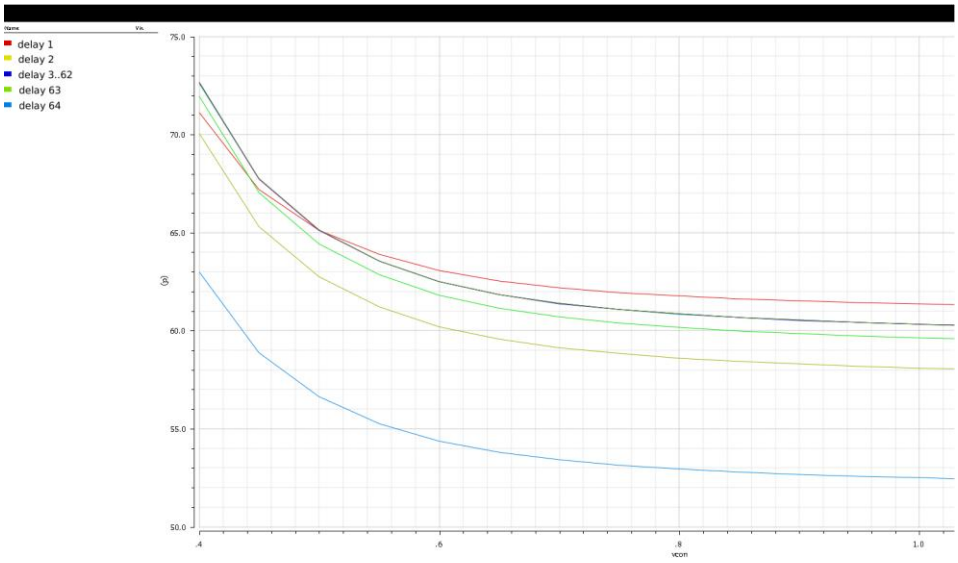


Figure 15 Nonuniformity of delay range in sample delay line, tt condition

The results point out that the delay is at some extent deviated from nominal delay range in the beginning and in the end of delay line. If we tap the signal from those points, the deviation from desired value, or INL and DNL, might be huge. We can reduce the nonuniform loading effect by adding at least two dummy delay elements in each ends of line. The feedback system is only applied in the middle of the line, so that the loading effect is considerably similar on each tapping point.

We also need to consider the delay change due to other variations, like voltage supply and temperature variations. Using typical process condition, both delay elements are tested in different V and T conditions, resulted in Figure 16 and 17.

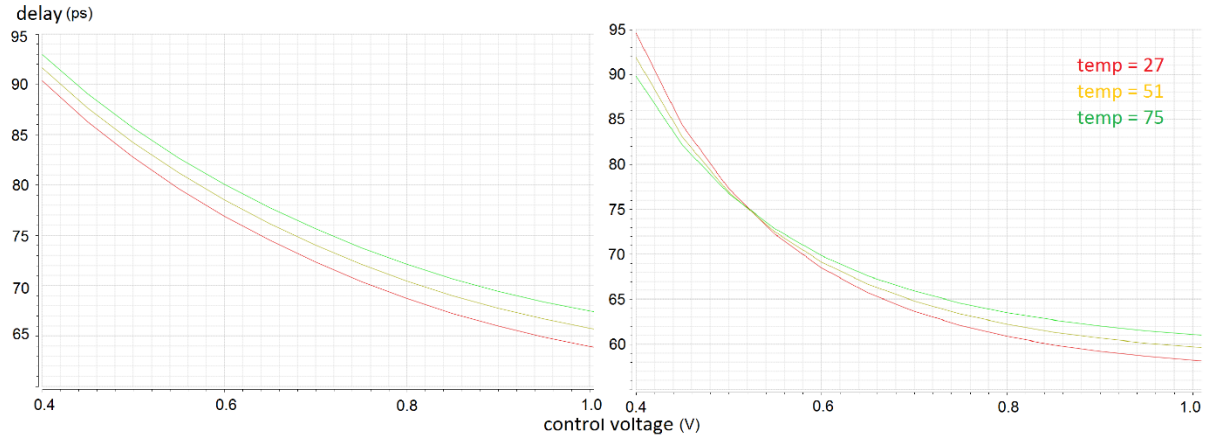


Figure 16 Simulation of delay range DE-1 and DE-2 (right) with temperature variations, tt.

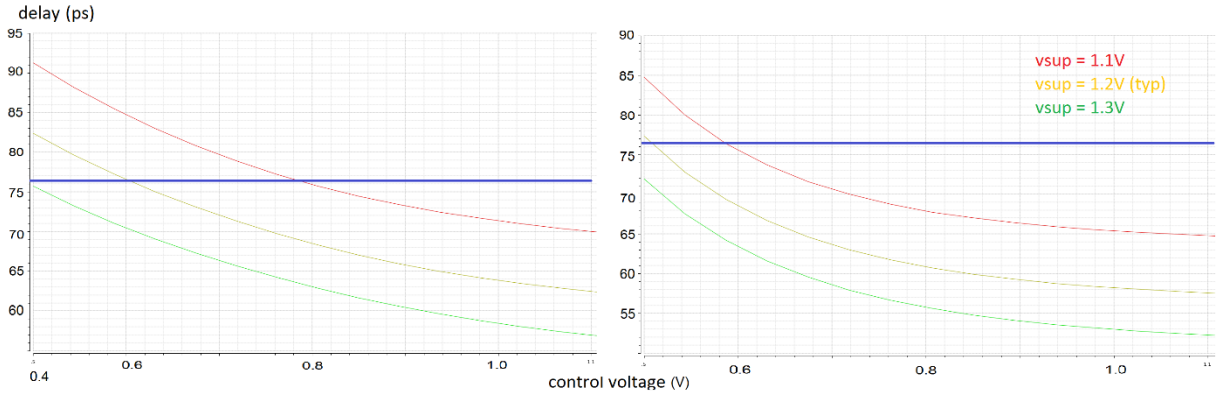


Figure 17 Simulation of delay range DE-1 and DE-2 (right) with voltage supply variations, tt.

Under temperature variations, DE-2 has better response since delay value near nominal is slightly disturbed compared with delay value near limit of the range, which diverges around 2ps. However, the DE-1 response is also acceptable since it only gives around 2ps offset to delay value. Under voltage supply variations, both delay elements have similar response, with delay offset between 6ps and 8ps. Since the variations of the delay is still in the delay range of each elements, the variations can be fully compensated by its own negative feedback. **This problem needs to be taken into account when under ss process corner whose delay range is less than tt corner, shown in Figure 18**. In the V_{sup} = 1.1V case, nominal delay is out of delay range so the feedback system cannot compensate itself.

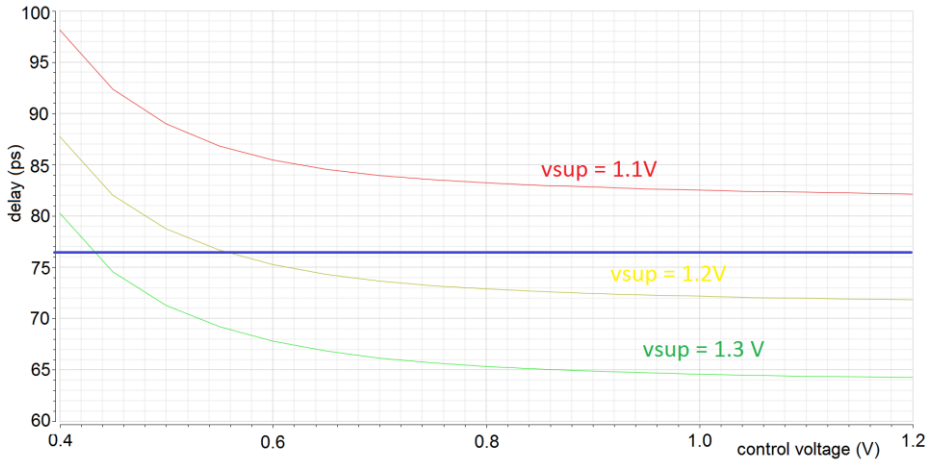


Figure 18 Simulation of delay range DE-2 with voltage supply variations, ss condition.

In short, the additional compensation is only needed for process variations. In delay range simulation, we assume the ff and ss condition as process corners. In order to make sure that the process variations statistically cannot reach even worse condition rather than ff and ss condition, we need to run Monte Carlo simulation to this delay line. The results of 200 point Monte Carlo for process variations only in typical condition (OFF-ON) are given in Figure 19 and 20.

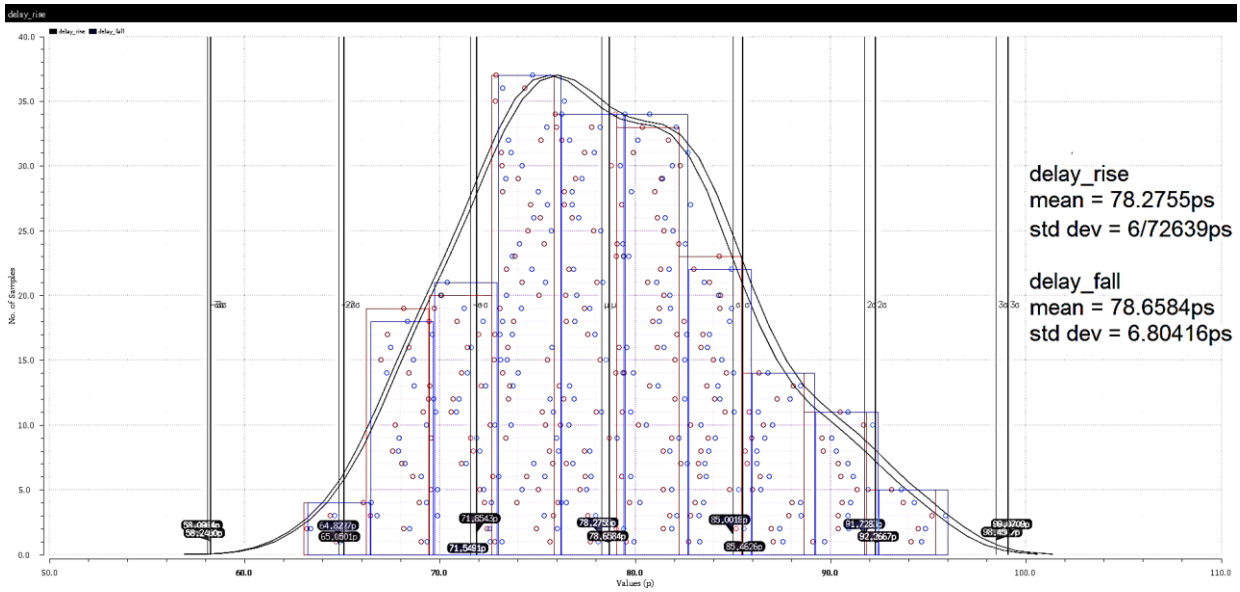


Figure 19 Monte Carlo process simulation for DE-1

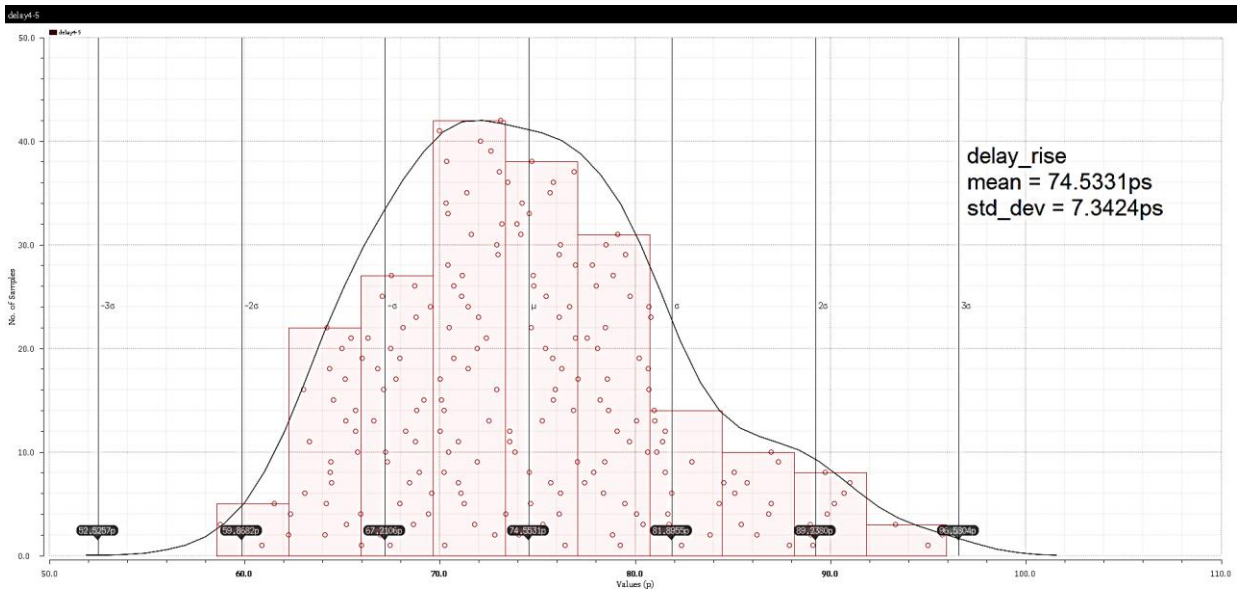


Figure 20 Monte Carlo process simulation for DE-2

From results above, we can compare border of Gaussian distribution with typical operation of ON-OFF configuration during ss and ff condition, shown in Table 2.

Table 2 Process Variations Simulation

Configuration	Nominal delay	Border in Gaussian distribution ($\mu \pm 3\sigma$)
DE-1 ss condition	101 ps (more)	99 ps
DE-1 ff condition	52 ps (less)	58 ps
DE-2 ss condition	108 ps (more)	96.5ps
DE-2 ff condition	49 ps (less)	52.5ps

All of the nominal delay under process corners are out of Gaussian distribution range. Therefore, for both type of delay elements, additional compensation technique previously designed is statistically sufficient to handle process variations up to ss and ff corners. The last simulation to measure delay line performance, we need to do also Monte Carlo for both process and mismatch variations. The results and its summary are given in Figure 21 to 27.

Monte Carlo simulation	points	mean (ps)	stdev (ps)	3*sigma (ps)	delay range typ. (ps)
DE-1 cc mismatch	100	57.5	4.2	12.6	12
DE-1 oc mismatch	100	77.7	6.4	19.2	28
DE-1 oo mismatch	100	109.4	11.4	34.2	65
DE-1 oc process	200	78.3	6.7	20.1	28
DE-2 cc mismatch	100	56.2	4.1	12.3	17
DE-2 oc mismatch	100	70.8*	6.2	18.6	33
DE-2 oo mismatch	200	118.8	17.8	53.4	51
DE-2 oc process	200	74.5*	7.3	21.9	33

*not near with target delay, dominantly because of incorrect bias setting before simulation is started.

Figure 21 Summary of Monte Carlo simulation on delay line

As we can see from the summary of the simulation, the delay range of each delay element on every process corner can sufficiently handle even the deviation up to three times standard deviation from typical value. Although there are some cases like DE-1 cc (cc = ON-ON) and DE-2 oo (oo = OFF-OFF) whose delay range is slightly less than deviation of its Gaussian distribution, it is overestimated to compare it with three-sigma-deviated value, so all circuit configuration are still safe under process and mismatch variations. Based on previous results and simple estimation on area and power consumption, we can compare the performance of delay elements and choose the best one, as shown in Table 3.

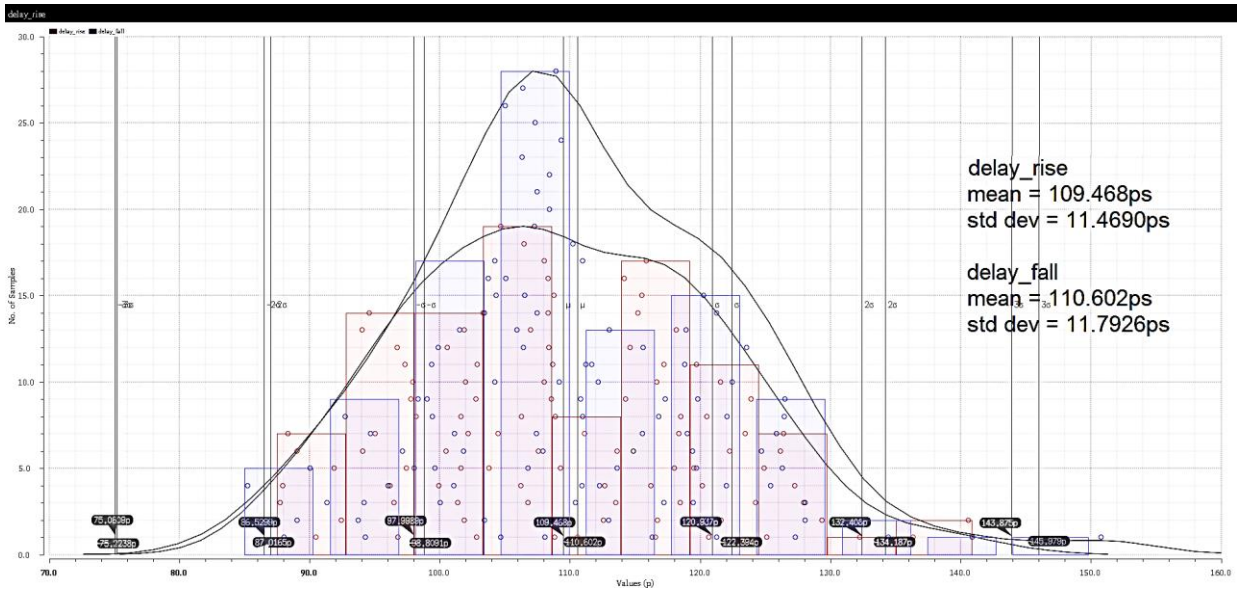


Figure 22 Monte Carlo all variations for DE-1 (OFF-OFF) condition

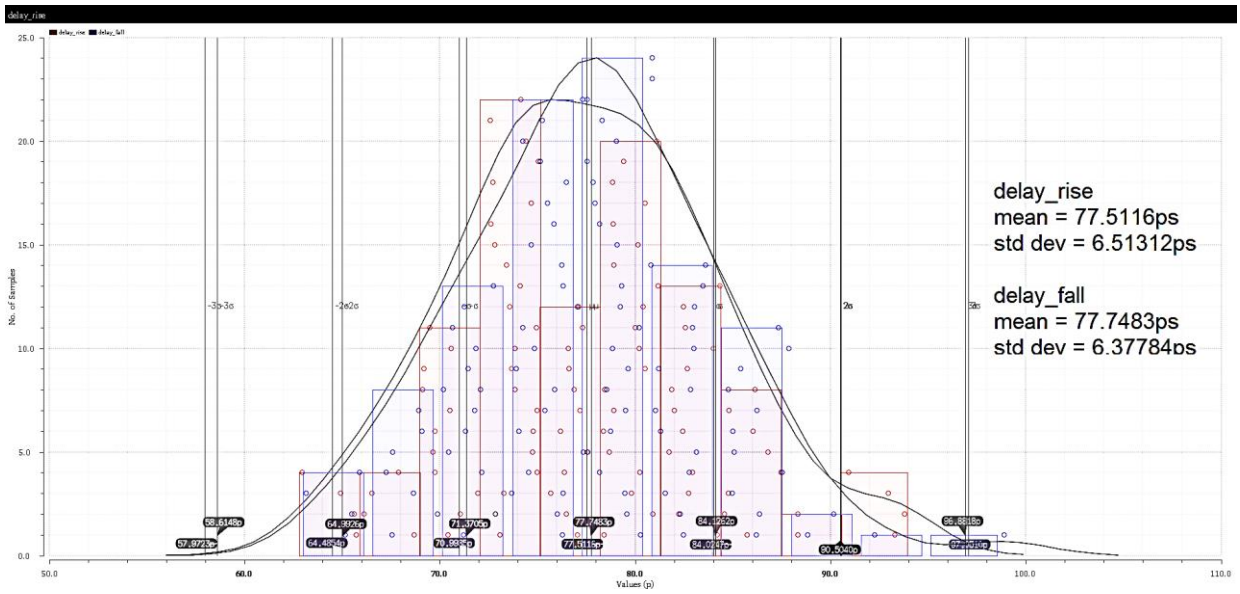


Figure 23 Monte Carlo all variations for DE-1 (ON-OFF) condition

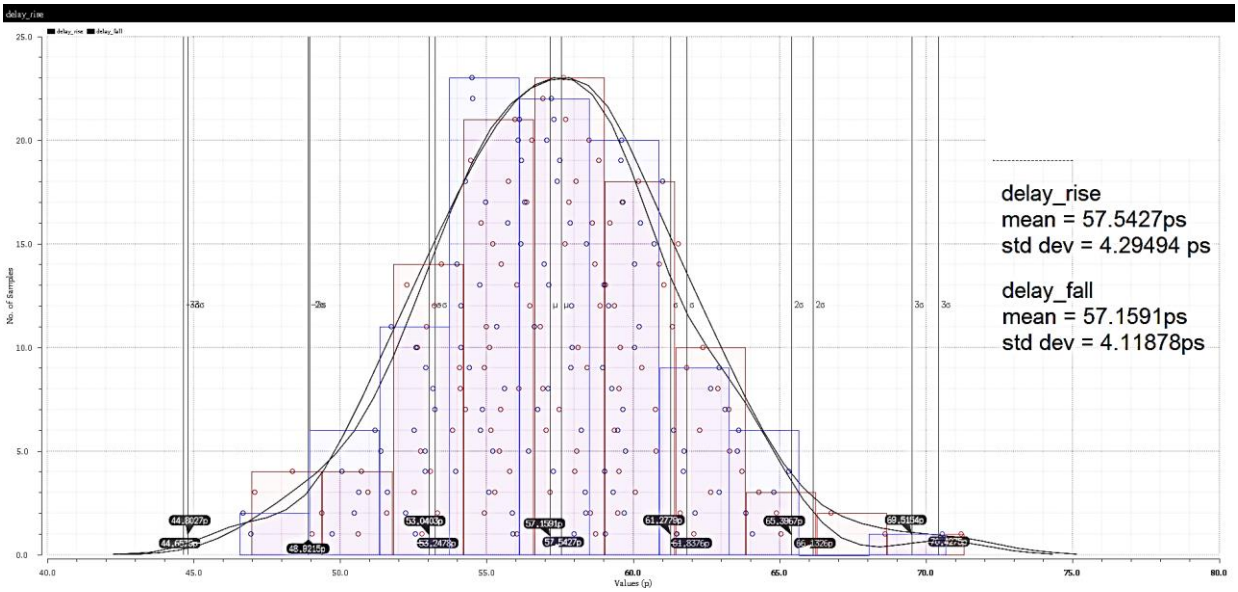


Figure 24 Monte Carlo all variations for DE-1 (ON-ON) condition

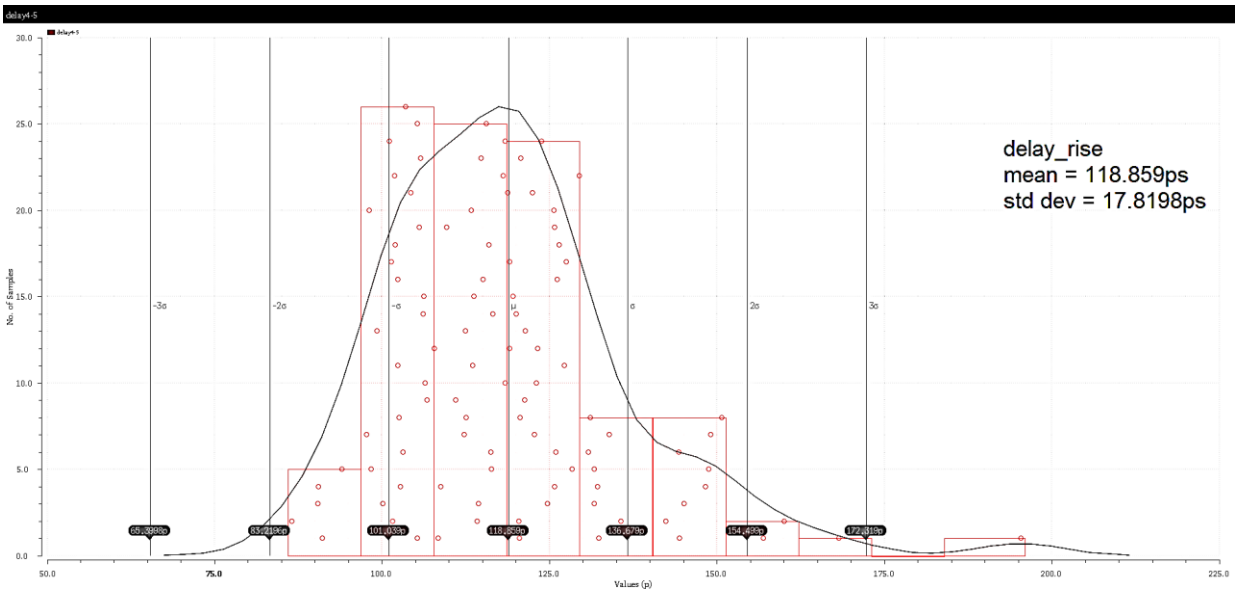


Figure 25 Monte Carlo all variations for DE-2 (OFF-OFF) condition

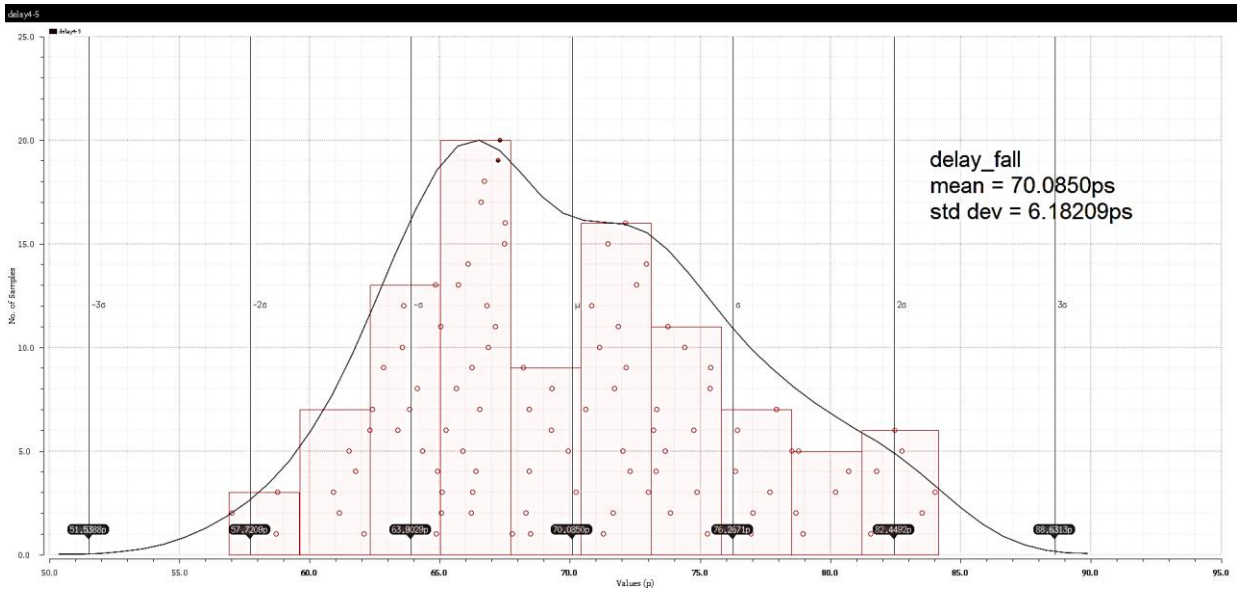


Figure 26 Monte Carlo all variations for DE-2 (ON-OFF) condition

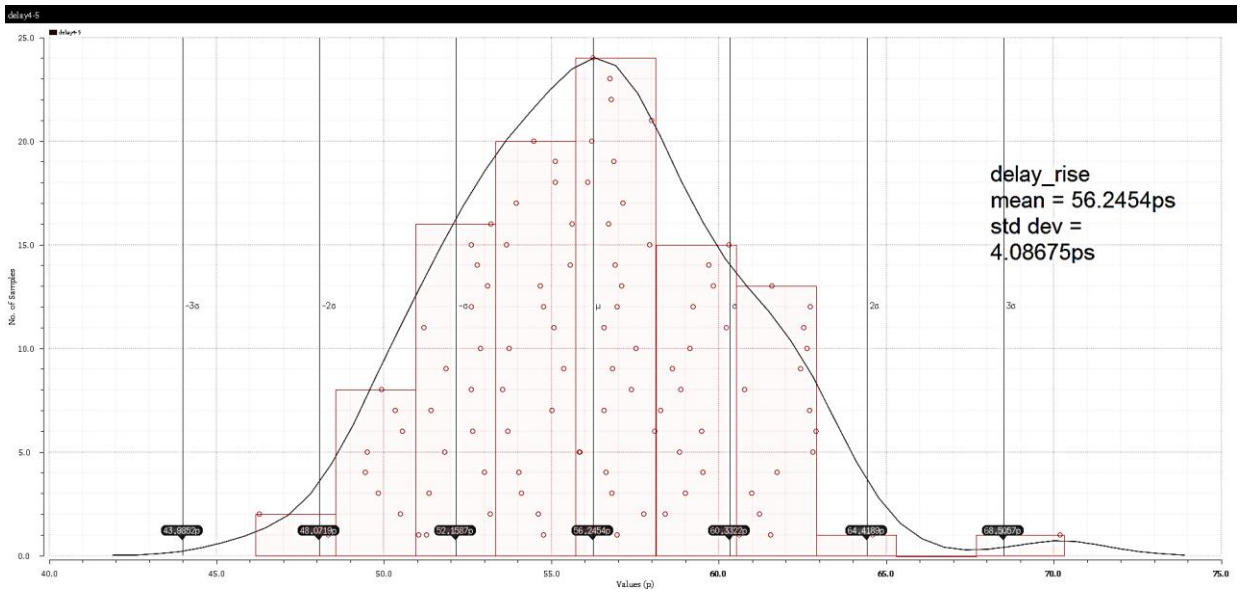


Figure 27 Monte Carlo all variations for DE-2 (ON-ON) condition

Table 3 Comparison Between DE-1 and DE-2

Parameter	*DE-1*	*DE-2*
Delay range (ff, tt, ss)	65ps, 28ps ,12ps	51ps, 33ps, 17ps
Response to voltage and temperature variations (after $\Delta T = 24^oC$; after $\Delta V_{sup} = 0.1V$)	Delay offset 2ps; delay offset ≈ 8ps	Delay range diverges 2ps around target delay; delay offset ≈ 8ps
Response to process and mismatch variations (stdev during cc, oc, oo configuration)	4.1ps, 6.4ps, 11.4ps	4.1ps, 6.2ps, 17.8ps
Area (estimated = bias width +DE width)	11 + 12.04*64 = 781.56um	9.2 + 6.6*64 = 431.6um
Power (estimated = static current in bias circuit, ff)	240uA	40uA

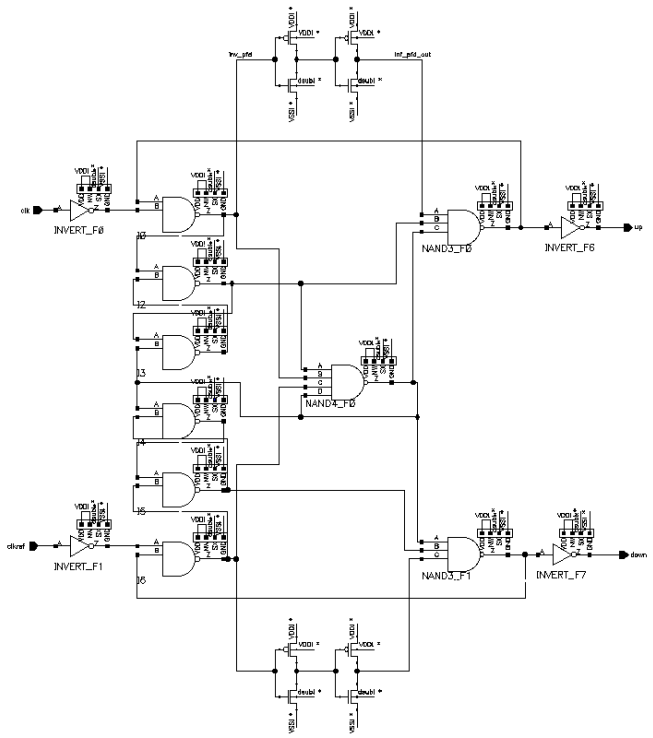
The area is estimated by calculating total width of the transistors in each configuration of delay line. The static power consumption is estimated by calculating total dc current consumed, which the simulation is explained in detail in Overall System section. The performance of delay range and response to process, temperature, voltage and mismatch variations for both configuration seems to be more or less the same, but DE-2 configuration can achieve it with less area and static current consumption. We are now more convinced that DE-2 is better than DE-1.

3.1.2. Phase Detector and Charge Pump

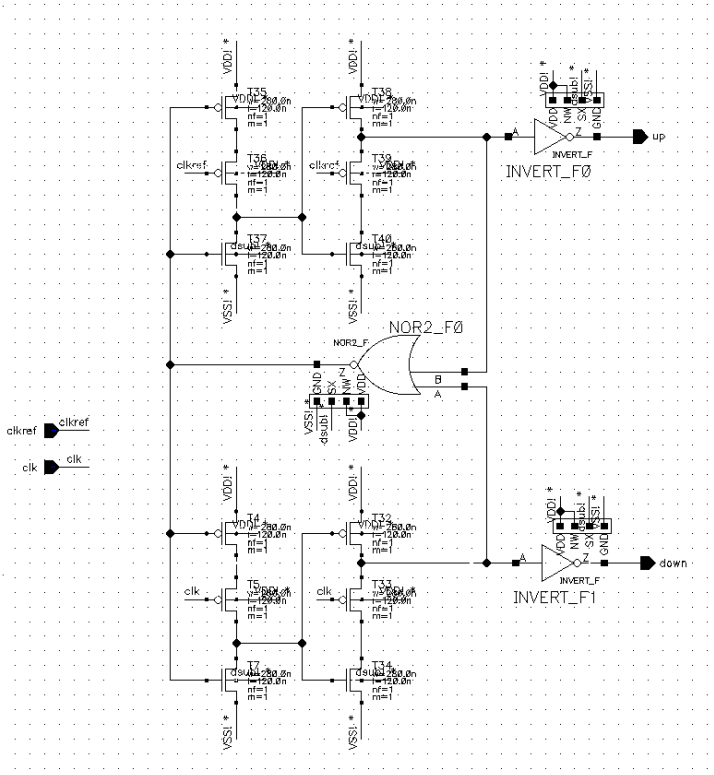
The circuit schematics of PFD and CP are given in Figure 28 and 29.

In addition, we need additional module to make sure that the output of charge pump -control voltage of delay line- is set at VDD during system startup. This is important because if control voltage is at ground during startup, it corresponds to no output signal in delay line. Consequently, in phase detector, there is no input signal to be compared with reference, so the feedback link is broken and lock condition cannot be achieved. The circuit schematics of startup module is given in Figure 30. It is important for CLK and CLKREF signal to have the same loads on each path. In order to achieve that, in CLKREF path the dummy inverter is added to equalize loads given by input flipflop in CLK path. In this case, start signal that sets $1/T_{bunch} = 330ns$ after startup, must be given to this component.

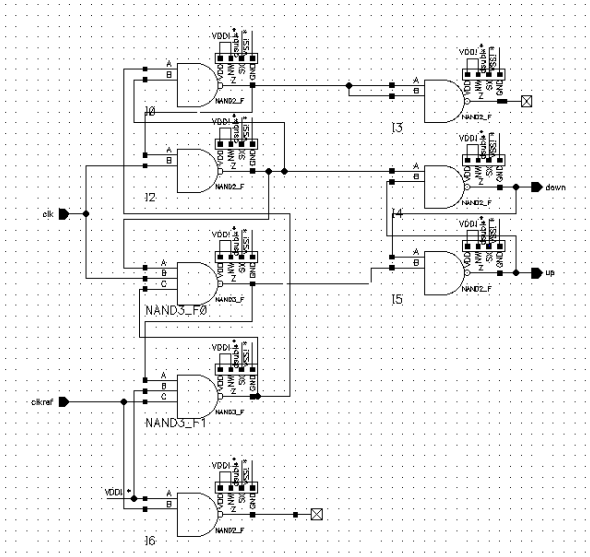
We need PFD that has negligible amount of jitter in lock condition, reasonable deadzone, and sufficient width of the output pulses to be given to charge pump. Those parameter can be observed by running PFD in several possibility of delay difference, driven by one signal with 204 MHz system clock frequency, and another signal with period slightly deviated from clock period (10ps, 100ps, and 1ns). The simulation results are given in Figure 31 to 33.



a) Static PFD



b) Dynamic PFD



c) Bangbang PFD

Figure 28 Schematics of several types of PFD

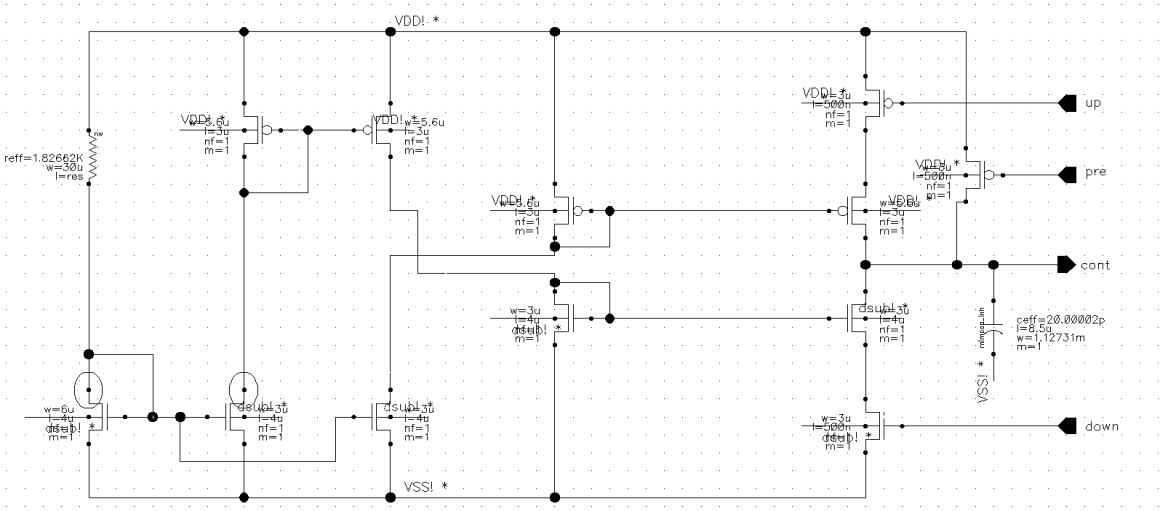


Figure 29 Schematics of charge pump with current mirror

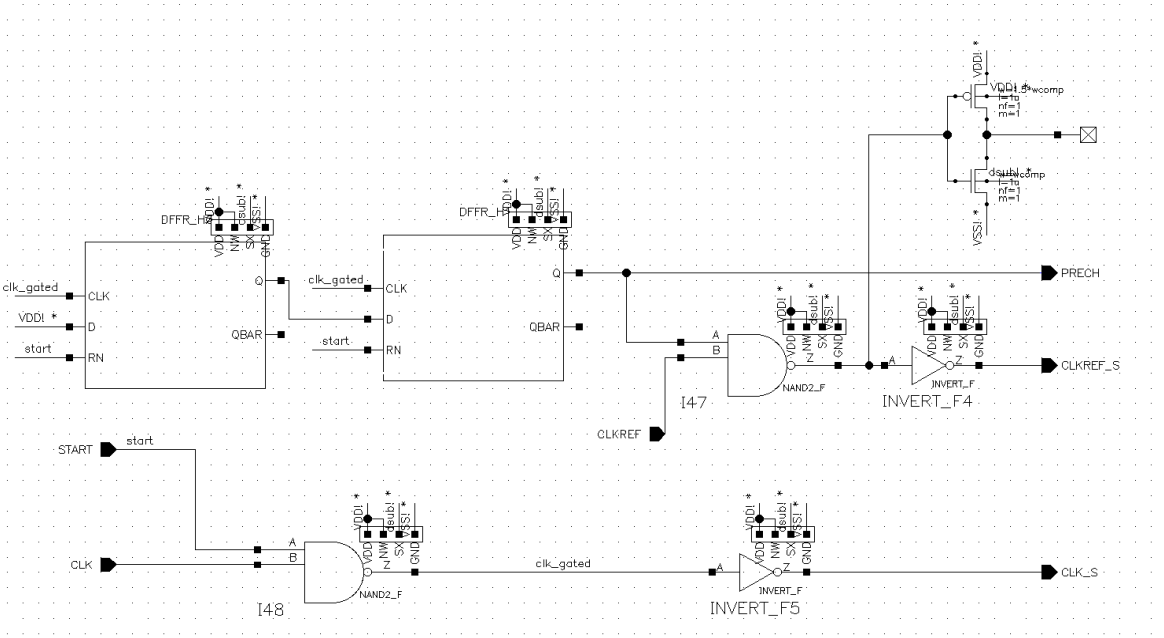


Figure 30 Schematics of startup circuit

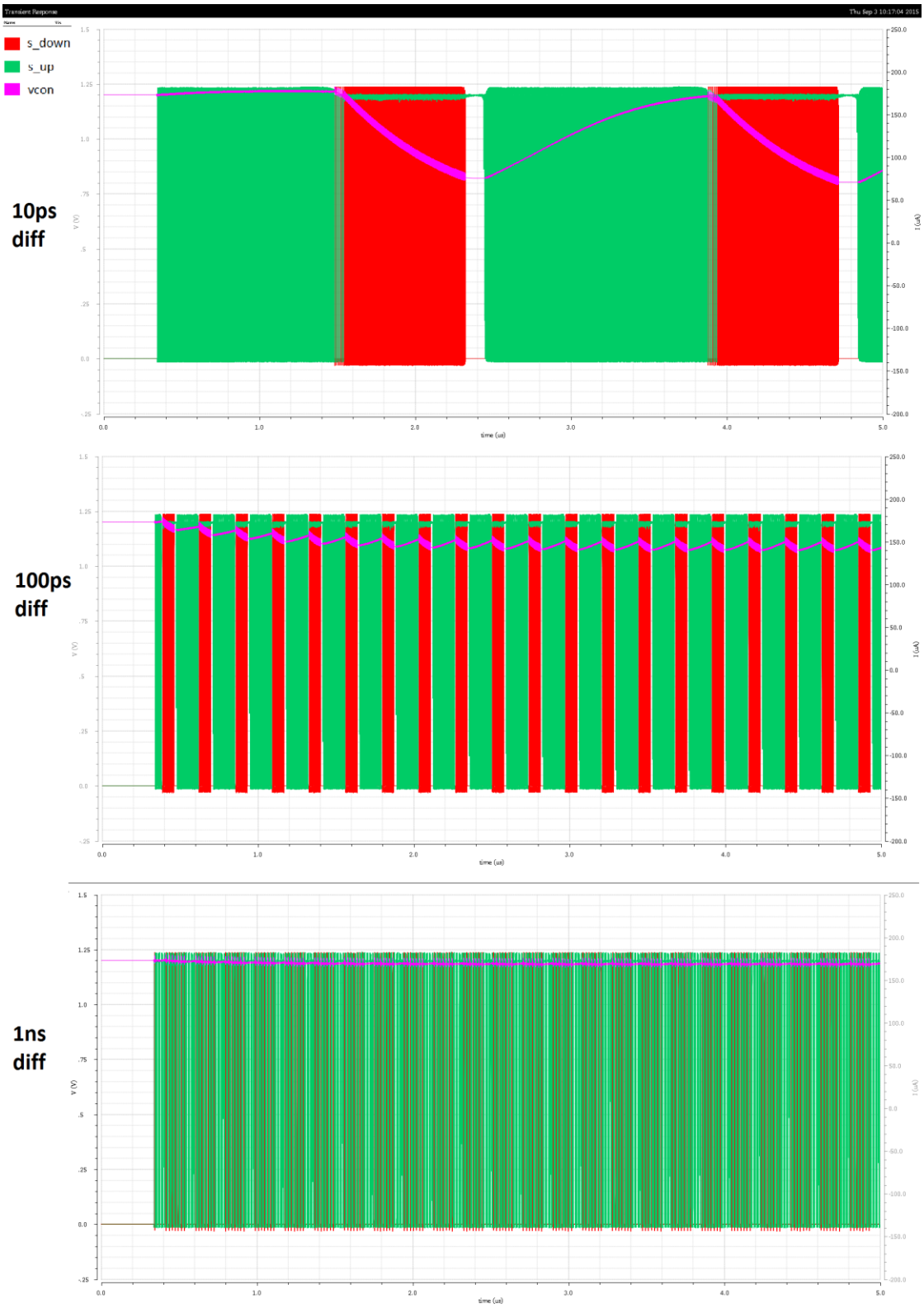


Figure 31 Simulation of static PFD with various period differences

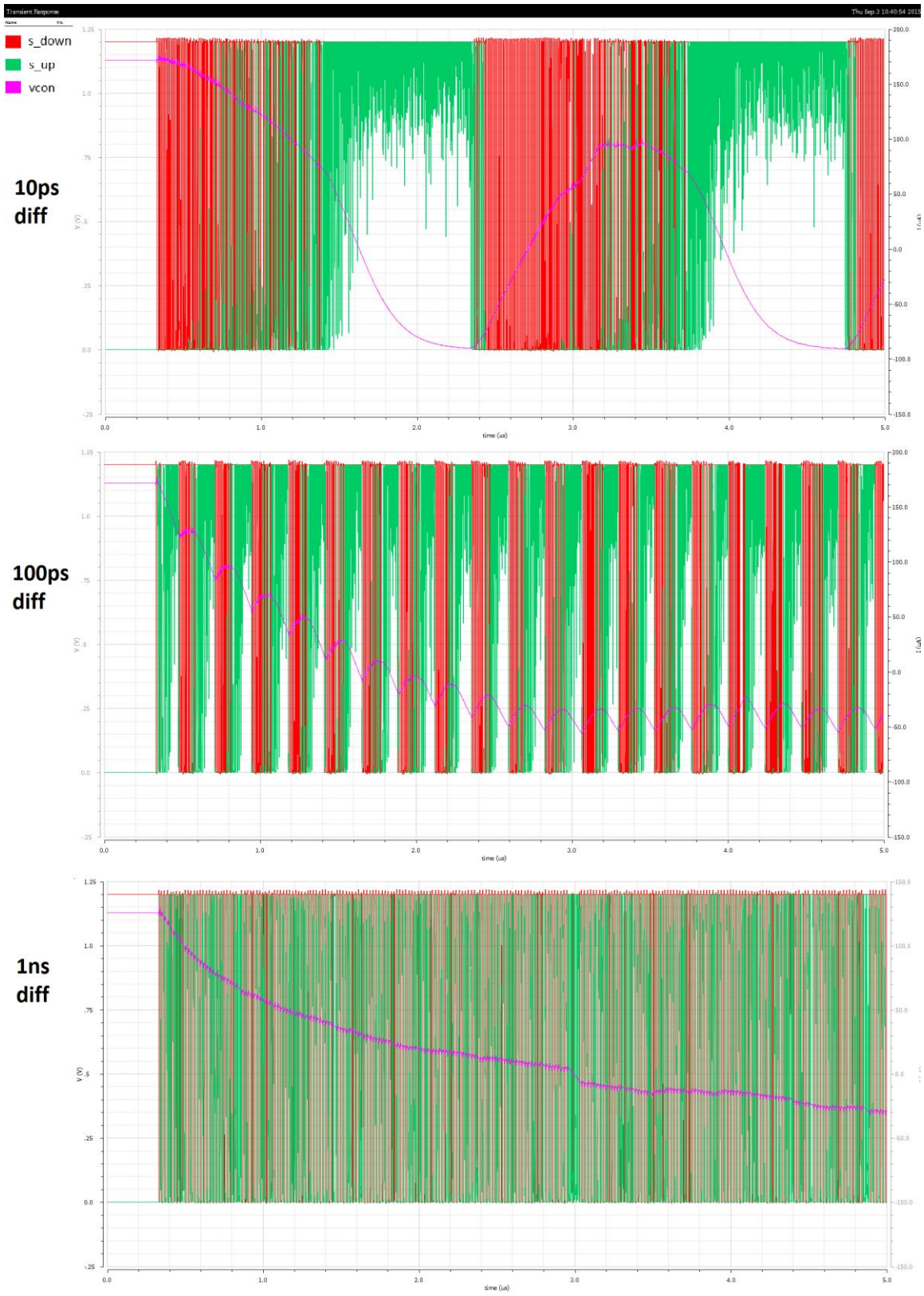


Figure 32 Simulation of dynamic PFD with various period differences

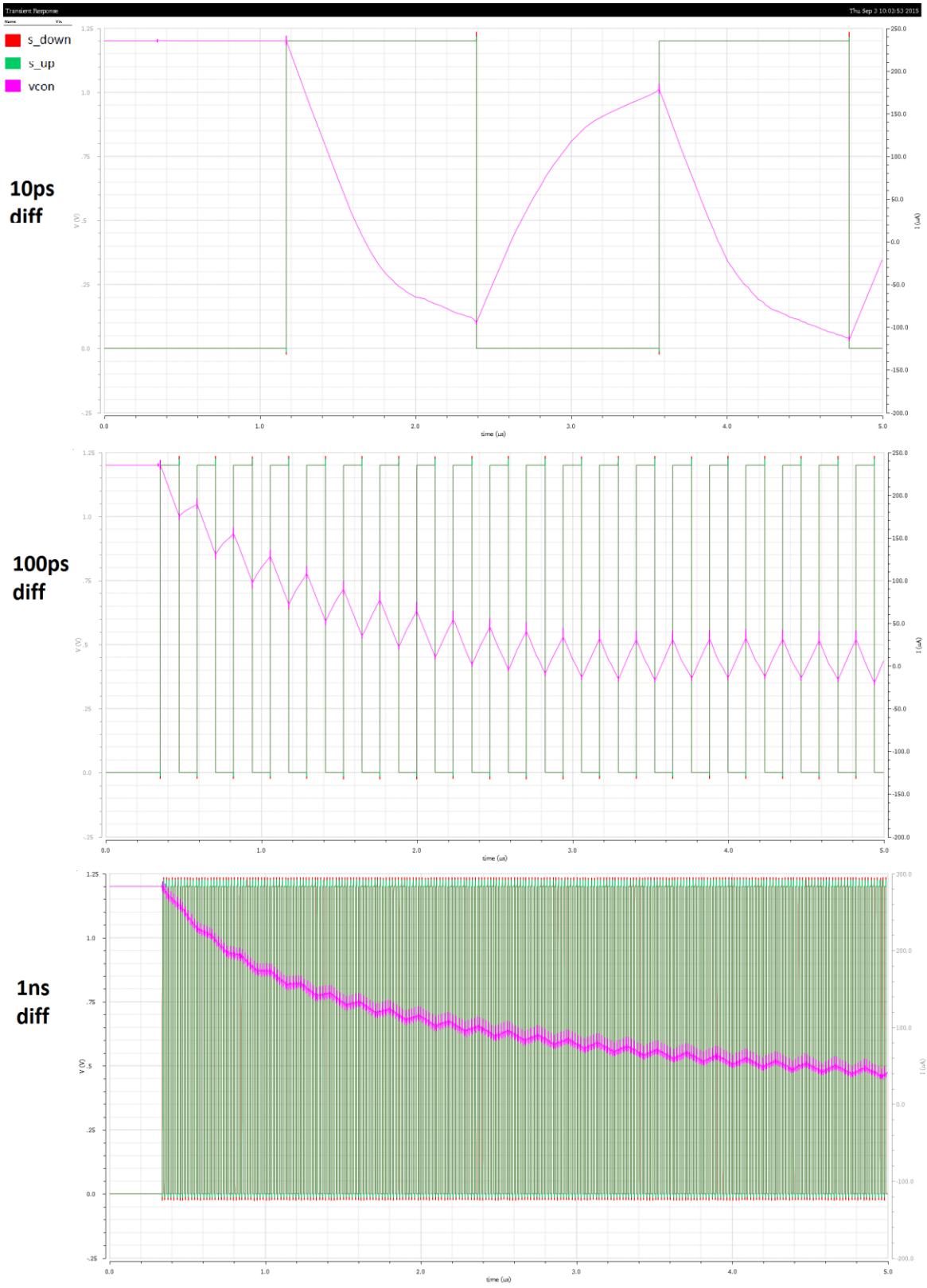


Figure 33 Simulation of bangbang PFD with various period differences

First, static PFD performs detection very well, with almost equal width of up (red) and down (green) signal, seen from the constant average of vcon (orange) value. Although the width of the pulse is smaller compared to other PFDs, causing the slow change of vcon, but it can be compensated by using higher I/C ratio in charge pump. On the other hand, bangbang PFD has wider up and down pulses, due to the two-state detection properties. But, it has sawtooth-like vcon signal during lock condition, which creates very huge jitter when employed in DLL, so it is not preferred for this application. Dynamic PFD has three state detection properties and wider pulse than static PFD, but it has very nonlinear characteristics and many jitters. In short, static PFD is most suitable for this application.

The next step is, to determine the I/C ratio of the charge pump. Desirable behavior that we need are reasonable fluctuation in lock condition and less response time (or high slope) from maximum phase difference between output delay line and reference. Firstly, we set the reasonable current reference in charge pump to be around 100uA. Then, we vary the capacitance to change the I/C ratio. The simulation results are given in Figure 34 and 35.

It is seen that, when we increase charge pump capacitance, the alternating response during lock condition is significantly reduced, with tradeoff of decreasing response slope. Response slope is directly related with lock time. Increasing more capacitance will not make any difference in jitter performance but worsen the response time of the system. Since there is no specific requirement about lock time, therefore, **dedicated 20pF MIM capacitor is enough for charge pump** to avoid significant jitter.

3.1.3. Other Components

Counter, thermometric-to-binary encoder, parallel-to-serial encoder, and other components design and simulation are not included in this Summerstudent project so far.

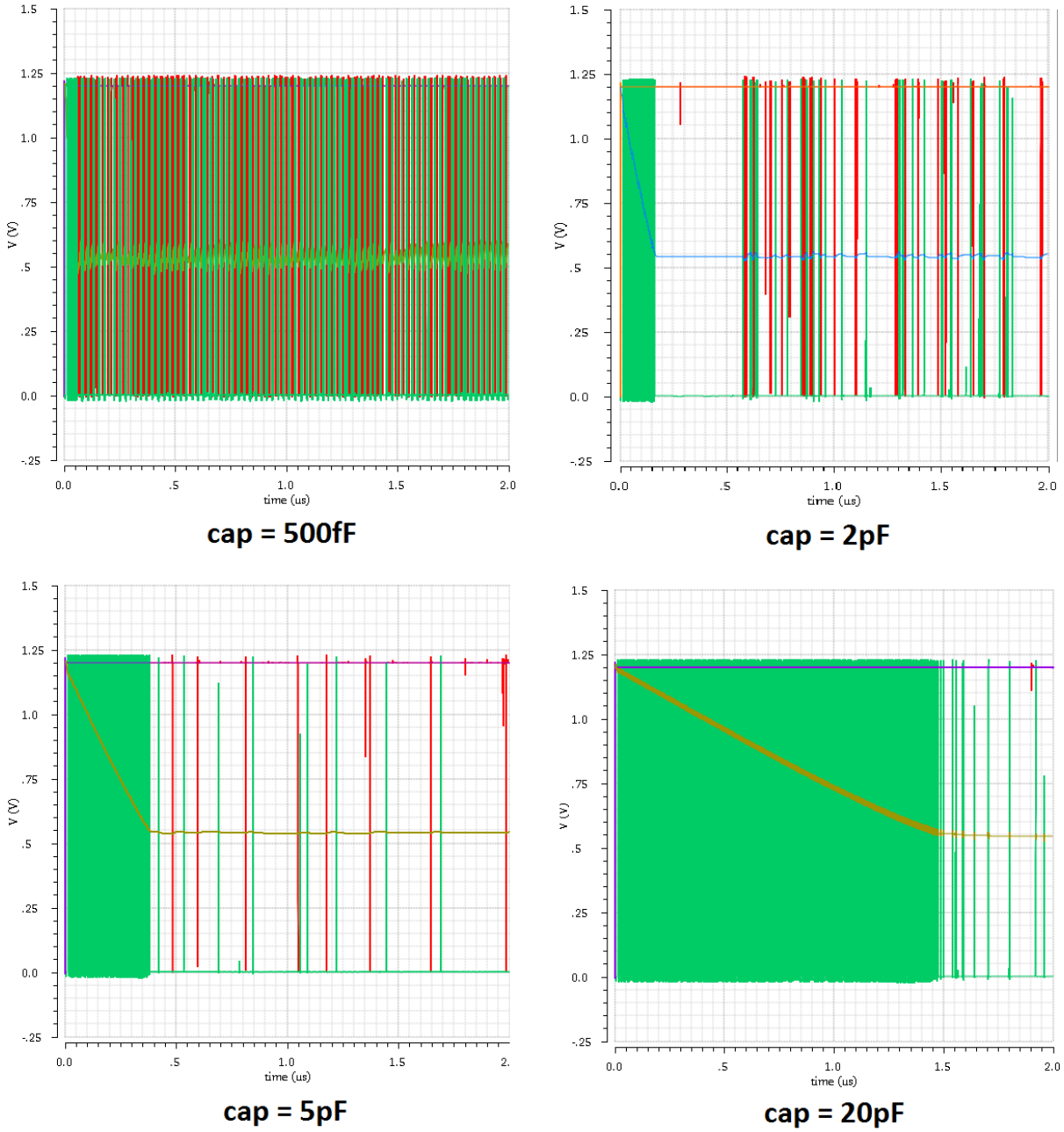


Figure 34 Control behavior with various CP capacitance

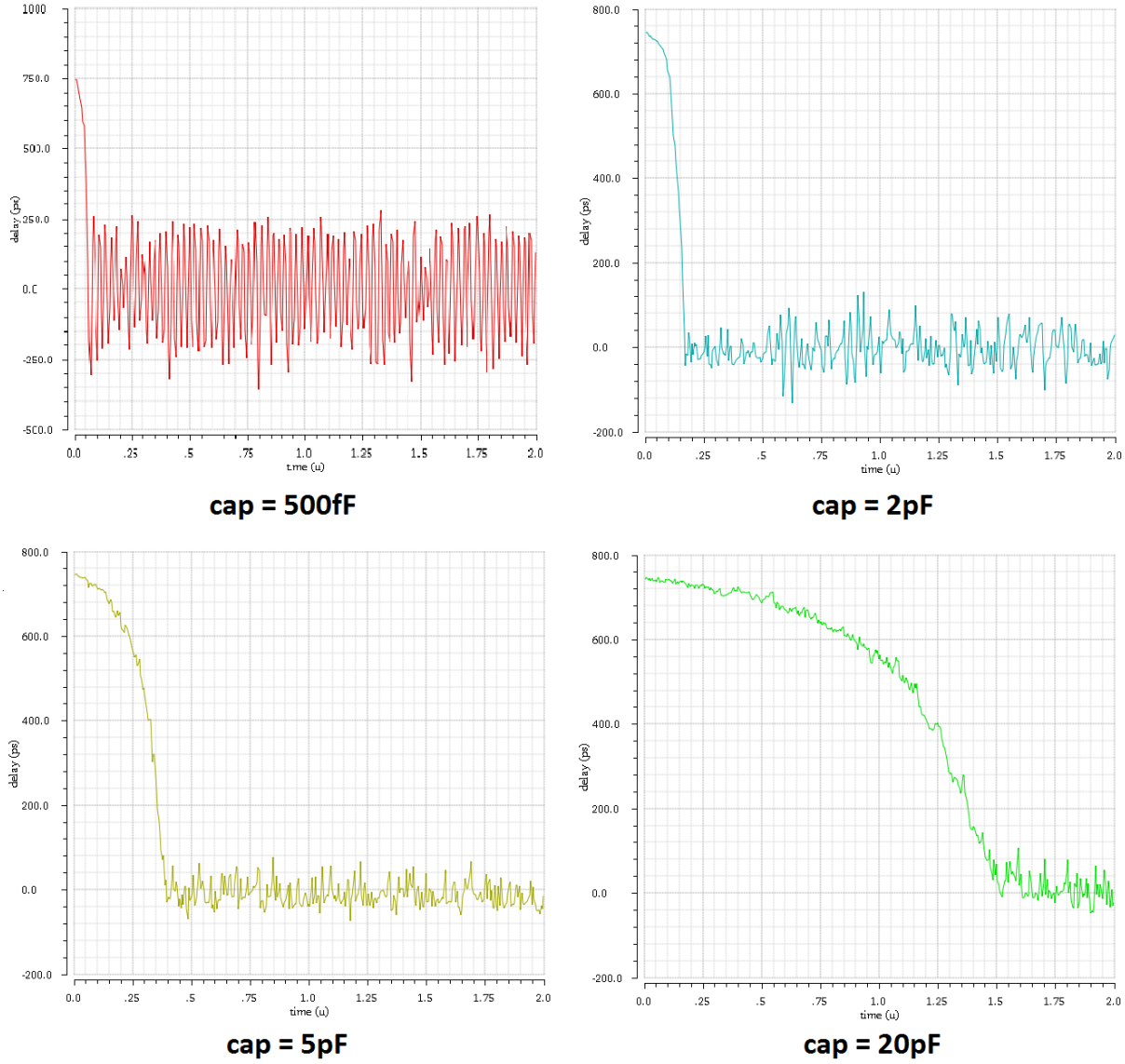


Figure 35 Delay behavior with various CP capacitance

3.2. Overall System

After choosing proper design for each essential elements in DLL, now we continue to check whether delay lock condition can be achieved in any process corners. Delay line is connected with latch on each of delay elements to model capacitance from sampling modules and thermometric-to-binary encoder. Since we will have closed-loop system, we need to swap the connection between phase detector and charge pump, activating negative feedback. Since the output of delay line is now already loaded with flipflop in startup module, then we can remove dummy element on it to reduce propagation delay. The DLL configuration is shown in Figure 36.

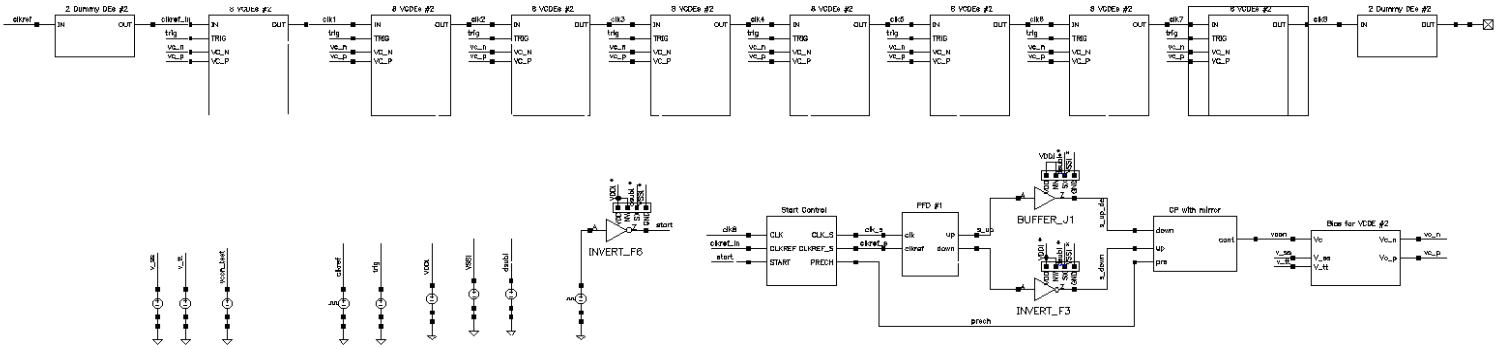


Figure 36 Schematics of overall DLL of DE-2

The simulation results, presented with delay difference between output signal and reference and control voltage behavior as a function of running time, are shown in Figure 37 through 43.

Figure 37 Rising edges on several tapping points, DE-2 type, tt condition

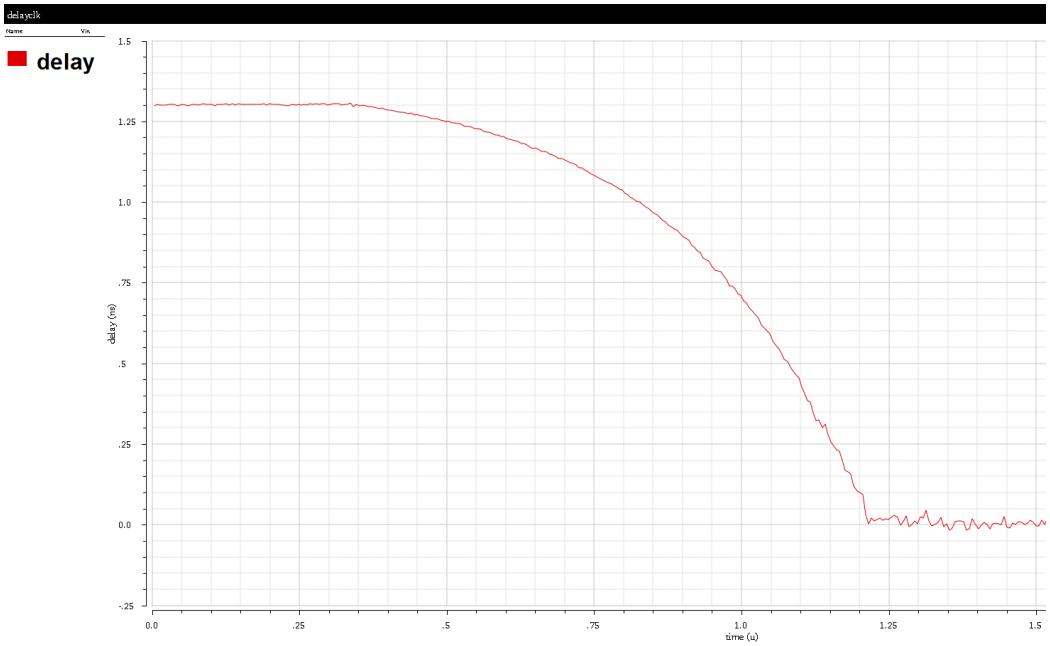


Figure 38 Delay difference during locking mechanism, DE-2 type, tt condition

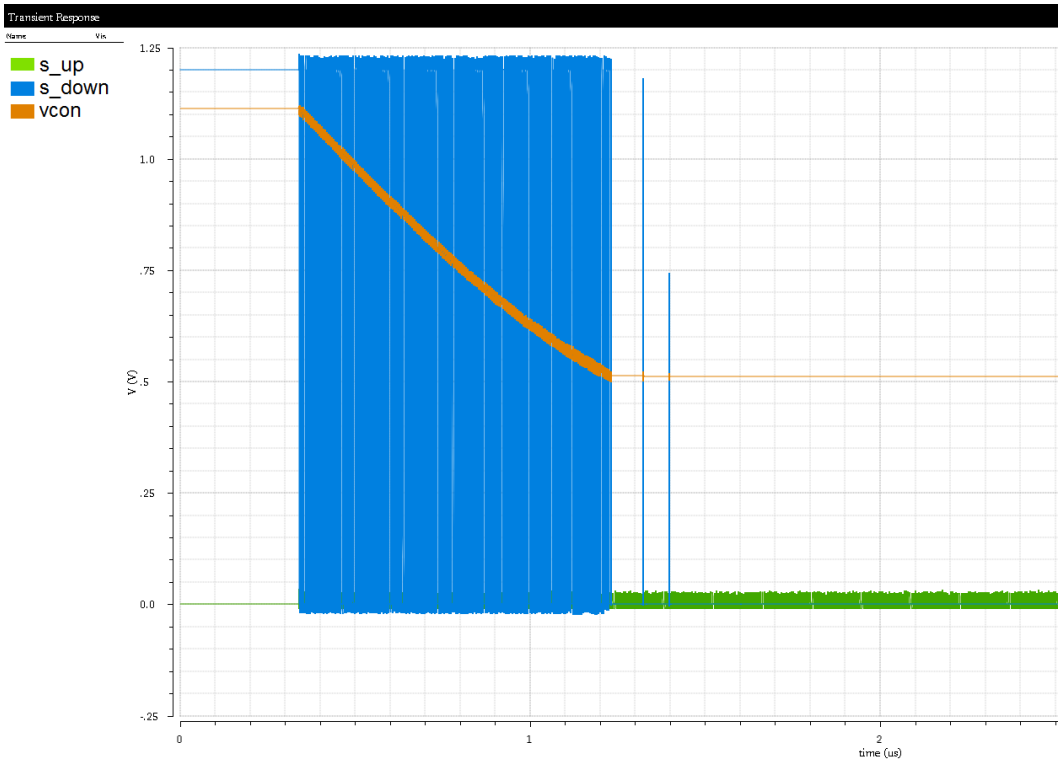


Figure 39 Control behavior during locking mechanism, DE-2 type, tt condition

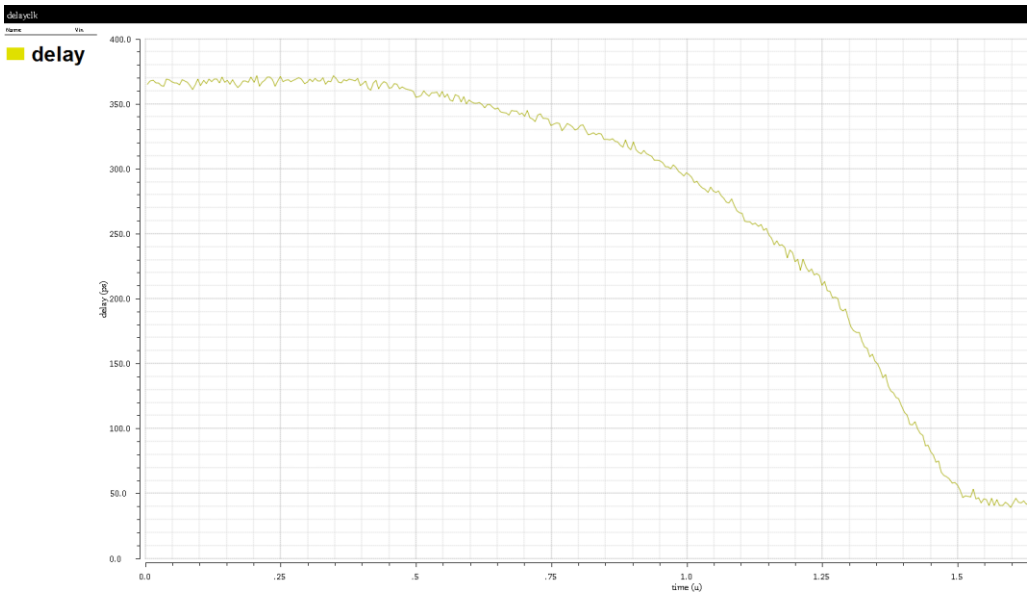


Figure 40 Delay difference during locking mechanism, DE-2 type, ss condition

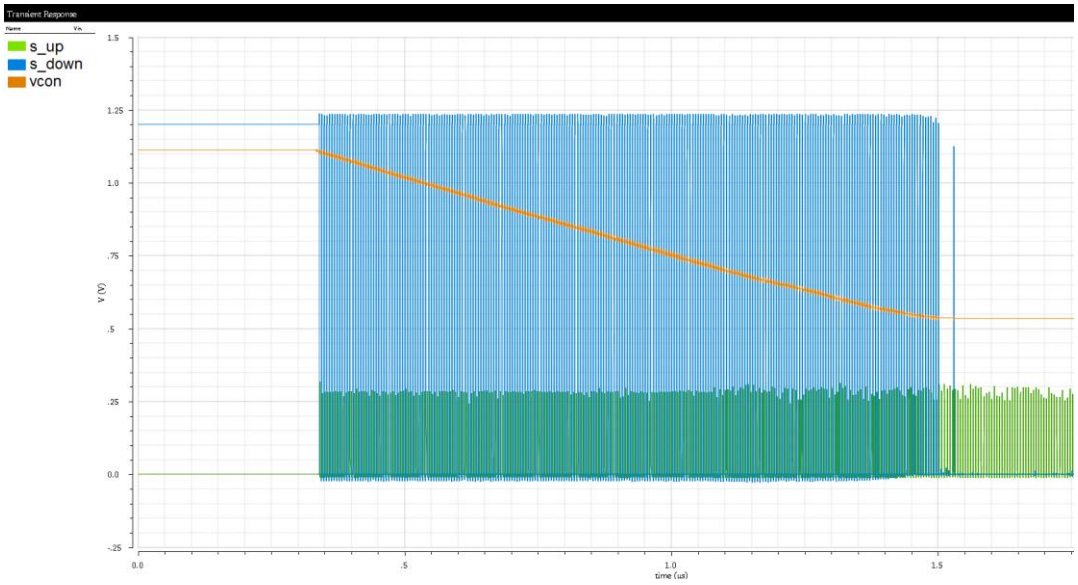


Figure 41 Control behavior during locking mechanism, DE-2 type, ss condition

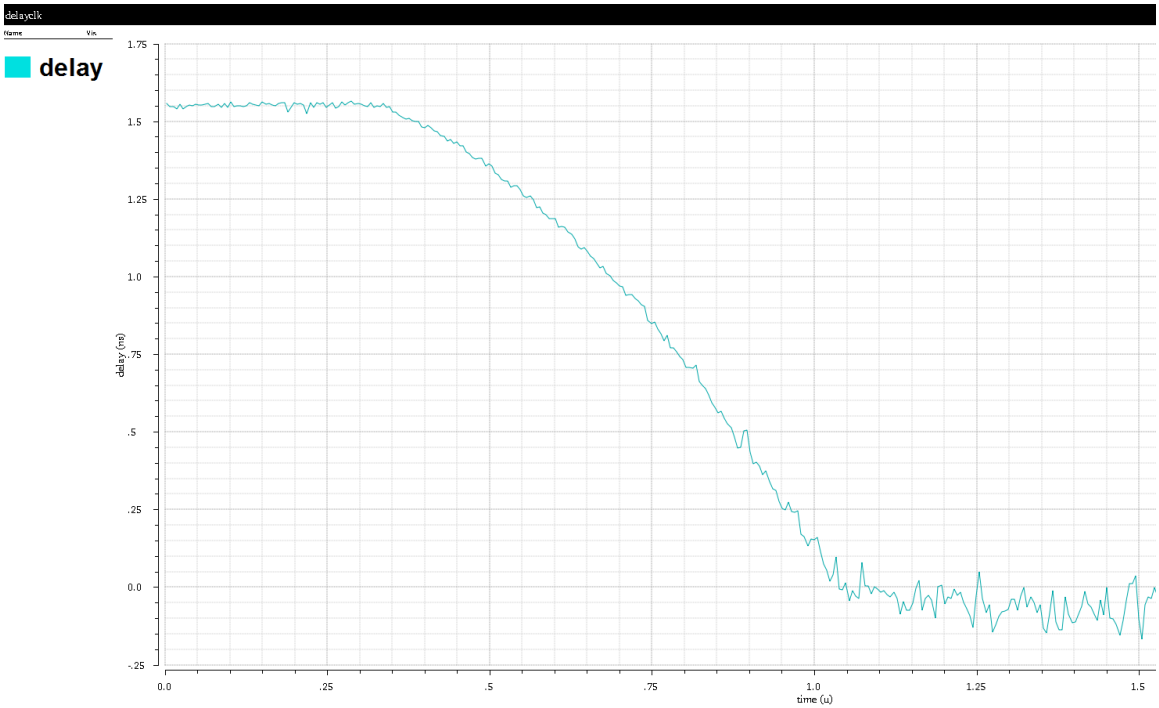


Figure 42 Delay difference during locking mechanism, DE-2 type, ff condition

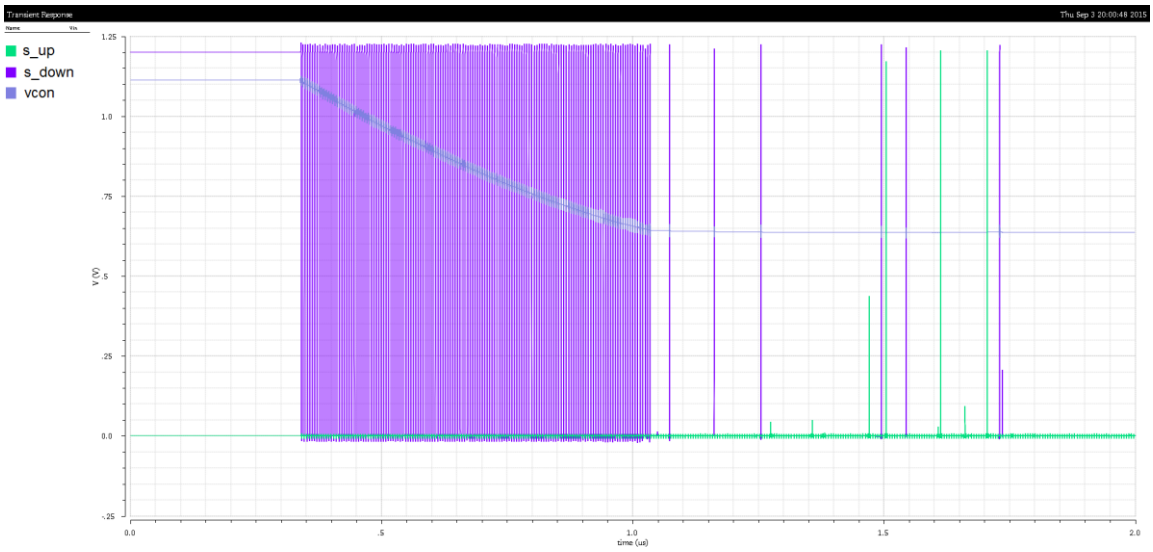


Figure 43 Control behavior during locking mechanism, DE-2 type, ff condition

There are three patterns that we can see from above results. First, on each of the delay difference-time curve, it starts with initial maximum delay difference, where in faster process corner, it has higher value. Second, lock time is shorter in faster process corner. Third, there is considerable amount of unwanted up and down signals during locking under ff condition. Those are all valid, because in fast process corner, we have more delay range and higher delay-to-voltage slope. Higher slope means small difference in control voltage create significant change in propagation delay, hence, more sensitive to variations. However, in some condition, the system does not lock

at near 0 ps delay difference, in other words, we have static phase error. Summary of above simulation can be seen in Table 4.

Table 4 Delay Locking Simulation Results

Process condition	Initial (max) delay difference (ps)	Lock time (including precharge) (ps)	Average delay error during lock (ps)	Average and max jitter during lock (ps)
ff condition	1600	1000	**-60**	53; 80
tt condition	1260	1200	0	25; 50
ss condition	370	1500	**40**	10.7; 20

Static delay error in tt and ss condition is quite significant, which corresponds to almost one LSB. This happens because the unbalanced load between paths travelled by each of the PFD inputs, especially inside startup circuit. Moreover, the unbalanced load is always changed under different process variations.

We can also estimate current (or power) consumption by calculating static current consumed by each of the components, mainly charge pump and bias circuit of delay line. By also comparing DLL with DE 1 and DE 2, the simulation results are shown in Figure 44 through 47.

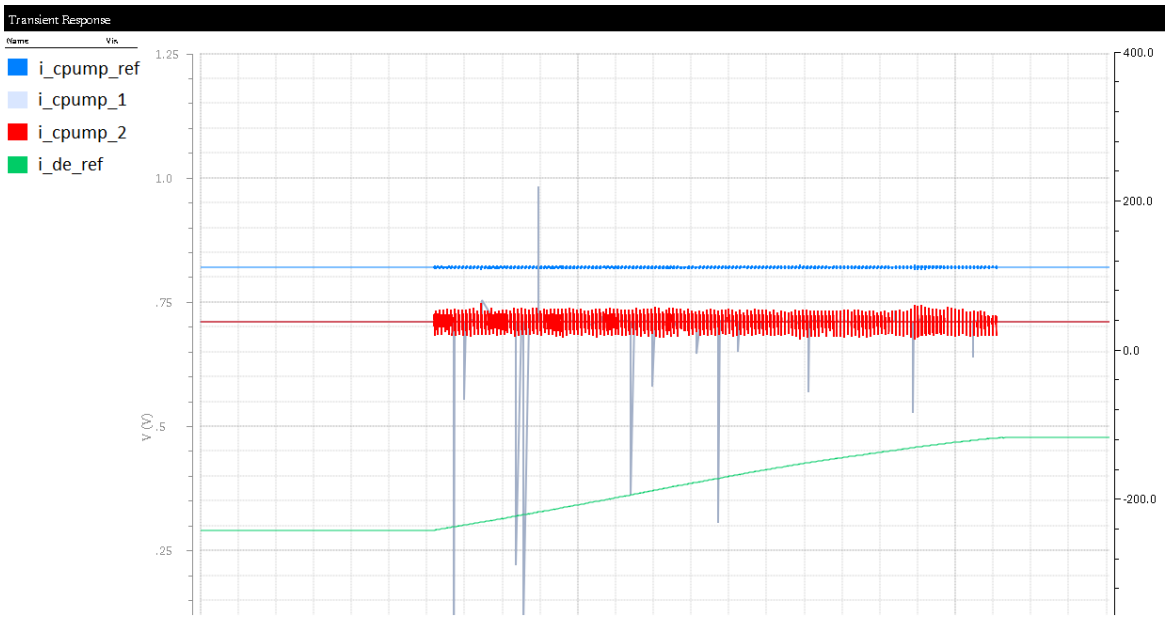


Figure 44 Current consumption during locking mechanism, DE-1 type, ff condition

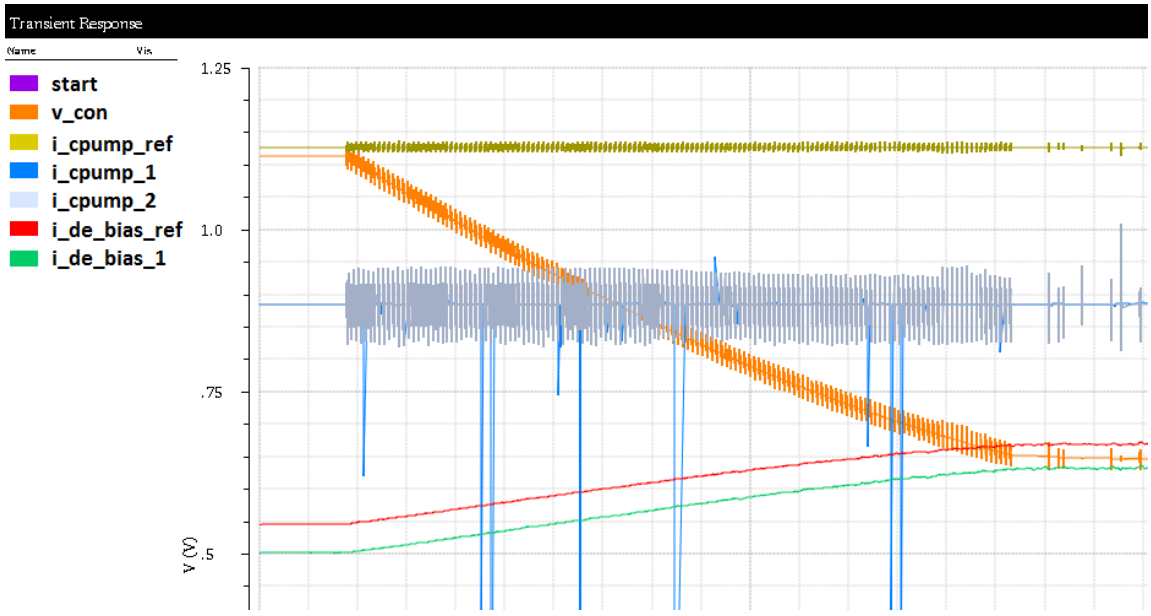


Figure 45 Current consumption during locking mechanism, DE-2 type, ff condition

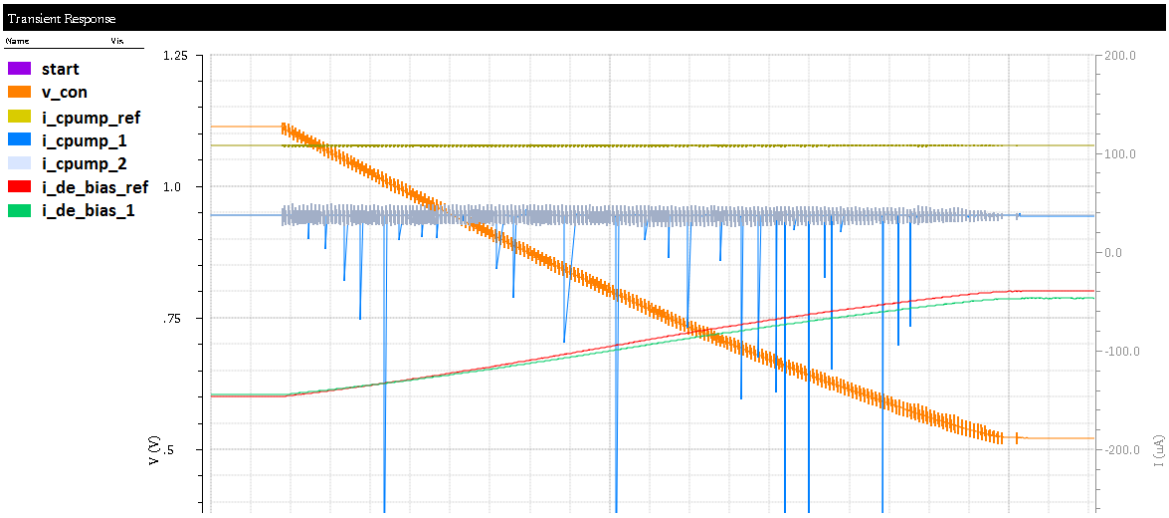


Figure 46 Current consumption during locking mechanism, DE-2 type, tt condition

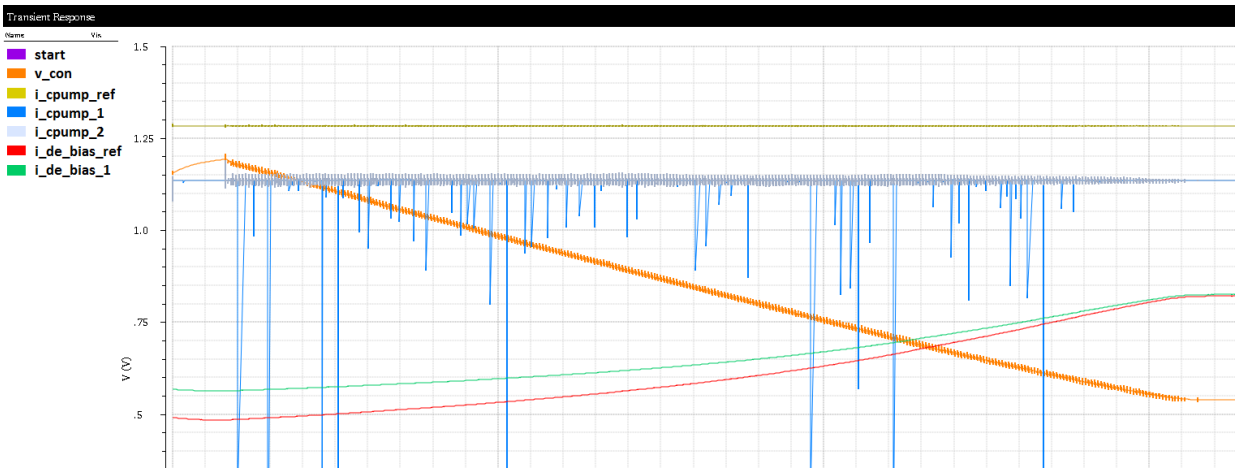


Figure 47 Current consumption during locking mechanism, DE-2 type, ss condition

For charge pump, since the current is more or less fixed due to current mirror structure, the current consumption is unchanged on every condition, which is around 110+40+40 = 190uA. Under ff process corner (without any additional current injection), DE-1 needs 120+120 = 240uA to power bias circuit of delay line, whereas DE-2 needs only 20+20 = 40uA. To conclude, delay line has As expected, the current is higher under worse process condition (tt = 160uA, ss = 180uA), since it needs more power to achieve the same target delay, compensated by current injection in bias circuit.

4. Conclusion

The time-to-digital converter design for readout ASIC of SiPM imaging system has been almost completed. However, there are several alternatives to improve performance of overall TDC, such as :

- Adding **digitally controlled dummy load** inside startup circuit. The digital control is also associated with process control register, so that average delay offset during lock can be reduced in ss and ff condition.
- Sizing control transistors (wcntr, wcntr2, wcntr3) in DE-2 in order to **have nominal voltage higher** than previously designed. Nominal voltage around 0.6-0.7 V is a good choice since the target delay is still approximately located in the middle of delay range. Since the delay-voltage relationship is nonlinear, using higher nominal voltage will make jitter smaller during lock condition. Examples of new sizing :

wcntr	wcntr2	wcntr3
160n	160n	900n

- Sizing transistors in delay element to have **less delay range**, therefore, less jitter during lock condition. But, having less delay range increase the risk of unable to lock due to PVT variations effect.
- Using **another TDC sub-gate delay architecture** that allows to have less stringent delay element requirement, for example, array of TDCs can allow delay element to have propagation delay more than 100ps to achieve TDC resolution below 100ps.

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