



PERCIVAL. The calibration of the chip and periphery board

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1. Introduction

Over the last decade, synchrotron radiation sources have seen a significant increase in brilliance, and the advent of free electron lasers has made entire new research fields accessible to investigations with X-rays. These advances in light source capabilities have resulted not only in a host of scientific advances and discoveries, but also in a need for a new generation of X-ray imaging detectors that can match the sources' capabilities in terms of frame rate and image dynamic range while recording image information with the fine granularity over a large – preferably uninterrupted – (multi)megapixel area with single-photon sensitivity. Developing such next-generation imagers is both costly and time-consuming, and the requirements at many photon science facilities are similar enough to invite a collaborative effort. The PERCIVAL (“Pixellated Energy Resolving CMOS Imager, Versatile and Large”) imager is being developed by a collaboration of DESY, Rutherford Appleton Laboratory (RAL), Elettra, Diamond Light Source (DLS) and Pohang Accelerator Laboratory (PAL) to answer this need for the soft X-ray regime.

2. Theory

2.1. The PERCIVAL sensor

CMOS sensors offer several advantages over other detection approaches for the described needs. They can generally be faster than CCDs as their architectures lend themselves to massive parallelization, enabling high speed at low noise; moreover, in-pixel intelligence can be integrated. Compared to hybrid pixel detectors, smaller photodiode capacitances can be realized in a monolithic CMOS imager, again enabling lower noise. In addition, small pitches of few tens of nm are less problematic in CMOS imagers since there is no need to push the boundaries of bump bonding technology, and the monolithic design also reduces complexity. Conversely, while at higher photon energies above few keV CMOS sensors are at a disadvantage due to the relatively thin commercially available epilayers (10s of nm), this active detection layer is thick enough for photons in the soft X-ray regime of PERCIVAL. Several key needs for the PERCIVAL sensor were already discussed above (see section 1): single-photon sensitivity with low probability of false positives in combination with large dynamic range and uniformly high quantum efficiency in the 250eV to 1keV regime, operation up to 120Hz, pixel size in the 10 – 100nm range, and Megapixel or larger sensor. The need for a low probability of false positives even at 250-300eV converts to a need for a noise level (best significantly) below $15e^-$ rms. To minimize noise, even at the relatively short integration times needed the operating temperature must be kept at around -30C – -40C. The dynamic range needed (reliable single photon detection to 10^5 photons) would imply a brute-force digitization dynamic range of better than 10^6 or 20 bit; instead multiple gains (4 gain levels) are implemented. In addition to these key needs, a cloverleaf arrangement with central hole must be possible to arrange sensors around the path of the undiffracted beam or cover a larger area. In order to allow this, the sensors should be buttable at two adjacent edges. Given the emphatic desire in the community for large sensor areas without butting edges, a single PERCIVAL sensor will have an active imaging area of $10 \times 10 \text{ cm}^2$, comprising 3520×3710 pixels of 27.0nm pitch. This is slightly larger than the 25nm pitch of the current test sensor, the change was made to optimize “full well capacity” per unit area of the full sensor. One key challenge is the desire to achieve high quantum efficiency in the soft X-ray regime down to 250eV. At this energy, attenuation lengths in both Si and SiO₂ are on the order of 0.1nm, and thus passive entrance windows of few, certainly no more than tens of, nm are required to enable quantum efficiencies above 90%. This makes back-thinning and back-illumination indispensable, and special care must be taken to reduce the entrance window thickness. The PERCIVAL sensor is being designed by RAL/STFC. A block diagram of the full sensor is shown in figure 2. Figure 1 illustrates the pixel architecture: The basic 3T structure (source follower, reset, and select transistors) is enhanced by the addition of a series of switches (SW0-2, AB) and capacitors (C0-C2). During charge integration, the gates of the SW transistors connecting the capacitors are biased moderately at around 0.7V. Under low-flux conditions, the diode voltage is not lowered

much from its reset voltage (around 2V), no current can flow through the transistors to the capacitors, and the system behaves like an ordinary 3-Transistor Active Pixel Sensor.

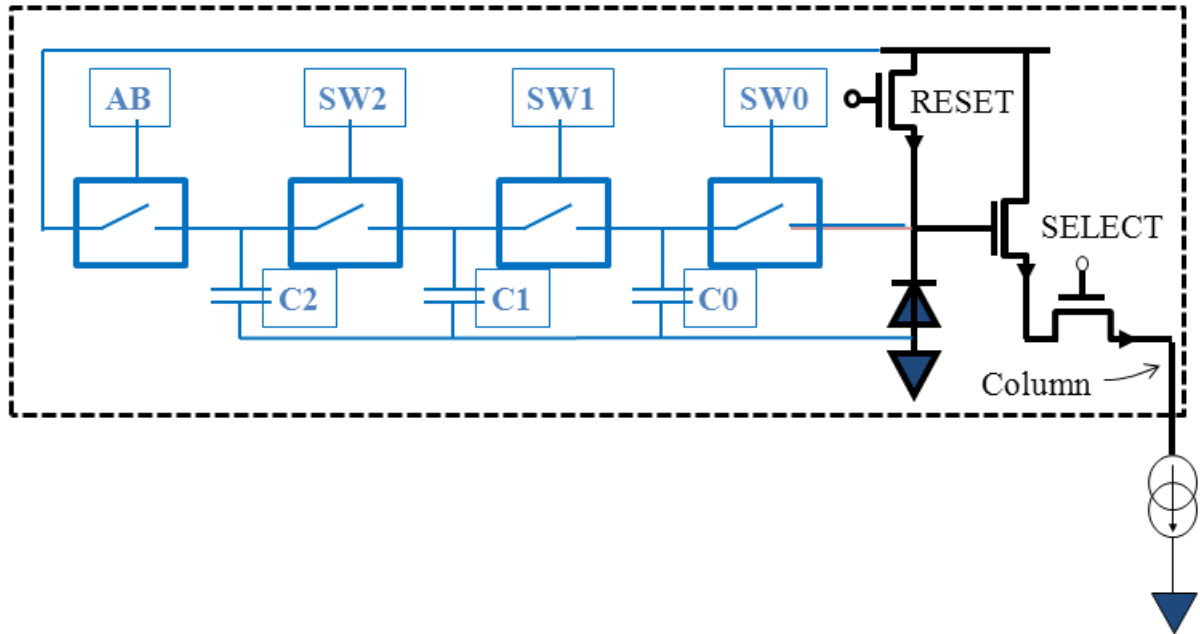


Figure 1. The PERCIVAL pixel. High dynamic range is achieved with multiple readings and lateral overflow. In black the basic 3T pixel, in blue the added overflow structure.

At higher photon fluxes, the diode voltage is lowered significantly, to the point where the diode voltage becomes comparable to the transistor gate voltage. At this point, subthreshold current will start flowing, starting charging the (first) additional capacitor, while the voltage on the diode will stay roughly constant—the system has switched to its second-highest gain mode by combining the capacitance of the diode and the C0 capacitor. During readout, the switches SW0-2 are sequentially opened (resulting in ever increasing effective pixel capacitance) and the resulting source-follower voltages are compared to a threshold in the sampling stage to identify which of the four overall capacitances (and thus gains) is best suited to the charge recorded within the particular pixel and image. In normal operation, only this “best” voltage is passed on to the ADC for conversion (and the gain information is stored). The ADC consists of a coarse and fine stage with two different current ramps, allowing for a total of 12-bit (plus one bit overrange) conversion. Together with the 2-bit information recording the gain (= SWx switch setting), 15 bits per pixel and reading must be transmitted to the readout. The sensor is designed to allow for digital correlated double sampling (CDS), i.e. recording the baseline voltage in each pixel before charge integration, and this information — although useful only for the highest gain based on diode capacitance only—is also converted into the same 15bits. In order to achieve readout rates of 120Hz over 3710 rows, 7 ADCs per column operating at 7ms conversion time are used. Data from 32 columns is multiplexed into one LVDS data output line running at 460MHz data rate. In total, 111 LVDS lines output the data from 24864 ADCs, resulting in 50Gbit/s (including CDS) image data from a single sensor running at 120Hz.

2.2.The PERCIVAL camera system

The PERCIVAL camera will consist of the CMOS sensor itself plus a combination of electronics boards for power supply, bias, control, and readout – in addition to the mechanical infrastructure required to keep sensor and electronics at optimum operating temperatures, and the computing infrastructure to handle the 50 Gbit/s continuous data stream. Figure 3 shows a block diagram of the camera system. Critical bias and supply voltages will be generated in vacuum close to the sensor on a “Periphery Board”. It is intended to use Low- Temperature Cofired Ceramics

(LTCC) here due to its good thermal-expansion match to Si. The choice of LTCC as PCB material will likely entail splitting this into two physically separate PCBs, with both performing a mix of signal distribution and voltage regulation. This in-vacuum board will also host monitoring capabilities for biases as well as temperatures. From the Periphery board, input (100) and output (120) LVDS lines will have to be routed through flexible leads of several 10s of cm and a vacuum flange to the outside of the chamber, where they connect to a “Carrier” board. This Carrier board will host an FPGA running the finite state machine (FSM), a “Trigger & slow communication” board for receiving timing and control inputs from the outside world, and two “Mezzanine” boards each hosting one FPGA for data handling, memory, and four 1-10Gbit internet links. This Mezzanine board [1] is a custom DESY development shared by AGIPD[2,3], LAMBDA[4], and PERCIVAL, and is already used in today's test configuration. While the sensor functions at room temperature, optimized noise performance is expected around -40C, and many science applications demand that the sensor be mounted movable within the vacuum chamber. The mechanics, cooling approach, and physical layout of the electronics for the full-size sensor will be designed with maximum user flexibility in mind.

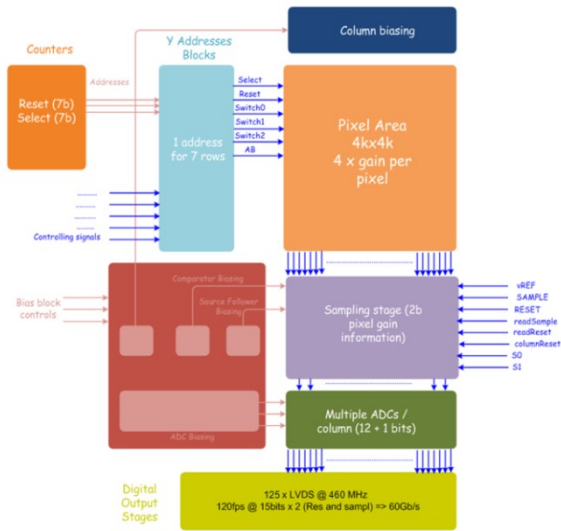


Figure 2. The PERCIVAL full sensor block diagram

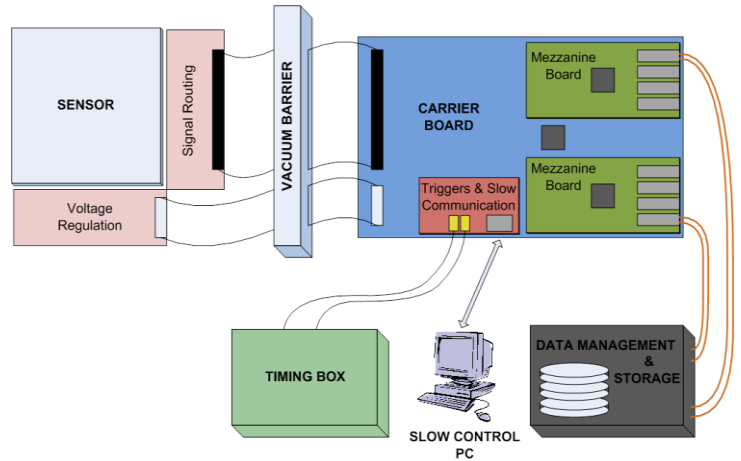


Figure 3. Block diagram of the PERCIVAL camera.

2.3. The PERCIVAL test system

Test chip(s) Before designing and fabricating a full 10_10cm² chip, smaller test sensors were produced to both evaluate the performance of various pixel architectures, gain decision logic, and the ADC and to verify the fast digital output circuitry. The sensors are fabricated in a commercial 180nm CMOS technology. Test Sensors 1 and 2 (“TS1” and “TS2”), with 210x160 25-μm-pixels each, allow comparison of a total of 12 different pixel designs (70x80 pixels each), with identical periphery. Half use an annular partially pinned photodiode[5], half are based on a more conventional n-well diode design. These sensors use slower CMOS output lines (8 single-ended CMOS outputs nominally running at 20MHz) and slightly less efficient data formatting (12% padding zeroes), but enable testing of the pixel and ADC performance at full readout and conversion speeds. TS1 and TS2 are currently undergoing detailed testing in front-illuminated configuration (see section 5). After preliminary tests ascertained TS1 and TS2 are functioning properly, wafers with TS1 and TS2 chips on 18mm epilayer were forwarded to NASA’s Jet Propulsion Laboratory (JPL) for backthinning; first backthinned TS1 and TS2 chips are expected in January 2014. The TS1 and TS2 chips are wire-bonded to a carrier board (Chip on Board, or CoB) which interfaces to both the custom readout system described in section 4 and the standard

imager test system employed at RAL/STFC. A separate test sensor, “TS3”, incorporates the more efficient multiplexing and faster data streamout needed for the full sensor. Data from 32 columns with their 7 (+ one backup) ADC are multiplexed to a single LVDS output. TS3 also incorporates a PLL, on-chip bias current generation, and LVDS inputs. At room temperature, the TS3 performs as expected, tests at operating temperature (around -40C) are expected to yield similar results.

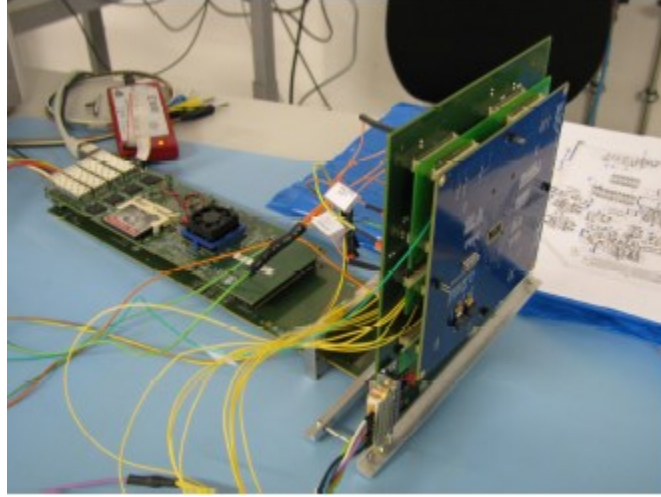


Figure 4. The test setup on a benchtop. From right to left, CoB with test chip, interposer board, periphery board. The latter connects to the horizontal SD board (note the vacuum barrier flange already in place), on which in turn the Mezzanine board is placed. See text for details.

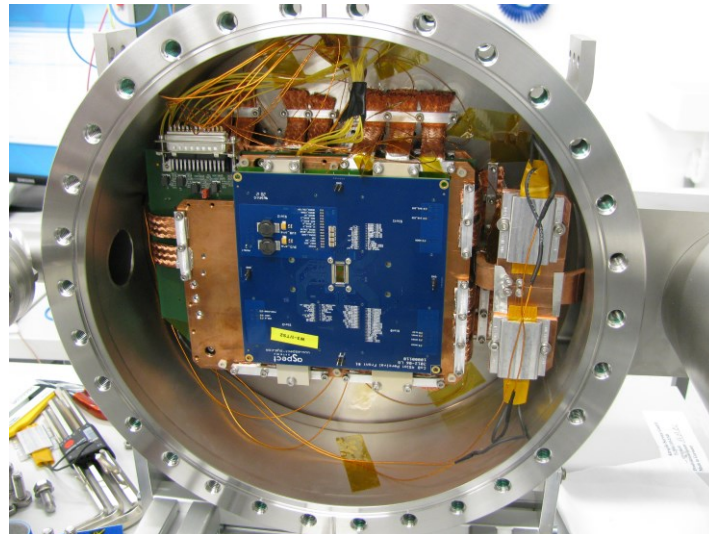


Figure 5. The open PERCIVAL test chamber. Copper plates thermally tied to the chamber surround the Periphery board and provide cooling paths to hot active components, tied to the chamber walls. The cryocooler sits in the chamber extension to the right, resistors on the cold finger provide counter-heating.

3. Experimental part

3.1. The PERCIVAL Test Periphery Board

3.1.1. Checking of the board

Biases and supplies for the test chip are generated on the so-called periphery board. In theory different instance of this board should give always the same biases. But in practice is not so. So for each of these periphery boards we had to measure the output meaning the bias provided to the chip when a certain digital input is given. We have measured the voltage and current with the help of multimeter.

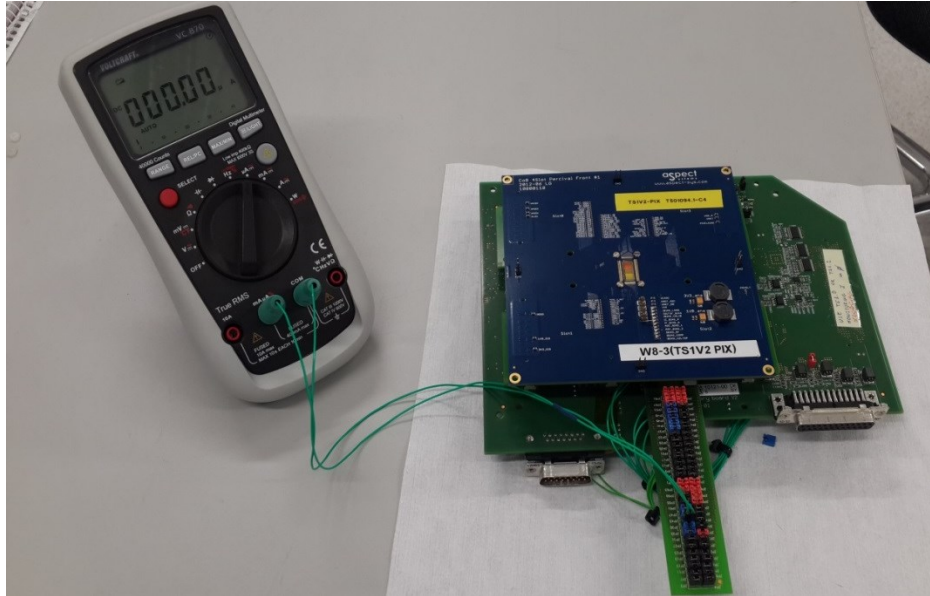


Figure 6. Periphery board with the chip TS 1.2, connected to the multimeter.

In one instance, a board did not work properly, because the resistor R697 was wrong, replacing the 0Ω resistor there with the proper $1k\Omega$ enabled proper operation of the board.

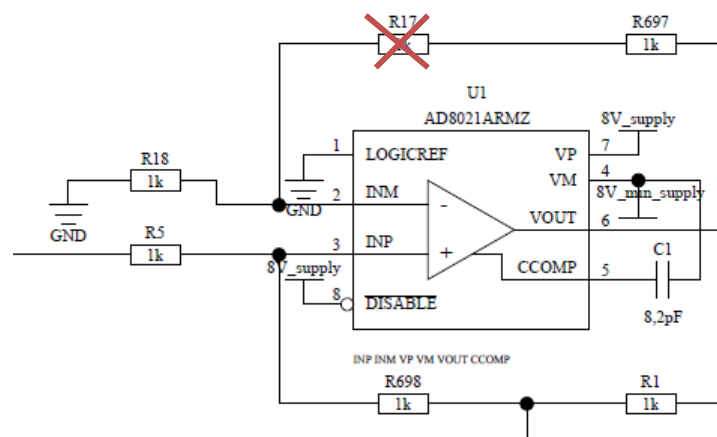


Figure 7. The part of the current source. The wrong resistor R697 was shown in this figure.

3.1.2. Finding the optimal bias for each board

The boards, actually, may have different optimum digital settings. We gave different digital input to the board and we measured the analog output. Then we found out the output, which is

nearest to the output that we wanted to achieve. And that is the optimal operation point for the board. We repeated this on all biases.

3.1.3. ADC calibration of the board

The ADCs on the periphery board read back the bias voltage that are generated. We had to calibrate the ADC, so that the read out is not a digital number, but it is also current or voltage. We have taken the output of ADC and we have taken the measured value, this is a linear fit.

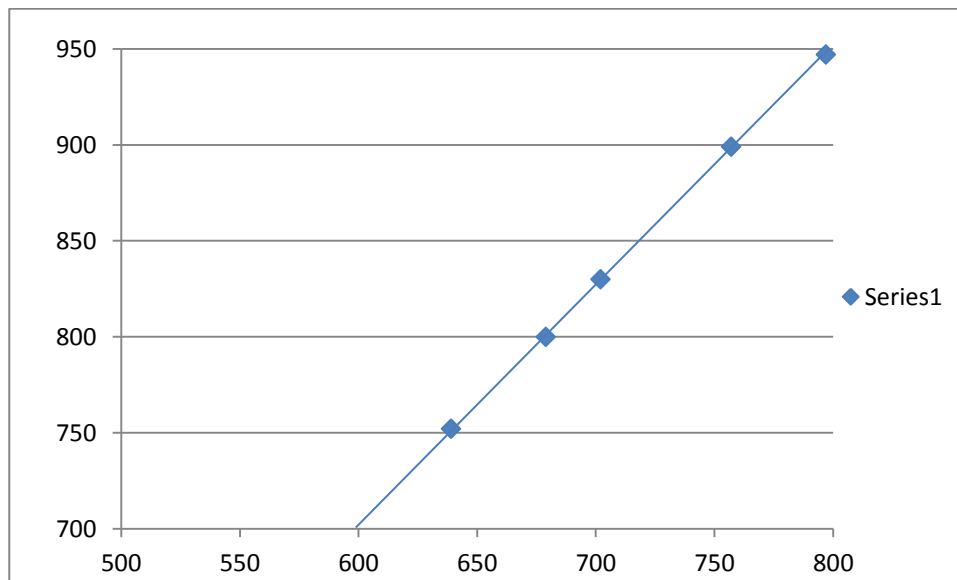


Figure 8. The linear fit – the relationship between ADC output and the output that we have measured.

ADCbias1					
dig input	meas I [uA]		monitored	slope	offset
100	50,63		531	0,08009906	8,17266776
125	64,55		703		
150	78,38		876		
175	92,25		1049		
189	100,04 std		1148		
ADCbias2					
dig input	meas I		monitored	slope	offset
150	75,29		1068	0,08556902	-17,220629
175	89,22		1248		
195	100,36 std		1385		
225	117,05		1599		
250	130,96		1700		

Figure 9. Calibration constants, relating ‘monitored’ to ‘meas. I’

3.2. Calibration of the chip

We have basically done 3 things with the chip:

- We did the ADC calibration of the chip
- We made a PTC
- We have taken a lot of dark measurement in several conditions to evaluate the noise

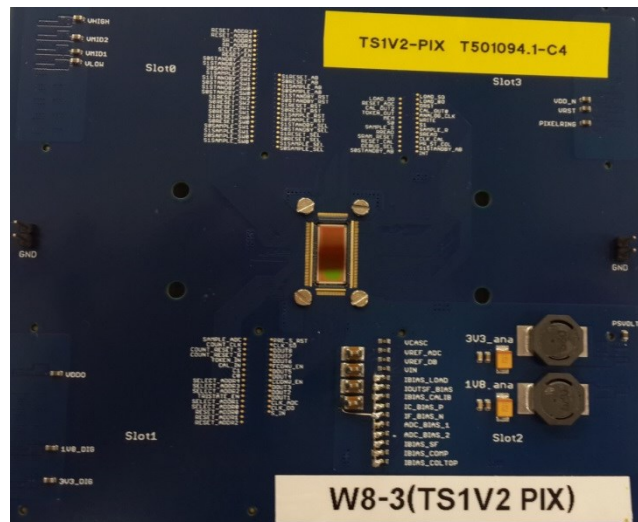


Figure 10. The newest PERCIVAL prototype chip is called “TS 1.2”

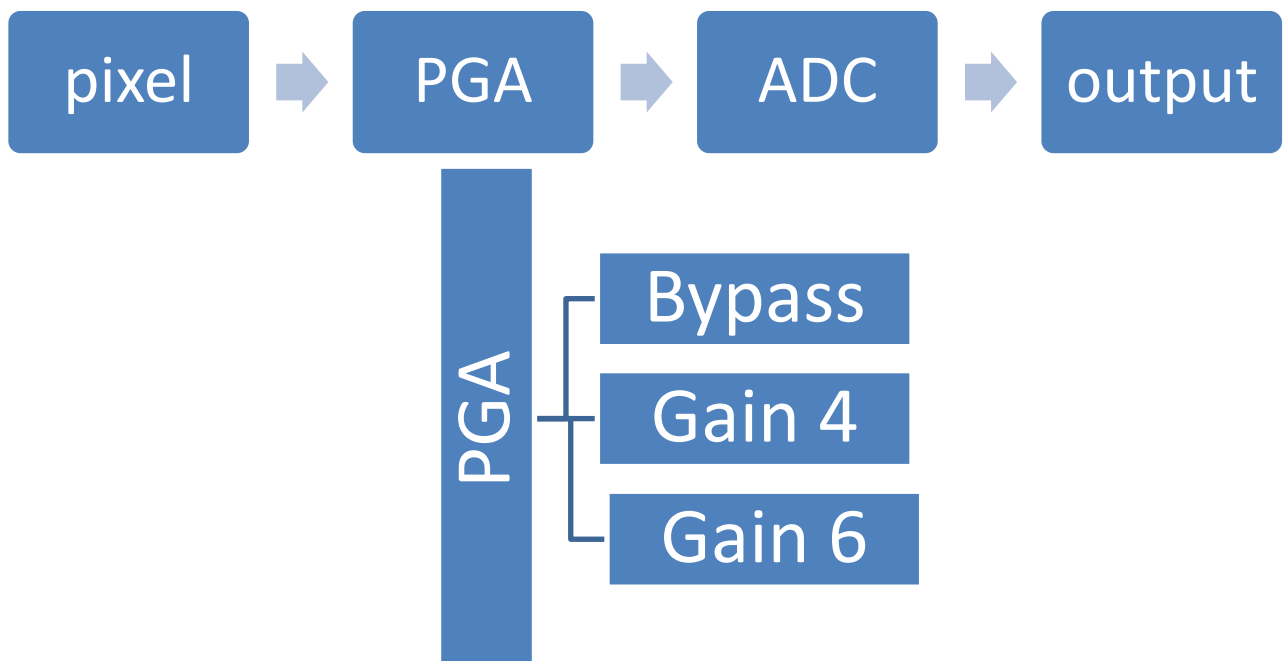


Figure11. The signal comes to the pixel ,then it passes to the PGA which has the 3 different gains. The signal comes to the input of the ADC and from the output of ADC we can readout the output.

3.2.1. The ADC calibration of the chip.

The chip gave out two different number: fine ADC value (0-255) and the coarse ADC value (0-31), which could be interpreted like the least significant bit and the most significant bit of the number. We have to put this two numbers together to provide it total number. And this we have done by making a measurement, by giving an input that changes a voltage provided at the top of each column for testing proposes , the V_{in} , and seen the output of the ADC. Putting these two things together, we obtained this curve . Another result that we have obtained is that we see the curve, and in some points it is not a straight line. That means, that there is a region in which the system is not linear.

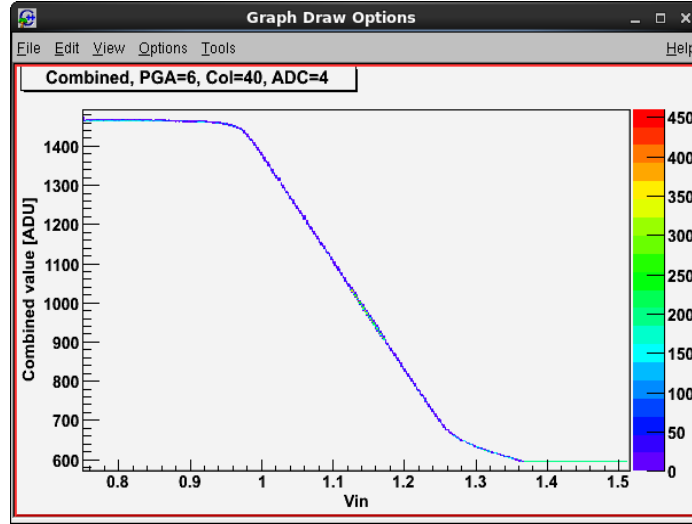


Figure12. Relationship between Vin and combined value (coarse value and fine value)

3.2.2. Photon Transfer Curve Calibration

We have made a Photon Transfer Curve (PTC) calibration. First step is to produce an average over a given Region of Interest (RoI) for each integration time:

$$\bar{x}_{Dark\ corr, TInt} = \frac{1}{N} \sum_{i,j} \bar{x}_{Dark\ corr.}$$

$$\sigma_{Dark\ corr, TInt}^2 = \frac{1}{N} \sum_{i,j} \sigma_{Dark\ corr.}^2$$

Finding the 0.5 slope in the linear region corresponds to the shot-noise limited case in the sensor response ($Noise \cong \sqrt{N_\gamma}$) and allows for a lot of other calculations to be made. We can take the log-log PTC- based calculations using the equation for the 0.5 slope in the form of $y = mx + c$:

$$\left[10\left(\frac{-c}{m}\right)\right]^{-1} = Gain_{log}$$

$$\min_{TInt} \left[(\sigma_{Dark}^2)^{\frac{1}{2}} \right] = Noise_{log} (ADU)$$

$$\frac{Noise_{log} (ADU)}{Gain_{log}} = Noise_{log}(e^-)$$

The noise taken in this method is from the dark measurement.

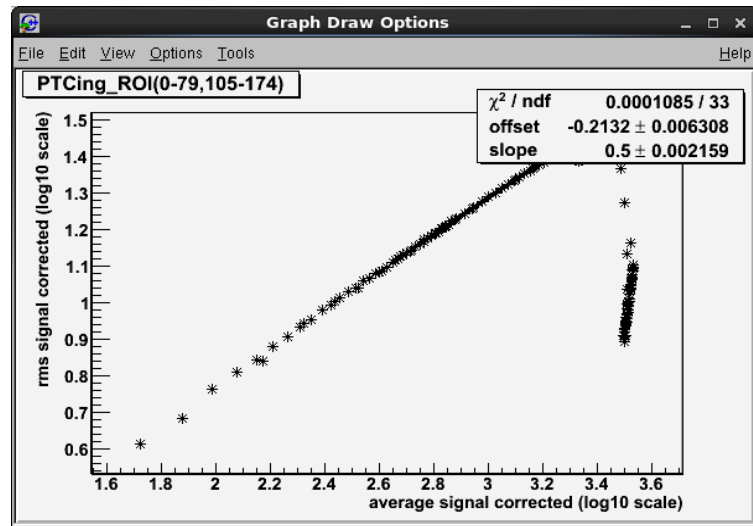


Figure 13. Average signal corrected dependency values for the rms signal corrected values

3.2.3. Dark measurements

We have made dark measurements at different integration times. We wanted to see how much the noise evolves increasing the integration time. We did measurements for 3 different PGA Gain. We can see that a higher PGA gain reduces the noise.

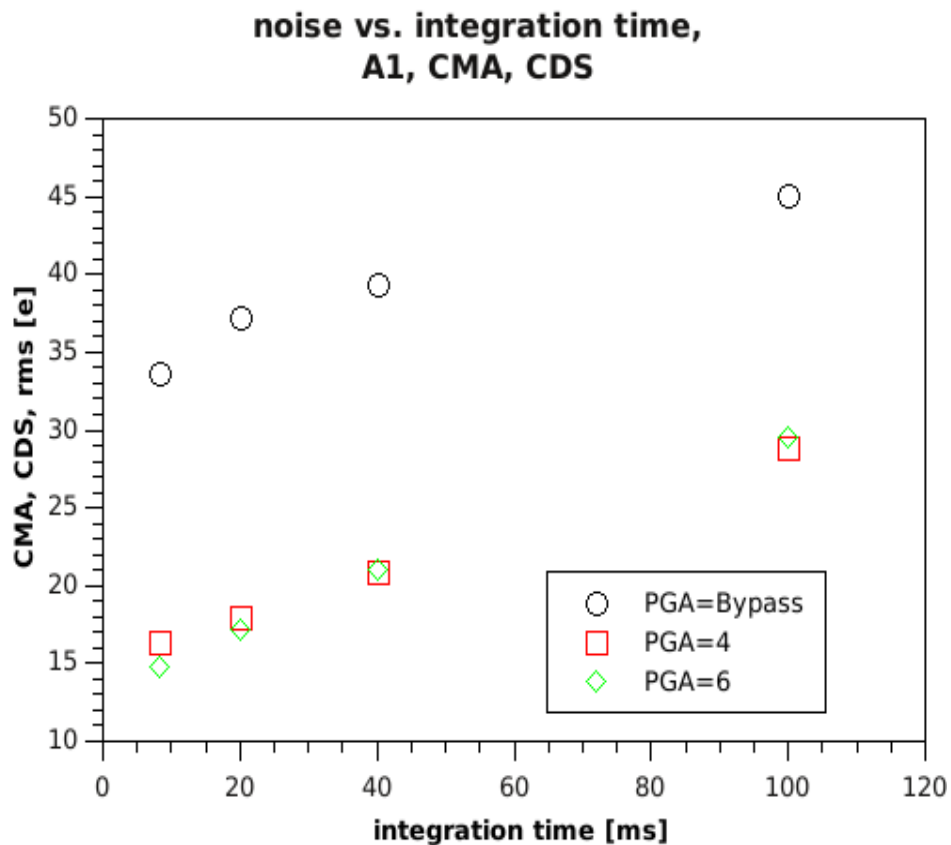


Figure 14. noise resolution as a function of integration time for several types of gain . At PGA =4 and PGA=6 the result is almost linear

4. Conclusion

- We worked with the newest test chip TS 1.2. and found out the values which is nearest to the values that we wanted to achieve for all biases
- We did the ADC calibration of the board. The relationship between two values (coarse and fine) was not a linear.
- We took dark measurements. Increasing the integration time increases the noise and a higher PGA gain reduces the noise.

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