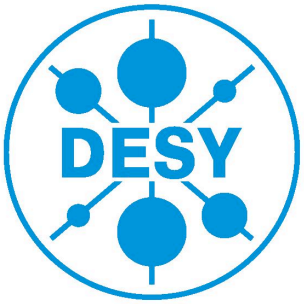

Trigger Threshold Verification for the Hadronic Calorimeter Prototype for the ILC

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Abstract

This report outlines the development of a trigger threshold verification system for the commissioning of an analogue hadron calorimeter developed by the CALICE collaboration for an International Linear Collider project. This method uses the LED system which was already integrated into the front end electronics, and the two trigger modes of the prototype. The aim is to investigate the behaviour of each channel and verify that the trigger threshold set does not exceed the value of 0.5MIP. This study serves as a preparation for the upcoming testbeam in CERN scheduled from October to December 2014. The results shows that the method is a fast, safe and reliable way to verify thresholds without incurring additional cost.

Contents

1 Introduction

1.1 The International Linear Collider

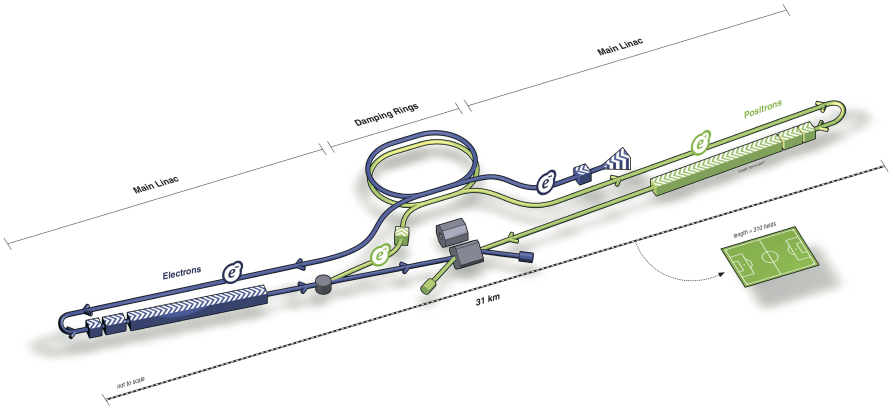

Figure 1: The Internatinal Linear Collider

The International Linear Collider (ILC) is a proposed e^-e^+ linear collider with a center of mass energy of 500GeV (upgradable to 1TeV). It has a length of 31km. Figure 1 shows a conceptual sketch of the ILC. The ILC is a precision machine that uses well define initial state of pointlike particles for collision to produce clean final states. Kitakami City, Japan is the proposed location for the ILC to be built.

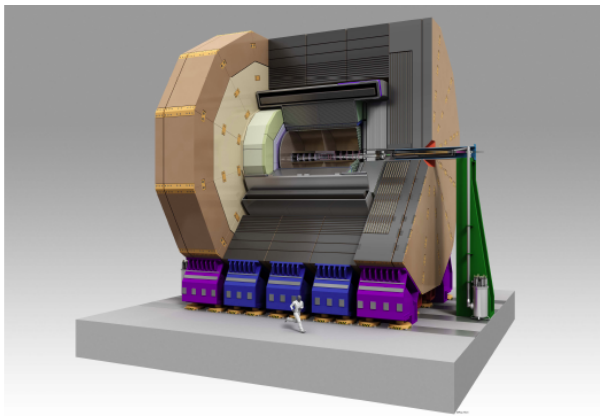

Figure 2: The ILD

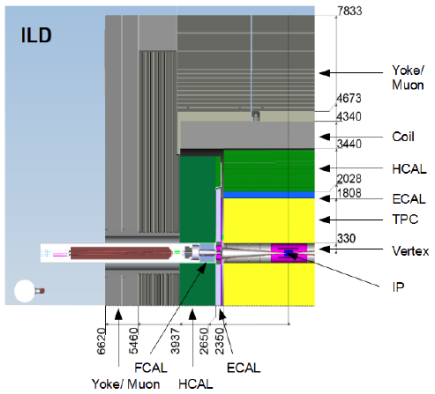

Figure 3: Section view of the ILD

Figure 2 shows the International Large Detector(ILD), which is one of the two proposed detectors for the ILC. It has an onion-like structure which is shown in Figure

3. The layer in green is called the hadronic calorimeter. As the name suggest, it is the calorimeter for hadronic particles. There are several proposals for the hadronic calorimeter. The subject of interest for this report will focus on the hardware development of the analogue hadron calorimeter.

1.2 The Analogue Hadron Calorimeter

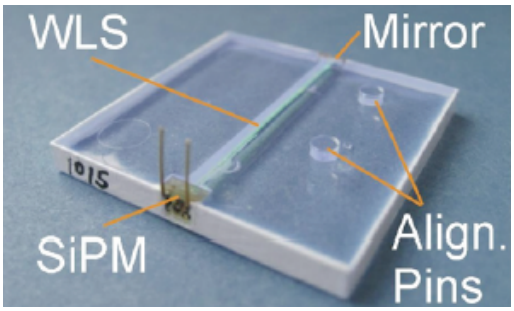

Figure 4: Scintillator tile with SiPM

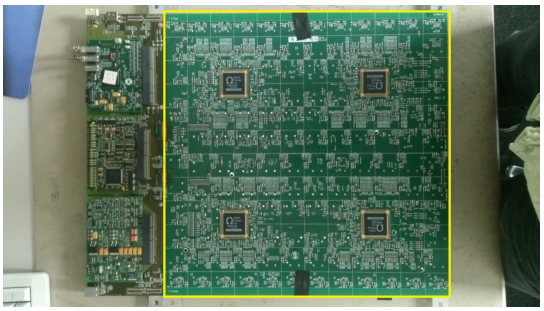

Figure 5: HBU Prototype

The analogue hadron calorimeter is a sampling calorimeter that uses a sandwich structure of steel or tungsten absorber and scintillator tiles. Figure 4 shows the 3cm x 3cm scintillator tiles with SiPM before it is covered with reflector foil. Each channel of this setup is readout by the SPIROC2b Application Specific Integrated Circuit (ASIC). 4 SPIROC2b chips are mounted on a board of readout electronics, which is called the HCAL Base Unit(HBU) shown in figure 5. This is the base unit for the AHCAL in which the scintillator tiles and SiPM is mounted on the bottom side of figure 5. Each SPIRO2b ASIC can accommodate 36 channels, thus a total of 144 channels are available for each HBU.

Data acquisition system(DAQ) of the HBU for simple testing in the lab are done using the LabView software. Trigger threshold and LED amplitude settings setting (which will be explain in the next session) for each SPIROC2b chip are all done using this software.

1.3 Triggering system

Triggering is the part of the calorimeter where it filters out unwanted events or noise. The triggering system of the HBU consist of the auto trigger mode and the external trigger mode. In external trigger mode, all events are recorded and the time distance between each trigger can be defined in the DAQ software. In auto trigger mode, only events with signal larger than the threshold will be recorded. Auto trigger threshold are set via DAC counts which are loaded into the SPIROC2b chips via the LabView program. However, for the same DAC threshold settings, the output threshold position in terms of ADC counts varies with each channel. In addition, it is only possible to set a

global trigger threshold for each SPIROC2b chip. Therefore, it is crucial to define a good global trigger threshold for each SPIROC2b chip(that works for all 36 channels in the chip). Previous measurements using testbeam shows that 0.5MIP is a upper boundary where the threshold setting is at optimum with an acceptable noise level.

2 Trigger threshold study using LED system

The goal of this study is to verify that the trigger threshold DAC value set for each SPIROC2b chip does not exceed 0.5 MIP. This is done by extracting the trigger efficiency curve by comparing the auto trigger LED runs with the external trigger LED runs. The trigger position are then extracted from that and plotted to an ADC vs DAC threshold plot. The plots are fitted and extrapolated down to calculate the position of threshold for 0.5MIP in DAC counts.

2.1 The LED system

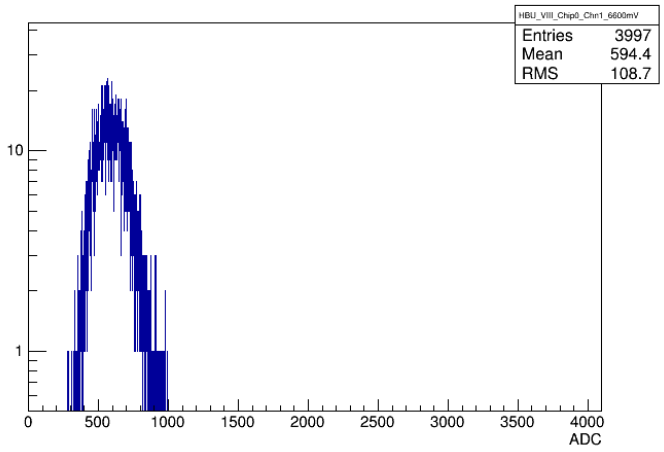

Figure 6: ADC output of a typical LED run at VCALIB = 6600mV.

The AHCAL engineering prototype is equipped with one LED for each channel originally meant for the gain calibrations of the SiPMs. The LEDs are located on the HBU and transmit light directly to the scintillator tiles. All LEDs are synchronized to generate light pulses in which the light amplitude is controlled by the "VCALIB" which has a range of 0mV to 10000mV. The optimal VCALIB in which good signal can be seen varies from channel to channel, depending strongly on the type of SiPM used. Figure 6 shows a typical ADC histogram of a run for a channel using LED system.

2.2 Measurement method

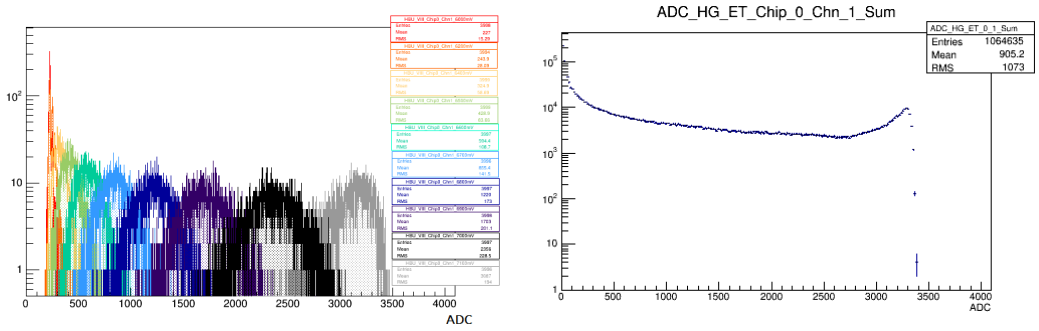

Figure 7: On left, spectra of runs with different VCALIB in the range of 6000mV to 7100mV in external trigger mode. The pedestals for these runs are subtracted and sum up and shown as the black plot on the right.

The triggering modes are briefly mention in section 1.3. Since the external trigger takes all data regardless of the signal pulse height, a sum of all data with pedestal mean subtracted are taken by varying the VCALIB will result in a spectra shown in the right plot of figure 7. The pedestal mean for each channel is calculated by taking the mean of the pedestal within a 2 RMS range from the bin with maximum content[3].

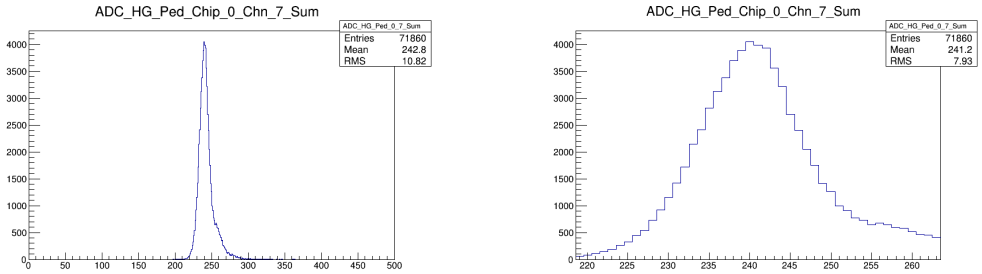

Figure 8: Histogram of a pedestal of a typical channel is shown in the left plot. The right shows the same plot but with a ADC range of 2 RMS from the peak value. The mean for the right plot is used as the actual pedestal value.

By repeating this with the auto trigger mode, we will obtain a spectra which it starts to build up at some ADC value(shown in red, green and blue plot in figure 9). In this plots, the DAC values for trigger threshold are set to a rather high value of 300, 350 and 400 to minimize noise. A normalizing procedure (which scale all number of cycles of each run to the same value) is perform to correct the statistics for each plot. Following that,

if we divide the external trigger spectra with the auto trigger spectra, we can extract a trigger efficiency curve.

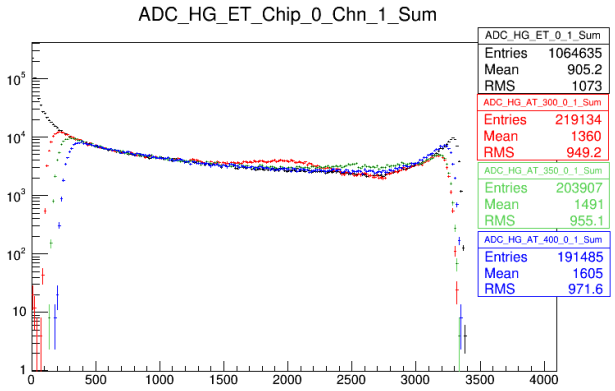

Figure 9: Spectra of external(black) and auto trigger runs(red for trigger threshold DAC set at 300, green for 350 and blue for 400).

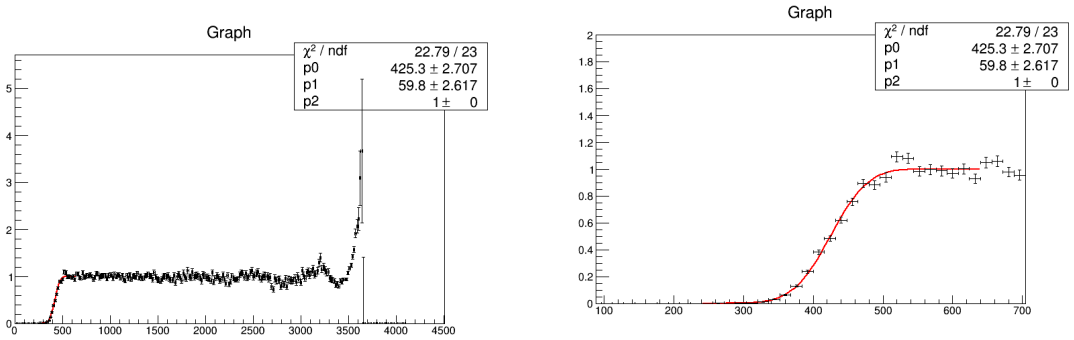

Figure 10: Right plot shows the divided plot for a typical channel.Left plot is the same plot but it is enlarged at the position when the trigger efficiency starts to rise

Figure 10 shows the divided plot which shows the trigger efficiency for a typical channel. The trigger position (in terms of ADC) is then define to be the point at which the trigger efficiency is equal to 50%. For the division to work, it is important that both external and auto trigger runs are taken within the same VCALIB range and with the same voltage increment per step. Setting the same VCALIB does not guarantee the same light amplitude from the LED, therefore it is also important that external and auto trigger measurements are done together for each VCALIB and there should not be any time delay in between. As shown in figure 10, error function in the following equation (1)

$$f(x) = p2 * \mathrm{erf}(\frac{x - p0}{p1}) \tag{1}$$

where,

$p0$ = trigger position
$p1$ = trigger width
$p2$ = normalizing factor

was used to fit the divided plots. It is also important to be careful with errors calculated after the division because this will affect the fit of the curve. Generally, the fitting function does not take into account of zero values. To have a more accurate fit on the divided plot, there are 4 simple conditions:

$$\text{Trigger Efficiency}_i \ , \ \frac{\mathrm{AT}_i}{\mathrm{ET}_i} \begin{cases} \mathrm{AT}_i = 0, \mathrm{ET}_i = 0 \ ...(\mathrm{a}) \\ \mathrm{AT}_i = 0, \mathrm{ET}_i \neq 0 \ ...(\mathrm{b}) \\ \mathrm{AT}_i \neq 0, \mathrm{ET}_i \neq 0 \ ...(\mathrm{c}) \end{cases} \tag{2}$$

where,

i = the bin number
AT = bin content for auto trigger
ET = bin content for external trigger

Condition (a) can be ignored while (c) can be fitted normally with TF1 in ROOT using the errors from the division. However, since the result from dividing the plots in condition (b) is the same as condition (a), ROOT will treat the result and its error as zero, thus ignoring it in the fit, when in actual the condition (b) are zero values that we want to take into account during fit. In order to make the fit "see" the zero values in condition (b), assuming Poisson statistics we apply a non-zero error by assuming that this is the result of a true value with an upper limit of 1 σ error to fall into zero. By looking at the basic equation of the division with errors, we have:

$$\text{Trigger Efficiency} = \frac{\mathrm{AT} \pm \Delta\mathrm{AT}}{\mathrm{ET} \pm \Delta\mathrm{ET}} \tag{3}$$

Using gaussian error propagation to calculate for errors and representing trigger efficiency with the symbol r,

$$\Delta\mathrm{r}(\mathrm{AT},\mathrm{ET}) = \sqrt{(\frac{\partial \mathrm{r}}{\partial \mathrm{AT}}\Delta\mathrm{AT})^2 + (\frac{\partial \mathrm{r}}{\partial \mathrm{ET}}\Delta\mathrm{ET})^2} \tag{4}$$

Solving and rearranging,

$$\Delta\mathrm{r}(\mathrm{AT},\mathrm{ET}) = \frac{\mathrm{AT}}{\mathrm{ET}}\sqrt{(\frac{\Delta\mathrm{AT}}{\mathrm{AT}})^2 + (\frac{\Delta\mathrm{ET}}{\mathrm{ET}})^2} \tag{5}$$

where,

$$\Delta AT = \sqrt{AT}$$
$$\Delta ET = \sqrt{ET}$$

For condition (b), we assume a 1σ upper limit for AT. Thus, working out for condition (b) and (c) and simplifying equation (5),

$$\Delta r_i(AT,ET) = \begin{cases} \frac{1}{ET_i}\sqrt{1 + \frac{1}{ET_i}} & \text{for } AT_i = 0 \\ \frac{AT_i}{ET_i}\sqrt{\frac{1}{AT_i} + \frac{1}{ET_i}} & \text{for } AT_i \neq 0 \end{cases} \tag{6}$$

where, for $AT_i = 0$, all values of AT are set to 1 following the assumption that this zero value is the result of 1σ upper limit from true value mentioned before. The errors calculated using equation (6) are plotted to a TGraphAsymmErrors in ROOT (Figure 10) since we can't apply asymmetrical errors into TH1.

Previous study[3] using charge injection shows that the trigger positions shows linear properties in the ADC vs DAC plot. Therefore for each channel, it is safe to assume a linear bahaviour and 3 trigger positions which are extracted for DAC trigger thresholds mentioned previously will be sufficient for this study. The values for 3 trigger positions in ADC counts for each channel are plotted into a graph to get the relation between the input trigger threshold DAC and output ADC cut position. The points are fitted with a simple fitting function and the offset and slope parameter from this fit is used to calculated the trigger threshold DAC for 0.5 MIP.

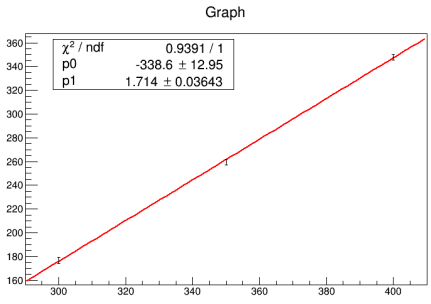

Figure 11: ADC vs DAC triggering threshold for 1 channel

Since it is only possible to set a global threshold for each ASIC and not to each channel, it would be nice if it is possible to get the fit parameters for each ASIC which has 36 channels. Figure 12 shows the profile plot of all 36 channels for 1 of the 4 SPIROC2b ASICs in the HBU. The large error bars in the Y-axis shows that the results varies from channel to channel. This variation is significant and therefore the parameters from this

fit is not an accurate way to compute the trigger threshold for the ASIC. Hence, it is better to compute the parameters for each channel and calculate the trigger threshold DAC value for it individually.

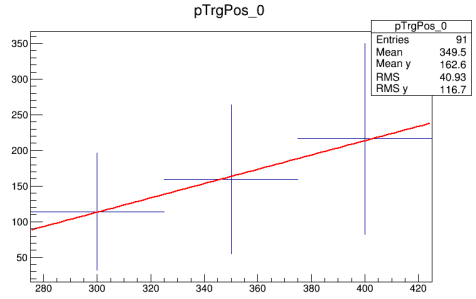

Figure 12: Profile plot of ADC vs DAC triggering threshold for 1 ASIC(36 channels)

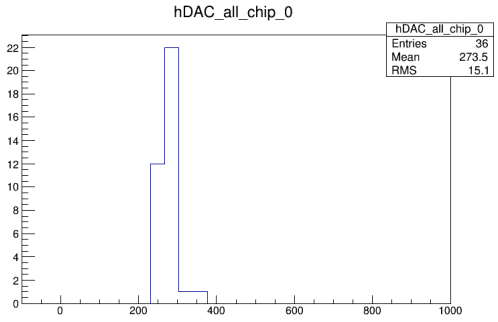

Figure 13: Histogram of 0.5 MIP trigger DAC values calculated for all channels in a typical SPIROC2b chip.

Figure 13 shows an example of this distribution for a typical ASIC. The DAC threshold for 0.5MIP is calculated for each channel and plotted into this histogram. The minimum value in this plot is the limit at which the threshold should not exceed. A fix value for MIP in ADC count is used to see if the method works well. Real MIP values will be needed to verify the actual threshold in the testbeam.

2.3 Testing with the HBU

In order to study the feasibility of this method on actual cases, this study was performed on the actual layers that are planned to be tested at the upcoming CERN TestBeam scheduled from October to December.

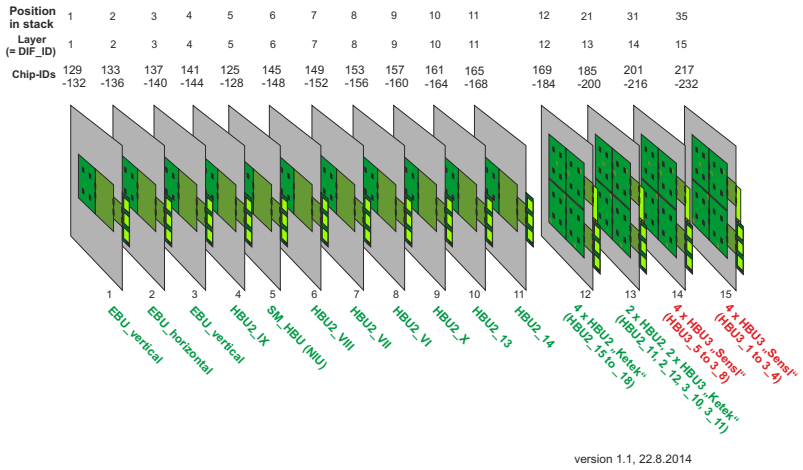

Figure 14: Illustration of the setup for the upcoming CERN Testbeam (by Mathias Reinecke), HBU VI to X are measured in this study

The simple data taking in the laboratory from run to run are taken in such a way that the number of cycles varies. This is to test if the method works when there are uneven cycles in the actual testbeam data. External trigger runs are taken with 1000 cycles in a run with a defined VCALIB and then 4000 cycles in the next run with different VCALIB. As for the auto trigger runs, all are taken with 1000 cycles. For each 1000 cycle runs in external trigger mode, each channel will have around 15000 events. For the auto trigger mode, there will be less number of events because it depends on the VCALIB and trigger threshold DAC applied. The number of cycles are taken so that they are not only useful for this threshold verification study, but it also be used for other purpose such as gain calibration which requires a relatively high number of statistics.

A total of 13 HBUs (refer Figure 14) are measured using this method. For some boards which was tested previously, it was found that there are some noisy channels or channels which are bad. These channels are turned off and not taken into account during the measurement. Depending on factors such as the LED light output, the light coupling between the scintillator tiles and the SiPM, the gain and pre-amp settings, the resulting output of each channel varies and need to be studied carefully when determining the range of VCALIB to be set. Typically a VCALIB of a range of 1.5V with an increment of 50mV per step should be sufficient.

The Trigger Threshold $\mathrm{DAC}_{<0.5MIP}$ (values in Figure 13) are calculated by dividing half a fix ADC/MIP value. This fix ADC/MIP is the result of deducting the actual pedestal mean from a fix value of 600, which is based on previous testbeam results, for

each channel.

2.4 Results and discussions

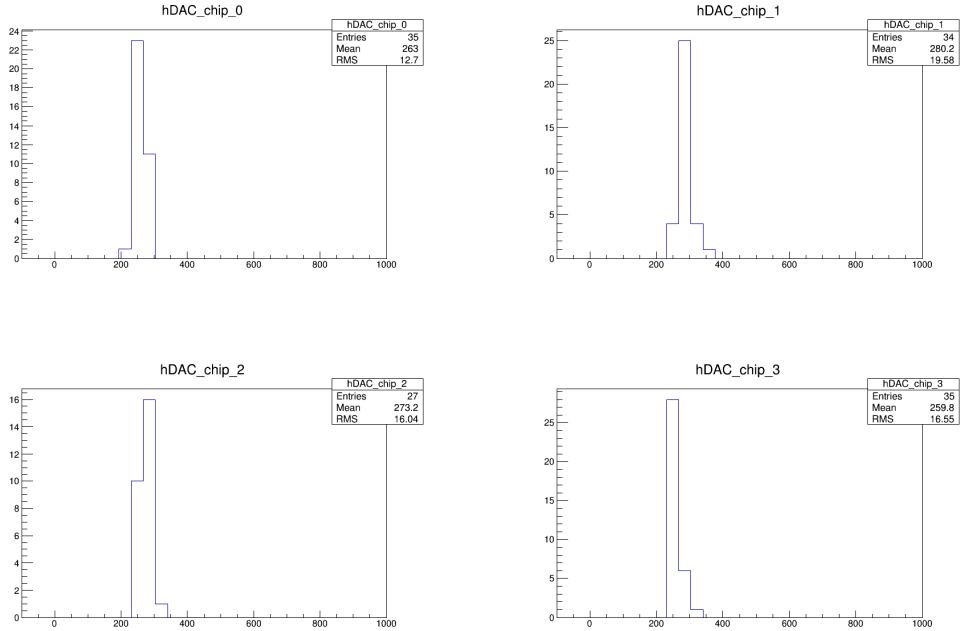

Figure 15: Plots of 0.5MIP trigger threshold in DAC for HBU_{3_1} ASIC 1(Top left), ASIC 2(Top right), ASIC 3 (Bottom left) and ASIC 4 (Bottom right). Only channels with passed fits are included in the plots.

From the measurement it was found out that most channels shows good fits and some typical plots for the trigger threshold DAC are shown in figure 15. Since each channels LED amplitude is not uniform with the voltage applied, it is not easy to estimate the range of VCALIB that should be set. Choosing a wider range would solve the channels which requires higher LED amplitude but this will increase the amount of time needed. The amount of time taken for each HBU data taking is about 6 to 7 hours. The relatively long time required for the data taking is because a high number of statistics are required for other purposes such as gain calibrations. In the planned testbeam, a new readout system which can take the data for all boards at the same time will be used and this will further reduce the amount of time required to do this measurement.

Table 1: Trigger Threshold $DAC_{<0.5MIP}$ for all channels calculated using estimated $ADC_{MIP_{signal}}$

HBU No.	Chip No.	$DAC_{<0.5MIP}$	HBU No.	Chip No.	$DAC_{<0.5MIP}$
VI	0	275	2_15	0	196
VI	1	249	2_15	1	228
VI	2	276	2_15	2	245
VI	3	287	2_15	3	245
VII	0	279	2_16	0	226
VII	1	274	2_16	1	255
VII	2	262	2_16	2	230
VII	3	287	2_16	3	240
VIII	0	263	2_17	0	223
VIII	1	252	2_17	1	248
VIII	2	270	2_17	2	223
VIII	3	264	2_17	3	253
IX	0	215	2_18	0	211
IX	1	219	2_18	1	243
IX	2	149	2_18	2	233
IX	3	231	2_18	3	237
X	0	293	3_1	0	227
X	1	231	3_1	1	254
X	2	214	3_1	2	235
X	3	124	3_1	3	233
2_13	0	208	3_2	0	244
2_13	1	216	3_2	1	246
2_13	2	219	3_2	2	251
2_13	3	207	3_2	3	236
2_14	0	114	3_7	0	263
2_14	1	206	3_7	1	261
2_14	2	157	3_7	2	250
2_14	3	186	3_7	3	269

The results for the HBUs tested are shown in Table 1. The values in table are just estimation since a dummy ADC/MIP value was used as mentioned in the previous section. Some chips has very low value (eg. HHBU No. 2_14, Chip no. 0), this is due to the limits set to remove bad fit data is not fully optimized yet. More work still needs to be done to perfect this method and better results are being foreseen.

3 Summary

A new method to set and verify the trigger threshold has been established. This method uses the LED system of the AHCAL engineering prototype to take runs in auto trigger and external trigger mode. The sum of plots for auto trigger are divided by the sum of plots for external trigger to extract the trigger efficiency. The position at which the trigger threshold acts on is then define from the trigger efficiency plot where the efficiency is at 50%. This is done for 3 trigger threshold settings of 300, 350 and 400 DAC counts. The positions in ADC counts for each trigger threshold are plotted into a graph where it is fitted and extrapolated down to calculated for lower DAC values. Using this plot we can compare the actual threshold applied and verify that for each channel it does not exceed 0.5MIP. This method is very safe as no channels was damaged during the study, and it can be done in a relatively short amount time with an acceptable level of accuracy. In addition to that, the use of LED system which was already integrated into the AHCAL prototype means that no additional hardware modification nor cost are required for this measurement.

4 Acknowledgments

I would like to thank my supervisor Katja Krüger and also Oskar Hartbrich for their continuous support, extreme patience and perfect guidance throughout the summer student program. They made this summer program truly meaningful to me and I will not forget it many thanks to them. I also thank Eldwan Brianne and Huong Lan Tran for being exceptionally helpful and for their truly valuable discussion with each other. I would also like to express my greatest gratitude to Mathias Reinecke for sharing his outstanding expertise and his precious time in answering all my silly questions.

I am also truly grateful to Felix Sefkow, Aliakbar Ebrahimi, Benjamin Hermberg, Jiří Kvasnička, Hörmfred Hartmünd, Shaojun, Dmitry Mironov and the FLC group for all the knowledge they have all shared with me. I would also like to thank the other summer students especially Christian Röske for making this a great experience.

Finally, I would like to give a special thanks to the summer student program coordinators especially Andrea Schrader for the hard work and support for the summer student program.

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