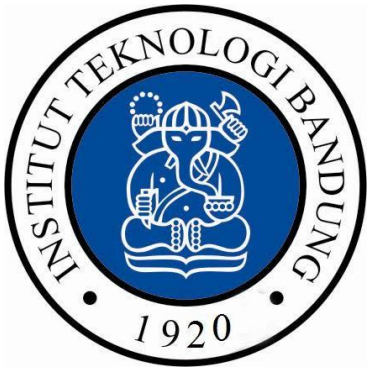


Summer Students Programme 2014

DESY Hamburg – FEC Department

Andi Wahyu Multazam, Institut Teknologi Bandung, Indonesia

September 10, 2014

Abstract

This report comprise 2 kind of projects; first, circuit design and implementation of 100 μA high pulse current source. The high pulse current should be able to have short rise time and overshoot as possible as it can made. At the end of experiment, it has 2 best possibilities result. First, 0.984 V amplitude, with 100 ns width pulse, 34.27 ns rise time, 3.25 % overshoot, and 6.99 % of undershoot. The other one is current source that has 0.889 V amplitude, with 100 ns width pulse, 34.76 ns rise time, 3.25 % overshoot, and 6.99 % of undershoot. Second, testing and measurement of DSSC main board. The description of system and its data structure has been clearly understood. At the end of this report, there are 8 out of 16 section measurement which was successfully done, and this paper only show one section of an AC signals.

Table of Contents

First Project: Circuit Design and Implementation of 100 μA High Pulse Current Source

1. Introduction

The purpose of this project is to study, design, and analyses high current pulse source that later could be used as pulse generator for ASIC board measurement and testing. Measuring and testing ASIC board need what is so called as high pulse current as input so that finally we could readout data from DEPFET sensor. The last sentence is none of our business, otherwise our circuit design would be used in upcoming days for such measuring stuff. The goal of this 'mini project' is to create and design circuit which able to generate such high pulse. The circuit will have a controllable parameter that are input voltage and resistor. The circuit also will have a independence current pulse $100\ \mu A$ which is very stable.

2. Requirements

Functional

1. Amplitude pulse $\approx 100\mu A$
2. Width pulse $50ns - 100ns$
3. Pulse frequency maximum 2 MHz - 5 MHz
4. Clock frequency above 100 MHz
5. Rise time $\leq 50\ ns$
6. Overshoot $\leq 5\ \%$

Non-functional

1. Single board circuit
2. Avoid of using long cable/wire to connect point to point
3. Good soldering would make good result and stability

3. High Pulse Current Source

Pulse wave or pulse train is kind of non-sinusoidal waveform that is much more similar to square wave with a very short period time of active value. In other words, rectangular pulse wave has small duty cycle. Here is the graph of rectangular pulse. For simplicity, we assume to take an even function

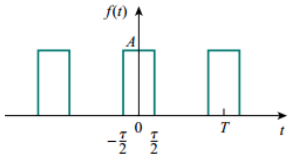
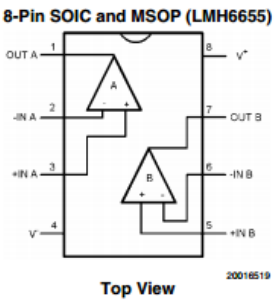


Figure 1: Even function for high pulse current

4. Amplifier LMH6654

The LMH6655 dual high speed, voltage feedback amplifiers are designed to have unity-gain stable operation with a bandwidth of 250 MHz. They operate from ±2.5V to ±6V and each channel

consumes only 4.5 mA. The amplifiers feature very low voltage noise and wide output swing to maximize signal-to-noise ratio.



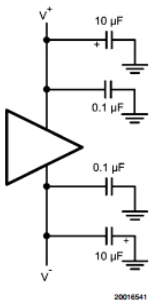


Figure 2: Inside LMH 6654

Figure 3: Capacitance consideration for noise reduction

The PCB should have a ground plane, as it is shown in Fig.3, covering all unused portion of the component side of the board to provide a low impedance path. All trace lengths should be minimized to reduce series inductance.

5. Design Circuit

Designing current pulse source could be vary, depend on what is that current source would be used for. This report present among one of those design which is fit to the requirement. This report is also trying to give insight of what is reason behind circuit design.

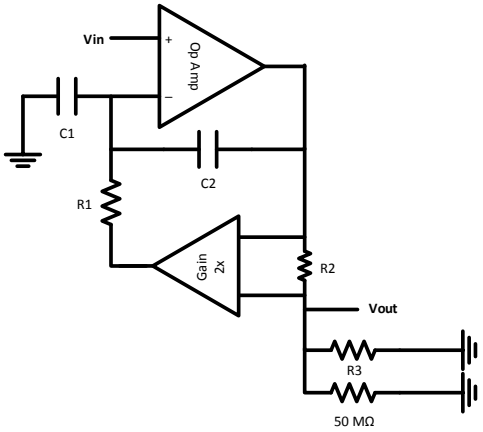


Figure 4: Circuit Design

The circuit design shown in figure 1 consist of 2 IC LMH6654 for which one IC act as Op Amp and another IC act as a block diagram of Gain 2. As mentioned in previous chapter, the current pulse source is designed to be $100\ \mu A$ independent for any impedance of load –in real situation load could be an ASIC chip board, but for the time being of waiting the ASIC board from IBM, it is still possible to replace with somehow another dummy load of $R_3 = 10\ k\Omega$. Apart from this independencies of current pulse to any load's impedance, the circuit should be in controlled with voltage input V_{in} and resistor R_3. The only way to make current pulse I_{source} flowing independence is by putting resistor R_3 between two input of a gain-2 block diagram, because the

pre-requested of current flowing in a wire is there is voltage difference and resistance in between. Moreover it is necessary to put other feedback op-amp as it is drawn above in figure 1. The point is to make node 1 act as a floating voltage, which means their voltage value is not fixed, depend on V_{in} and R_3. This situation could be achieved only by putting operational amplifier, since the output of op-amp depend on previous value of V_{in+} and V_{in-}, or mathematically written as it follows

$$V_{out}(t) = A(V_{in+}(t_-) - V_{in-}(t_-))$$

After putting two block of op-amp altogether, the issue of overshoot and oscillation arise to be overcame. Overshoot is condition when instantaneous output amplitude exceeds the nominal threshold of peak limiting. In this case, overshoot come from at least two different things. First, in a gain-2 block diagram shown by figure 2, two input of the second op-amp do not come at the same time, otherwise V_{2+} comes first and V_{2-} come after. The reason simply because that block diagram have 2 stages op-amp, and signal V_{2-} has to experience going through first stage before hit the second stage, and that take some different amount of times in output of second stage. Second, the output of op-amp simply defined by formula 1 above. But sometimes if pulse change or duty cycle is too short –in about 50 ns– then in a period time of transitioning output voltage there would be an overshoot. Second issue is oscillation that is a phenomenon in any electronic circuit where a positive loop exist between the system's output and input. Oscillation may tend to happen in a so called feedback system. In this circuit design, overshoot and oscillation can be overcame with capacitance and resistor as it is placed. The idea behind is capacitance could act as circuit delay, and resistance able to decrease high overshoot.

Below is a derivation of block diagram circuit with gain 2.

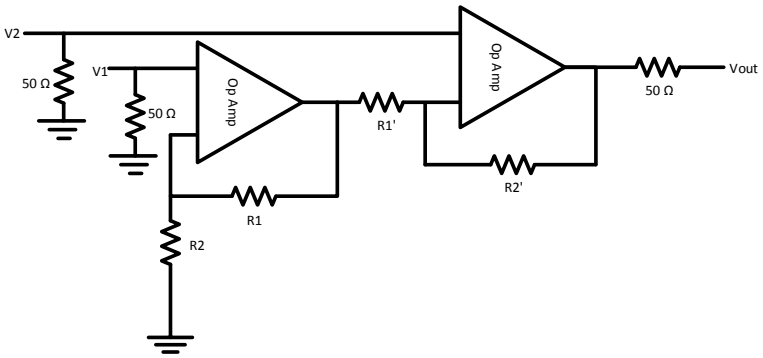


Figure 5: Circuit of Gain 2

Figure 2 is referred to as the two *op-amp in amp*. It is particularly applicable in single-supply system. Dual IC op amps are used in most cases for good matching, such as LMH6654 or LMH6655. By simple calculation the gain is defined as $1 + \frac{R_2}{R_1}$. In practical application, the $\frac{R_2}{R_1}$ ratio is chosen for the desired minimum in-amp gain.

$$V_{out} = (V_2 - V_1)\left[1 + \frac{R_2}{R_1}\right]$$

$$Gain = 1 + \frac{R_2}{R_1}$$

$$\frac{R_2}{R_1} = \frac{R_2'}{R_1'}$$

In this circuit design, we choose R value as it is recommended in datasheet

$$\frac{R_1}{R_2} = \frac{403\ \Omega}{391\ \Omega}$$

$$\frac{R_1'}{R_2'} = \frac{402\ \Omega}{389\ \Omega}$$

$$G = 1 + \frac{R_2}{R_1} \approx 2.03$$

Furthermore, we would like to complete the circuit design by choosing some fix component's value. Here dc analysis and ideal op-amp condition will be used for simplicity of analysis, otherwise there would be some complicated mathematical expression arise which is not really important in approximation. For reminding, there are some characteristics of ideal op-amp ;

1. Input Impedance = ∞ (there is no current to input)
2. Output Impedance = 0
3. Common-Mode Gain = 0 (CMRR = ∞)
4. Open-Loop Gain = ∞
5. Bandwidth = ∞

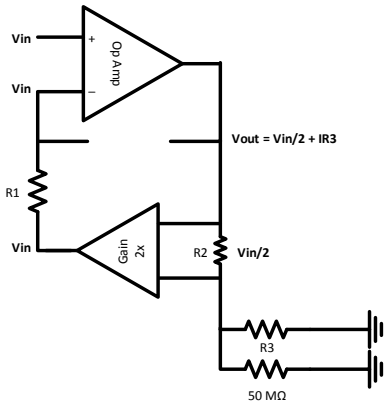


Figure 6: Circuit Analysis

Figure 4 above shows circuit dc analysis. Since current does not enter to the input of op-amp, then we will end up to this simple calculation

$$R = \frac{V}{I}$$

$$R_2 = \frac{V_{in}}{I_s}$$

Where $V_{in} = 100\ mV$, and by requirement $I_s = 100\ \mu A$, then $R_2 = 500\ \Omega$. The value of $R_3 = 10\ k\Omega$ is chosen as it could make voltage shown by oscilloscope equal to 1 V, and that would be a value that is quiet clear to see.

Additionally, the components value of R_2, C_1, and C_2 are value which would make time constants of capacitance as small as possible. Time constants defined as $\tau = R_{eq}C_{eq}$. The smaller value of tau, the faster process of charging and discharging it would be. But, there is one thing that has to be considered while choosing tau, which is oscillation effect. Since capacitor is emplaced as op-amp feedback, then they tend to make oscillation. At the moment, trial and error would be the best way to choose value of R_2, C_1, and C_2. We decided to put $R_2 = 1\ k\Omega$, then capacitance C_1 and C_2 value will follow in diagram below.

6. Implementation and Measurement

Implementation and measurement process of high current pulse generator consist of soldering components, packaging board, measurement, and deciding some left components that are C_1 and C_2. Figure below is a platform circuit board to use in this project

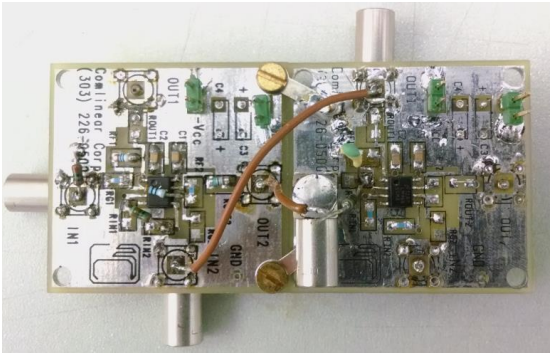


Figure 7: Implementation Prototype

From circuit above, there are still 2 components unfilled, that are C_1 and C_2. Our task is making trade off of measurement which give the best possibility result. Table 1 below shows all the possibilities result of some component's choosing. The measurement work at clock frequency = 100 MHz and signal rate f_0 = 500 kHz.

C1	C2	t-rise (ns)	t-settling		Amplitude (V)	Ripple before C2
			Overshoot rise (%)	Overshoot fall (%)		
1 nF	47 pF	24.39	3.04	4.18	0.5	Oscillate
	56 pF	26.94	3.03	4.52	0.5	
	68 pF	32.67	3.29	4.62	0.5	
	.	.	.	.	.	
	.	.	.	.	.	
	100 pF	45.65	4.03	4.89	0.395	

	120 pF	52.16	4.63	5.05	0.375	
C1	**C2**	**t-rise (ns)**	**t-settling**		**Amplitude (V)**	**Ripple before C2**
			Overshoot rise (%)	**Overshoot fall (%)**		
1.25 nF	47 pF	27.08	6.35	5.99	0.64	Oscillate
	56 pF	27.52	3.1	3.1	0.599	
	68 pF	31.38	2.46	3.42	0.564	
	.	.	.	.	.	
	.	.	.	.	.	
	100 pF	42.84	3.26	3.66	0.486	
	120 pF	47.64	3.69	3.9	0.45	
1	**C2**	**t-rise (ns)**	**t-settling**		**Amplitude (V)**	**Ripple before C2**
			Overshoot rise (%)	**Overshoot fall (%)**		
1.47 nF	47 pF	29.28	5.06	5.92	0.736	11
	56 pF	29.99	2.67	2.61	0.676	
	68 pF	33.29	1.55	2.86	0.635	
	.	.	.	.	.	
	.	.	.	.	.	
	100 pF	44.39	3.23	3.09	0.548	
	120 pF	48.68	3.64	3.32	0.506	
C1	**C2**	**t-rise (ns)**	**t-settling**		**Amplitude (V)**	**Ripple before C2**
			Overshoot rise (%)	**Overshoot fall (%)**		
2 nF	47 pF	33.79	3.35	9.39	0.959	10
	56 pF	34.05	2.88	5.78	0.902	
	68 pF	35.24	1.65	2.11	0.829	
	.				.	
	.				.	
	100 pF	43.09	2.22	2.14	0.713	
	120 pF	47.89	3.02	2.38	0.651	
C1	**C2**	**t-rise (ns)**	**t-settling**		**Amplitude (V)**	**Ripple before C2**
			Overshoot rise (%)	**Overshoot fall (%)**		
2.2 nF	47 pF	32.49	2.55	14.86	1.10	8
	56 pF	34.27	3.26	11.09	0.984	
	68 pF	34.76	3.25	6.99	0.889	
	.	.	.	.	.	
	.	.	.	.	.	
	100 pF	39.13	2.99	3	0.826	
	120 pF	42.43	4.26	3.57	0.748	
C1	**C2**	**t-rise (ns)**	**t-settling**		**Amplitude (V)**	**Ripple before C2**
			Overshoot rise (%)	**Overshoot fall (%)**		
3.2 nF	47 pF	43.02	2.89	23.25	2	6
	56 pF	44.87	2.86	15.55	1.77	

	68 pF	47.02	2.99	11.48	1.53	
	.	.	.	.	.	
	.	.	.	.	.	
	100 pF	43.13	3.23	4.15	1.16	
	120 pF	45.18	4.18	4.17	1.07	
C1	**C2**	**t-rise (ns)**	**t-settling**		**Amplitude (V)**	**Ripple before C2**
			Overshoot rise (%)	**Overshoot fall (%)**		
4.3 nF	47 pF	59.67	1.6	24.77	3.09	5
	56 pF	55.48	1.66	28.75	2.32	
	68 pF	62.13	1.73	11.97	2.02	
	.	.	.	.	.	
	.	.	.	.	.	
	100 pF	49.21	2.93	3.37	1.53	
	120 pF	52.67	3.38	3.77	1.41	

7. Result and Discussion

From the data taken of measurement above, we could see a trade-off components value between capacitor C_1 and C_2. At the beginning, capacitor C_1 is not exist in the circuit design, there is only C_2 on it. The result is somehow oscillation wave. The only possibility for that case is because the circuit is too fast and do not have match timing between one op-amp and others. This is very common problem if the circuit work under high frequency and very short pulse. Our first solution is to make the first op-amp slower by putting a negative capacitor feedback in between. This solution is making the circuit stop oscillating, but not effective enough to produce a good high pulse current. The problem remain is how to shorten the rise time and settling time of the output wave. Then we come up to the next solution, that is to put one more capacitor in node 1 goes to ground. With this solution, the wave form is much better than previous. Moreover, in some sense, adding capacitor would make a delay in a circuit, because capacitor need some amount of time to get charge and discharge consecutively. Our task is to find the best possibility result by choosing a proper value of C_1 and C_2. Otherwise, we have to derive the value with some complicated formula of the circuit transfer function, which is somehow not going good since there are so many forgotten parameter of op-amp in those formula. Furthermore, we could say that the larger capacitance value, the larger of rise time is, because the time constant is increase if capacitance increase.

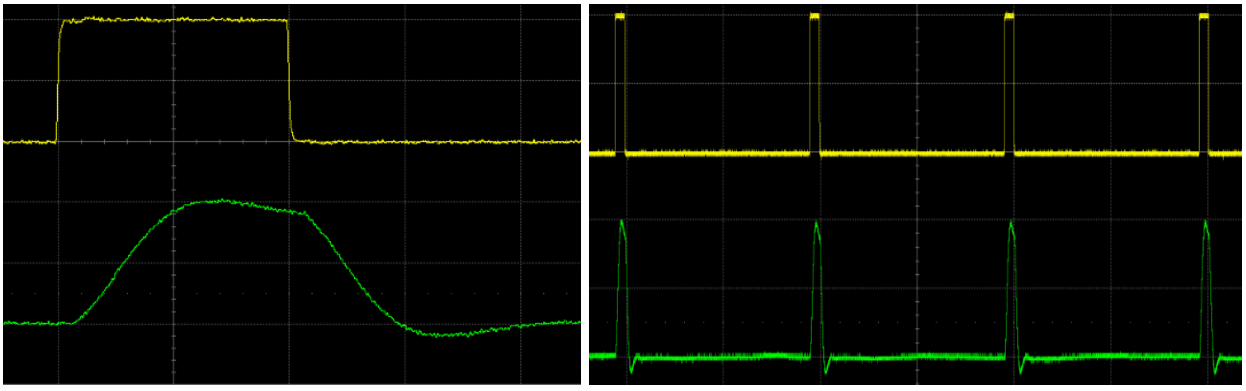


Figure 8: (a) output with C2 = 56 pF (b) overall output

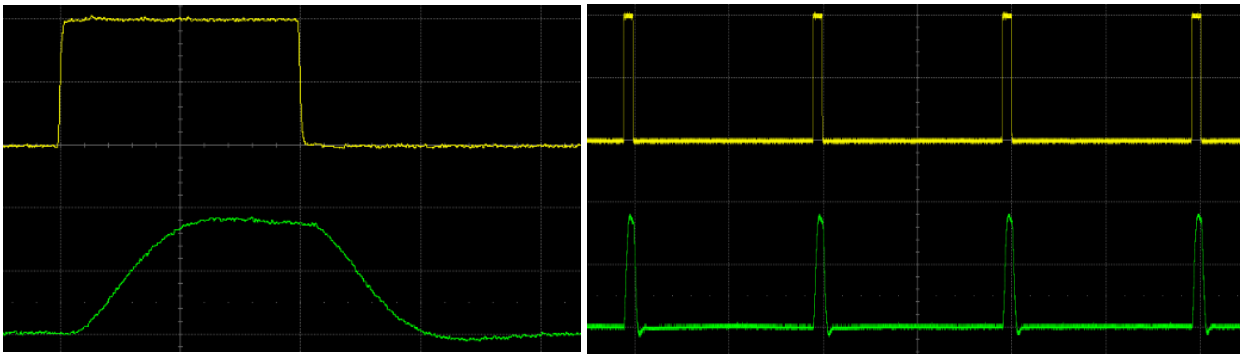


Figure 9: (a) output with C2 = 68 pF (b) overall output

From all the data measurement there are only 2 data which are taken into account. Figure 7 and Figure 8 show the output of current pulse. Those both data have their pros and cons by their self depends on what requirement needed. For instances, if the requirement has to be stick on the amplitude value ≅ 1 V, then figure 7 would be the best result. Otherwise if the requirement need more soft current pulse which do not have much disturbing signal like overshoot and rise time issue, then figure 8 would be the best option. In this case, we could not decide which one is the better, since the requirement itself still to be rough.

Second Project: Testing and Measurement of DSSC Main Board

1. Introduction

In this second project, I deal with measurement and testing of main board which will be used as a part of the whole X-Ray detector. As mentioned before, the system is based on a pixel-silicon sensor with a DEPFET as a central amplifier structure. The sensor will have the following key properties; the total size will be approximately 21 x 21 cm^2 composed of 1024 x 1024 pixels of hexagonal shape. The pixel array will be subdivided in 16 ladders. Every ladder comprise two monolithic sensor with 128 x 256 pixels each. The ladders will be geometrically arranged such that a central hole is left to let the unscattered photon go through. A simplified block diagram of the system is reported in fig.3

Every detector ladder is bump-bonded to mixed signal readout ASICs. The ASICs are designed in 130 nm CMOS technology and provide full parallel readout of the DEPFET pixels. The signals is coming from the detector, after having been processed by an analog filter, are immediately digitized by a series of 8-bit single slope ADCs and locally stored in a custom designed memory, also integrated in the ASICs.

2. System Overview

The main board consist of 16 sections of which symmetrically divided into eight in right and eight in left side. For each section comprise of 62 signal, which are divided into 40 DC signal and 22 AC signal. Among all of those 62 signal, we just interest in AC signals because they give more sense in analyzing how signal behave. In these 22 AC signals, some of them are basically differential signals which means the signals is taken between two nodes that have equal and opposite signals with respect to a common mode voltage. Although DC signals is not taking into account of our measurement and testing analysis, they all have a very important rule as a data

logging and comparison between standard and real output value. Moreover the DC signal are connected into 3 digital multi meters of Keithley 2701. The Keithley act as digital multi meter data acquisition and data logging system. The DC signals is very sensitive because of the nedle is not well connected with respect to main board wire. In this case, the 40 DC signals will notice us with some certain LOW parameter. Sometimes we have to lift up and down the needle in order to get the best measurement. Furthermore, because of my time constrain in this summer schools, I don't know about DC signals rule and how they behave in depth sense.

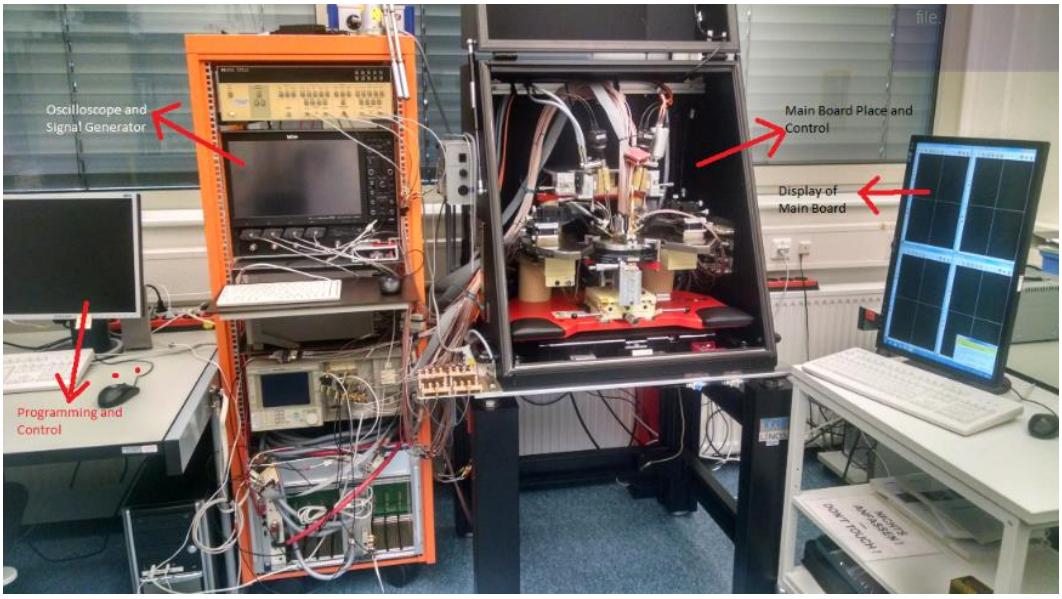


Figure 10: Whole system of measurement

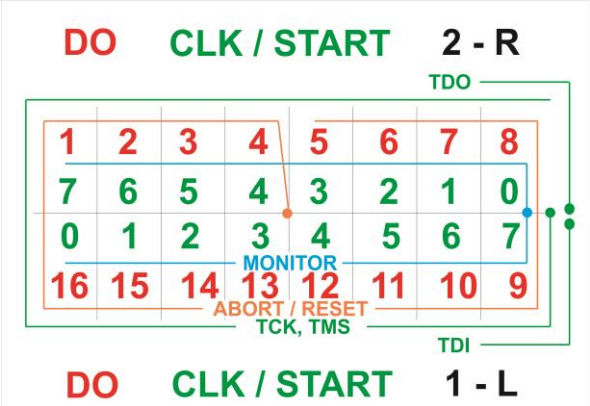


Figure 11: Main board DO, CLK, and START numbering

The overall system of measurement and testing is quite complicated. They have 3 main part which are sophistically connected each other; display for control signal and programing, signal generator and oscilloscope, and main board place and control. Control signal and programming consist of some monitor to control the overall program. All of the hardware used is able to control by graphic programming language named VEE Graphic Programming. We are able to control the whole flow of signal from and into any hardware connected. Basically VEE Graphic Programming is a bit

similar with LabView National Instruments Programming Language. Signal generator and oscilloscope is used for generating signal input and see the out coming output via oscilloscope. In this part is very complicated connection, because we have to deal with so many signals and therefore we use some manual and digital multiplexer to control all of signal flow. Main board place and control is the main things in this measurement. The main board we are going to measure emplace in such a big mechanical construction which are well equipped with some camera, needle, control position, and some flexible mechanical holder. The needle is very sensitive over the main board wire. It has to be well connected with the wire by changing the position. In some case, DC signals is very helpful in order to make sure everything is already well connected. Usually, they will have some different sound of which to differentiate well or bad connection.

I supposed to measure and test all section of main board, but because of some technical problem in main board, I just completed 8 out of 16 sections. In this report I would like to show only one result of measurement, because basically all of those section are similar behaving.

3. Measurement and Testing

Here are some procedure of main board measurement and testing:

1. Place the main board on the main board chamber and hold the main board solidly
2. Turn on power supply, and all hardware
3. Open the program that have already created before, go to the panel view to control some or all of the part hardware
4. Lift up or down the needle to control the position of needle with respect to main board wire. Use some DC signal to make sure weather is has already well connected or not, otherwise keep controlling the needle by looking its position in the display. Usually if some needle and wire goes wrong, there will be a "LOW" notification in control monitor.
5. Select the DO (Data Out) we are going to measure by selecting different selector in manual multiplexer. Once one side is fixed as left, then the other become right side
6. After everything has already well connected, run the AC signal on the panel view one by one, there are 11 AC signal in left side, and 11 AC signal in right side.
7. The oscilloscope should be display the output of certain AC signal, otherwise there is something wrong with the needle connection.
8. Save the data taking wave into ASCII format
9. Plot data and analysis

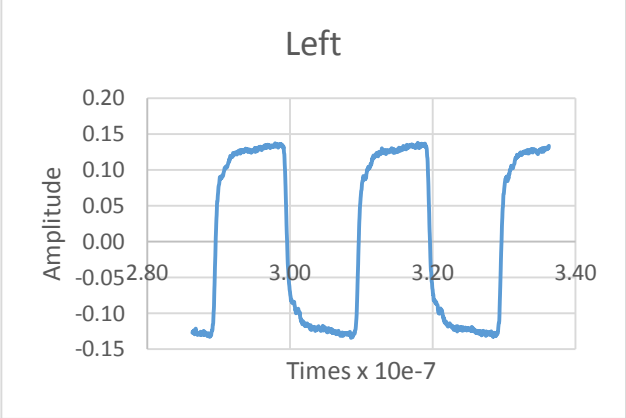
4. Result and Analysis

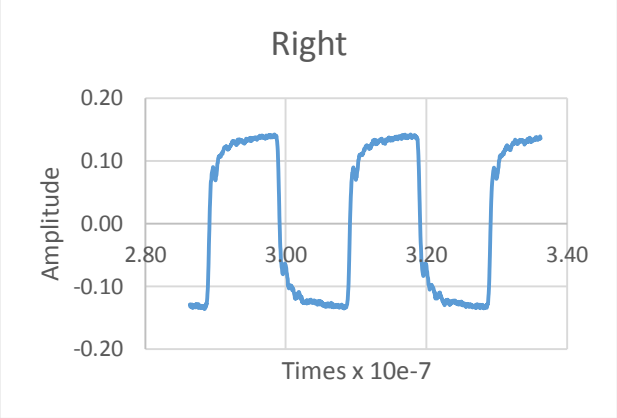
As it is mentioned before, from all of the section taken, in this part I am just going to show and analyze only one section, simply because all of the section should have the same characteristics. But out of them, we need to perform all the measurement in order to ascertain the connection along the main board is going right. The data below was taken from 2 section, which are section 1 and 16. In this case for each section has the similar naming with DO.

The measurement result consist of all the 22 AC signals, in which 11 AC signals goes symmetrically over right and left side. Those 11 signals are; ABORT, CLEAR, CLEAR GATE,

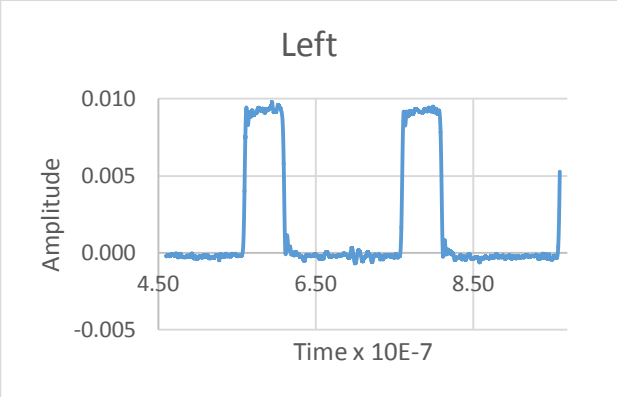
CLK, DO, RESET, START, TCK, TDI, and TMS. The signals TDI and TDO can be measured just only at the place 8-9. Because the needles TDI and TDO are shorted it is not necessary to measure TDO at all places. There are just measurements from 1-16 up to 4-13, therefore TDO is empty, and TDI contains just crosstalk. The parameter of testing and measurement is success or not depend on DC signal and the matching form of output AC signal. While it is compiling, all of DC signal should be in "OK" parameter, otherwise they are not able to give good result.

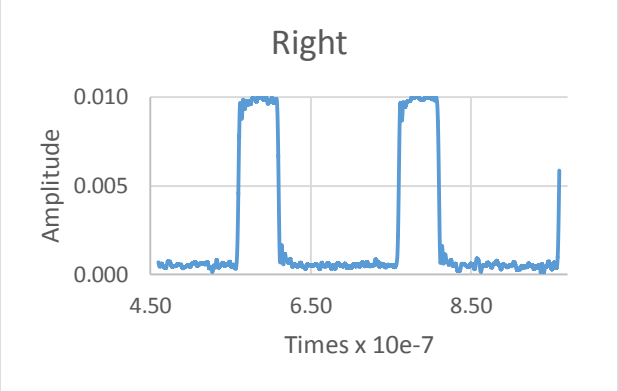
ABORT



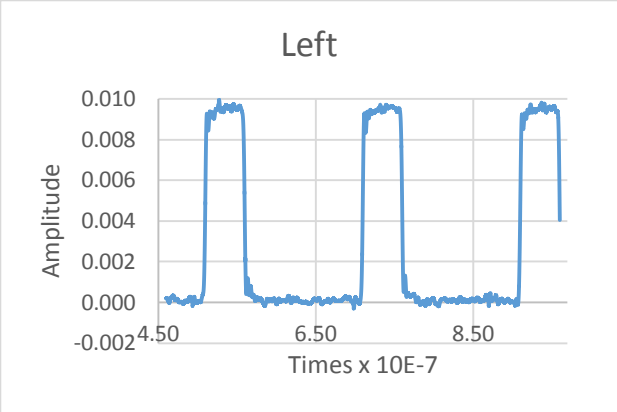


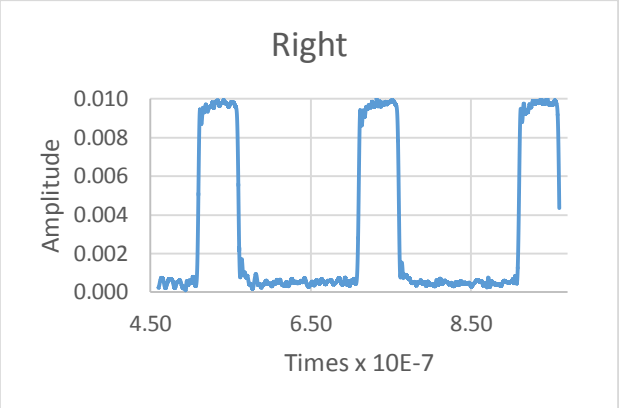
CLEAR



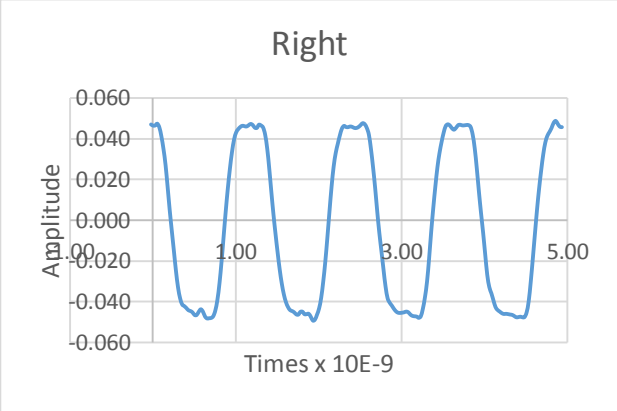


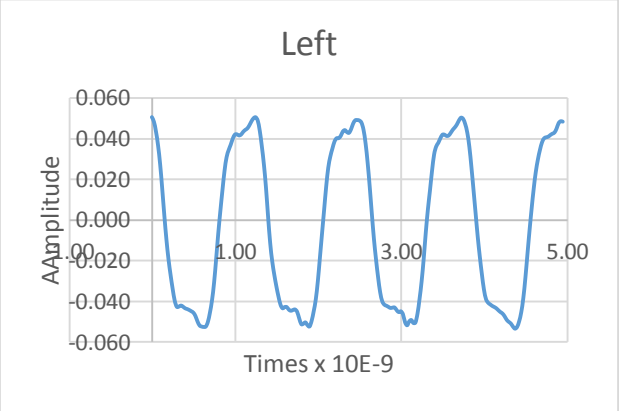
CLEAR GATE


Left
0.010
0.008
0.006
0.004
0.002
0.000
-0.002
Amplitude
4.50
6.50
8.50
Times x 10E-7

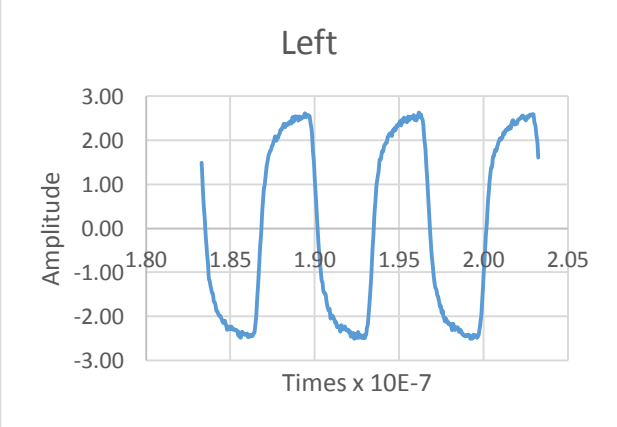

Right
0.010
0.008
0.006
0.004
0.002
0.000
Amplitude
4.50
6.50
8.50
Times x 10E-7

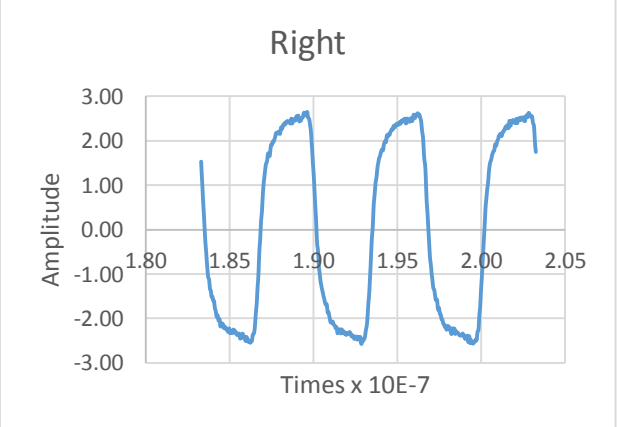
CLK


Right
0.060
0.040
0.020
0.000
-0.020
-0.040
-0.060
Amplitude
1.00
3.00
5.00
Times x 10E-9

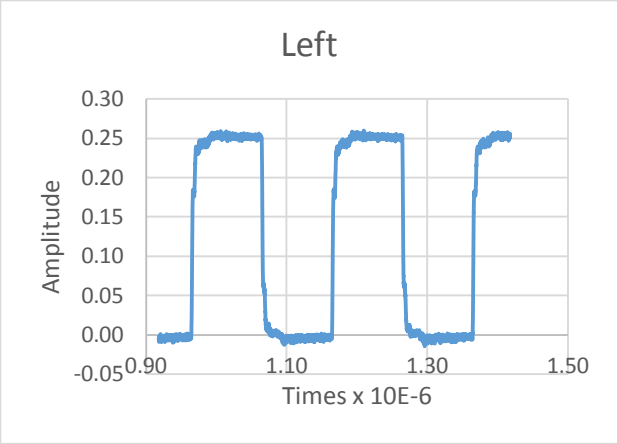

Left
0.060
0.040
0.020
0.000
-0.020
-0.040
-0.060
Amplitude
1.00
3.00
5.00
Times x 10E-9

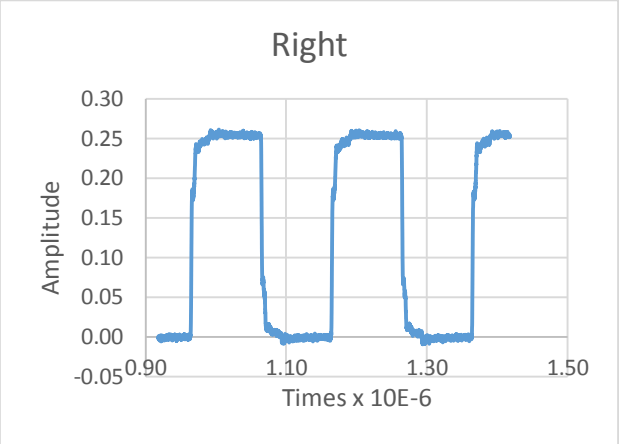
DO


Left
3.00
2.00
1.00
0.00
-1.00
-2.00
-3.00
Amplitude
1.80
1.85
1.90
1.95
2.00
2.05
Times x 10E-7

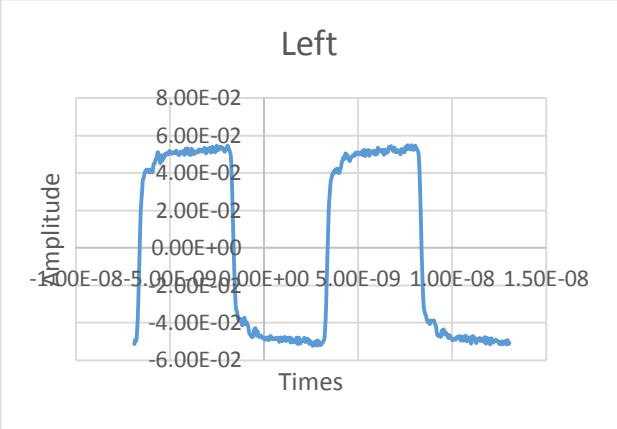

Right
3.00
2.00
1.00
0.00
-1.00
-2.00
-3.00
Amplitude
1.80
1.85
1.90
1.95
2.00
2.05
Times x 10E-7

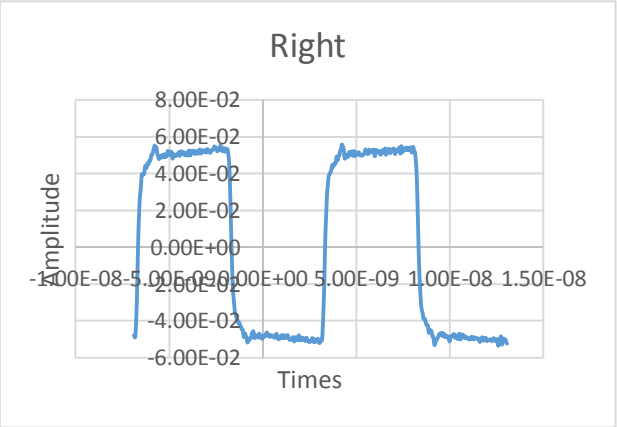
RESET



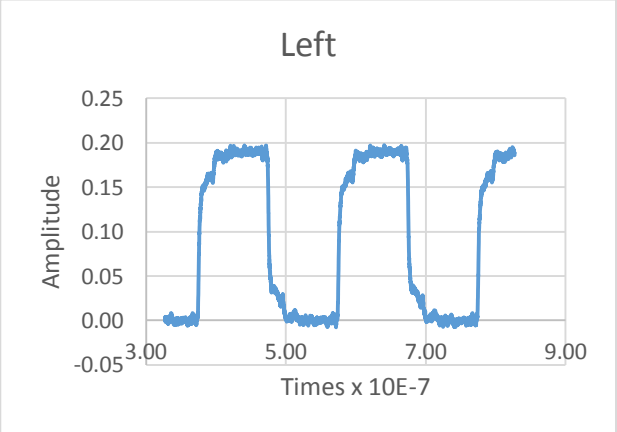


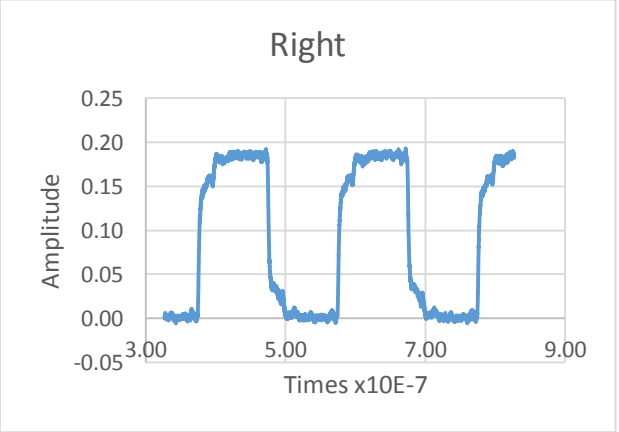
START



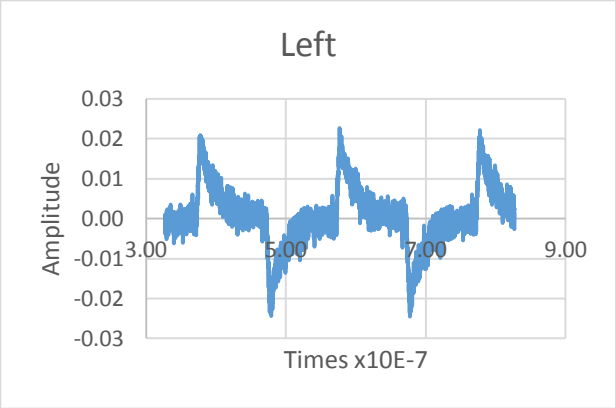


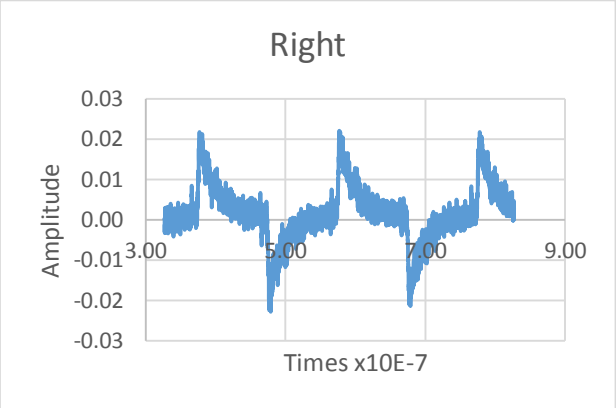
TCK



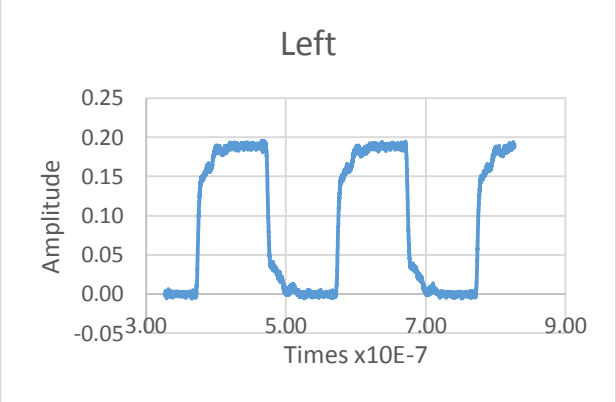


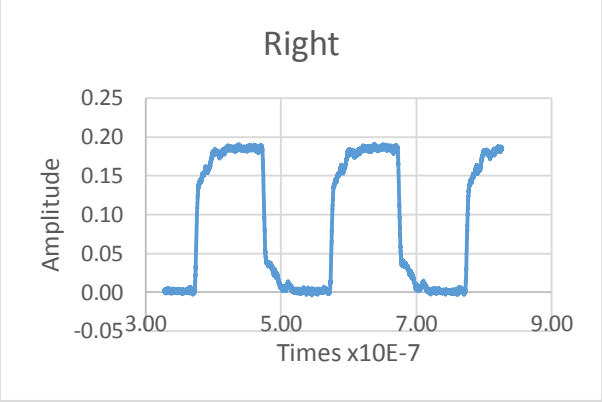
TDI





TMS





5. Conclusion

1. High pulse current source is successfully designed, implemented, and tested. There are two result which has in range of good performance as it mentioned in requirement. Current source that has 0.984 V amplitude, with 100 ns width pulse, 34.27 ns rise time, 3.25 % overshoot, and 6.99 % of undershoot. The other one is current source that has 0.889 V amplitude, with 100 ns width pulse, 34.76 ns rise time, 3.25 % overshoot, and 6.99 % of undershoot.
2. Circuit performance could be increased as a future work so that it could give better result. Some parameter of which need to increase is circuit new layout so that it has no long wire connection in between arbitrary two nodes, because long wire connection could make a noise effect especially under high frequency. Other future work is to find the best mathematical model of its transfer function which really describe the way circuit behave. This mathematical model would really helpful to plot response frequency, since almost impossible to take a lot of data from try-and-error way and plot its response frequency. Hopefully, the response frequency would become a consideration of what is going to happen if the circuit work under higher frequency.
3. There 8 sections out of 16 sections of DSSC main board are successfully tested and measure. All of the output AC signals give good periodic signals which similar between right and left side, because all of the DC parameter give “OK” result when it was compiling.