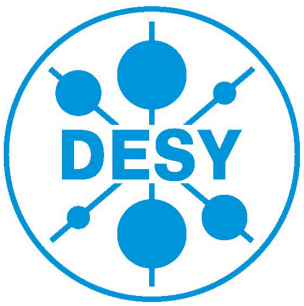

DSSC readout ASIC development for the European XFEL

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Abstract

This report describes my work as summer student at DESY in Hamburg. The main goal of my work was testing a prototype of a readout ASIC for the DSSC detector which is currently being designed for the European XFEL. The next – generation X-ray source, which the European XFEL is, requires two – dimensional integrating detectors with ultra – fast readout. As the DEPFET Sensor with Signal Compression is one of the three detectors dedicated to European XFEL, the FEC Group take a part in the detector development, especially readuot electronic design and performance. In this report the measurements and simulation results of DSSC readout ASIC are presented.

Contents

1 Introduction

The purpose of this report is to present my work in DESY during Summer Student Programme. I was taking a part with FEC Group project which concerned the developing of DEPFET Sensor with Signal Compression. My task was to measure the prototype of a readout ASIC for the DSSC detector and then to perform data analysis. At the same time I also simulated the readout system in order to compare measurements and simulation results.

1.1 European X–ray Free Electron Laser

The European X–ray Free Electron Laser is next–generation photon source which providing laterally coherent X–rays in the range of approximately 250 eV to 25 keV with a peak brilliance of 10^{33} photons/s/mm^2/mrad^2/0.1%BW. This international scientific user facility is under construction in Hamburg and it will start user operation in 2016 [1]. Generation ultrashort X–ray flashes with brilliance which is billion times higher than conventional X–ray radiation sources creates the opportunity for new kinds of research like taking three–dimensional images of the nanoworld or filming chemical reactions [2]. Generated X–ray characteristics are as follows: XFEL generate macro–bunches with a repetition rate of 10 Hz (Figure 1). Every macro–bunch is composed of a train of 2700 pulses with a temporal distance of 220 ns which gives the pulse rate at 4.5 MHz [1, 3].

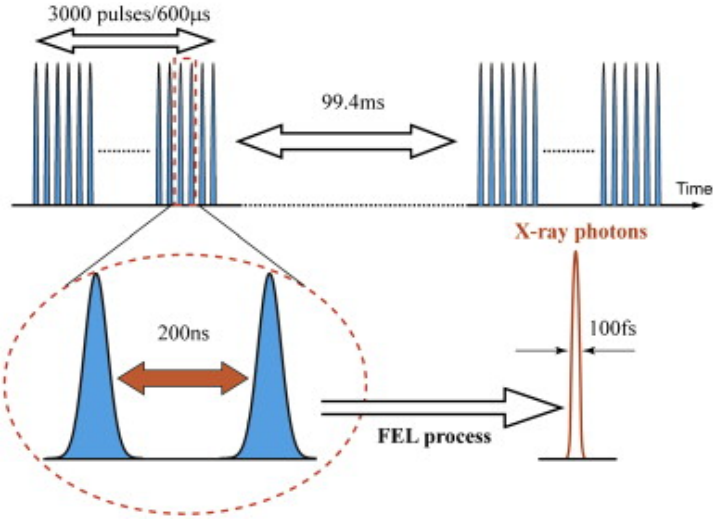


Figure 1: *X–ray bunch structure at the European XFEL [3].*

1.2 Detectors for the European XFEL

The high radiation intensity and short pulse duration of X–ray source is a challenging task for detection system, especially for readout electronics. At the start of the XFEL project no imaging detectors were available for very demanding requirements, and thus it was necessary to develop two–dimensional, ultra–high speed detectors. To make optimal use of the capabilities of the European XFEL facility, three different detector types are performed [1]:

- DEPFET Senesor with Signal Compression (DSSC) for the SQS (Small Quantum Systems) and SCS (Spectroscopy and Coherent Scattering) experiment;
- Adaptive Gain Integrating Pixel Detector (AGIP) for SPB (Diffraction of Single Particles and Biomolecules), MID (Materials Imaging and Dynamics) and HED (High Energy Density Matter);
- Large Pixel Detector (LPD) for FXE (Femtosecond X-ray Experiments).

Additionally two slower and more conventional detectors are beeing developed: a modified pnCCD and an FCCD. It is also worth to mentioning that essential detector parameters are single photon sensitivity and life time dose.

2 Theory

2.1 Detector architecture

DSSC camera is a high speed focal plane detector which will be able to acquire images every 220 ns providing a frame rate of 4.5 MHz and high dynamic range at the same time. The system is based on a pixelated silicon sensor with a DEPFET as a central amplifier structure. The camera is composed of 16 ladders (Figure 2) wherein every ladder comprises 2 monolithic sensors with 128×256 each. Finally the total size of DSSC detector is approximately 21×21 cm^2 composed of 1024×1024 pixels of hexagonal shape. Additionally, in the middle of camera in order to let the unscattered beam go through a hole is left. The concept of DSSC system is based on three key features: the intrinsic low noise provided by the DEPFET sensor device, the signal compression at the sensor level, the full parallel readout with immediate digitization of the signal in the focal plane [3].

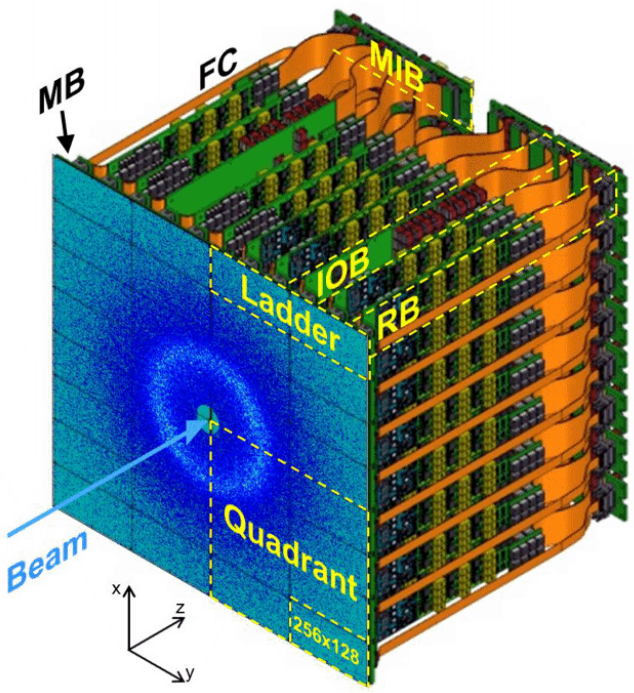
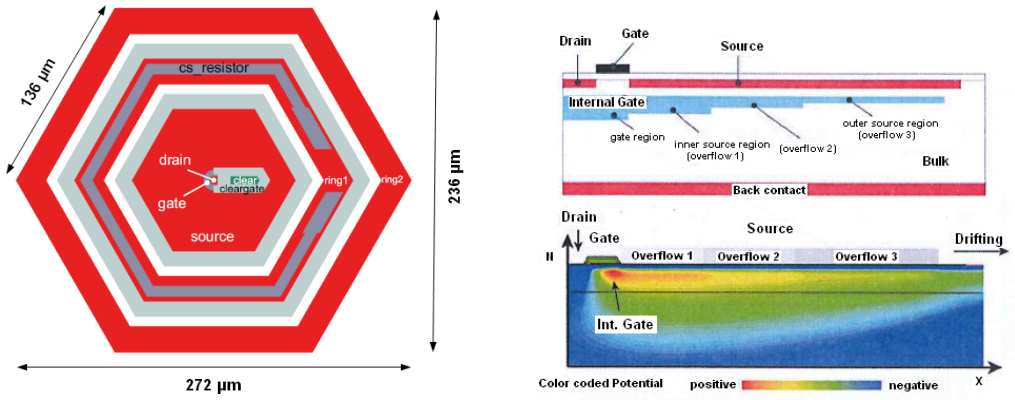


Figure 2: *DSSC pixel X–ray camera [4].*

2.2 Sensor

DSSC pixel has the shape of regular hexagon with side length of 136 μm (Figure 3). The central part of the pixel is filled by the DEPFET which is a Field Effect Transistor located on one surface of a silicon wafer. The DEPFET is enclosed by two drift rings that are biased increasingly negative from the inner to the outer ring. The hexagonal shape of pixel and drift rings was used due to the requirements of fast signal charge collection. What is more, drift rings provide then a more homogeneous drift field with respect to conventional squared pixel. It results higher effectivity in focusing the collected charge into the internal gate of the DEPFET. In order to ensure a high dynamic range which is sensitiveness to single low energy photons at the same time to measure at other positions of the detector signals corresponding to up to 10^4 photons of 1 keV per pixel, a strongly non–linear current–charge characteristic is provided. The sensor operation is as follows: the first signal electrons are collected in the potential well exactly below the gate due to its most positive potential (Figure 3). If that area is filled up with electrons the next disk collects electrons and so fort. As a result, only the fraction of the additional charge that arrives below the internal gate is effective in modulating the transistor current [3].



(a) *Geometry and simplified layout of a DSSC pixel [5].*

(b) *DSSC DEPFET concept provides non–liniear characteristic [3].*

Figure 3: *DSSC DEPFET sensor.*

2.3 Readout ASIC

Each sensor with 128 × 256 pixels is bump bonded to 8 readout ASICs (*Application Specific Integrated Circuit*) which means that each ASIC is a chip with 64 × 64 channels suited for the low noise readout and digitization of the DEPFET current signals and total number of ASICs used in DSSC system is 256. In the Figure 4 is shown simplified diagram of one pixel of 206 × 236 μm^2 [3].

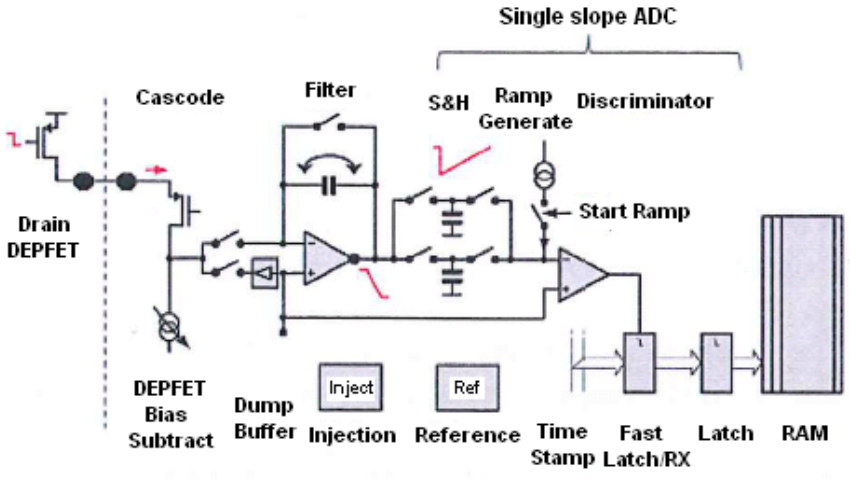


Figure 4: *Simplified diagram of one pixel of the DSSC pixel ASIC [3].*

Main blocks of ASIC pixel are described below [3]:

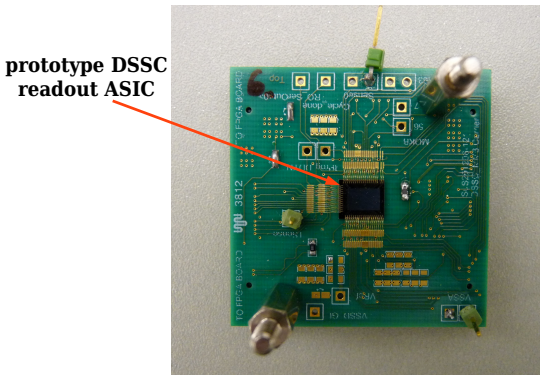
- A **cascode** to keep DEPFET drain at constant potential;
- A circuit for the **DEPFET bias current cancellation**, which is fixed by the DEPFET Gate–Source voltage and which can vary from pixel to pixel;
- A **filter stage implementing a trapezoidal shaping** with variable gain;
- An **injection circuit** which pulses known programmable current into the input node;
- A **Wilkinson type (single slope) ADC** with 8 bit resolution. This type of ADC is based on time to digital conversion: when the S&H capacitor is charged with a constant current source the GCC (*Gray Coded Counter*) starts counting. Once the reference potential is reached , a comparator latches 8 gray coded time stamps. A fast 800 MHz external clock is used to toggle the counter on both edges, giving a time resolution of 625 ps;
- A temperature and supply voltage insensitive **bandgap reference** in order to bias the circuit;
- A large **SRAM** to store at least 640 words of 9–bit during the X–ray macro–bunch;
- Further **auxiliary blocks**, like static control registers or monitoring lines.

3 Results

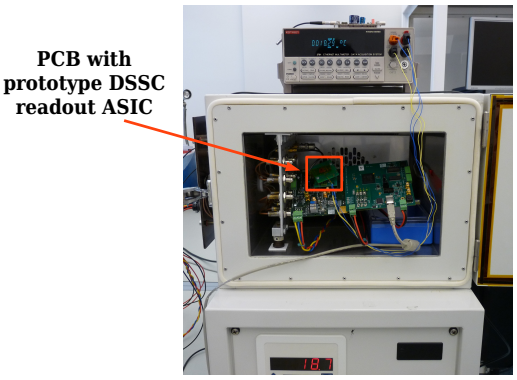
3.1 Setup

In order to check a temperature behaviour of prototype DSSC readout ASIC which was matrix composed of 8 $\times$ 16 pixels, all measurements were performed using oven (Figure 5). Inside oven the PCB board which hosts ASIC prototype was closed. The temperature range during the tests was from -40 °C to 40 °C. The ramp current[1] settings also have been changing by I_{rmp} DAC (0–7 a.u.). Parameters like *Gain*, which is responsible for gain of amplifier was equal 1 and *CurrentDouble* parameter was at 1 too.

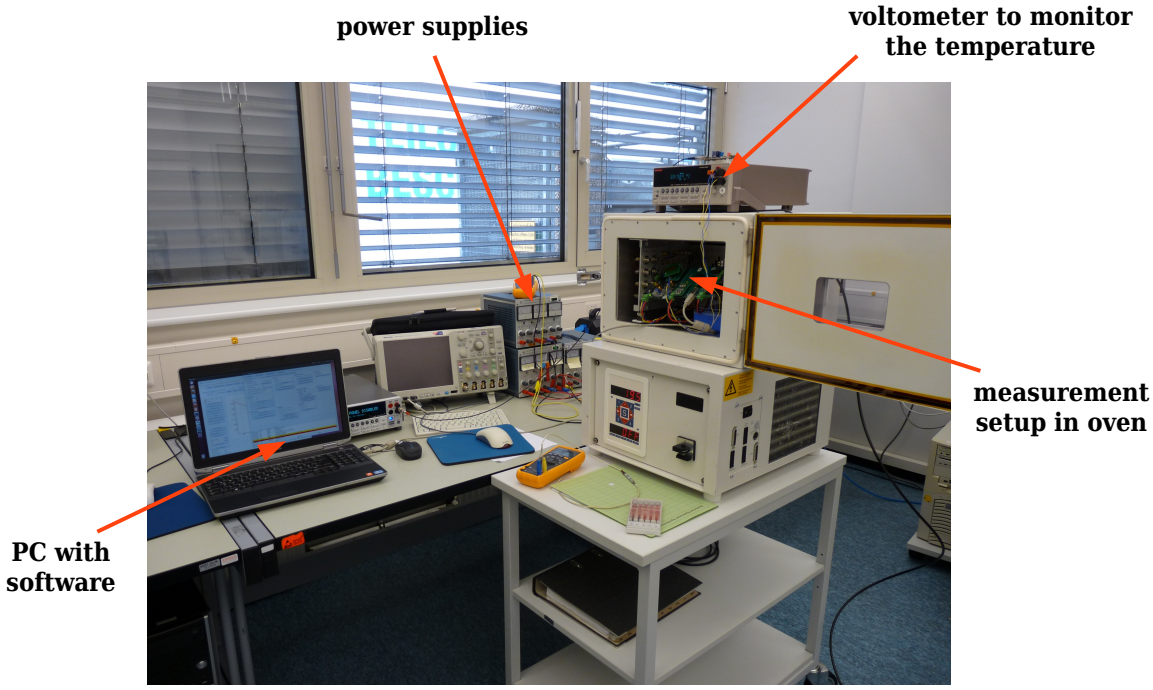
[1]Current charging C_{SH} capacitor.



(a) *PCB with prototype readout ASIC.*



(b) *Measurement setup in the oven.*



(c) *Measurement setup to perform temperature tests using oven.*

Figure 5: *Measurement setup which was used during temperature measurements.*

3.2 Circuit model application

The measurements of ASIC were performed for one pixel of readout matrix with using dc voltage source. Input voltage V_{in} varied between 0.2 V to 0.6 V with a step size 10 mV. For each voltage step one hundred ADC samples were taken and then they were used to calculate mean and standard deviation (RMS) of the histogram. The ADC characteristics were taken for eight values of $I_{r,set}$ and seventeen different temperatures in range from -40 °C to 40 °C. The frequency of GCC was f_{CLK} = 700 MHz and the states of GCC were changed on both edges of clock cycle. In the Figure 6 the results of measurements for three temperatures (-40 °C, 0 °C, 40 °C) are presented.

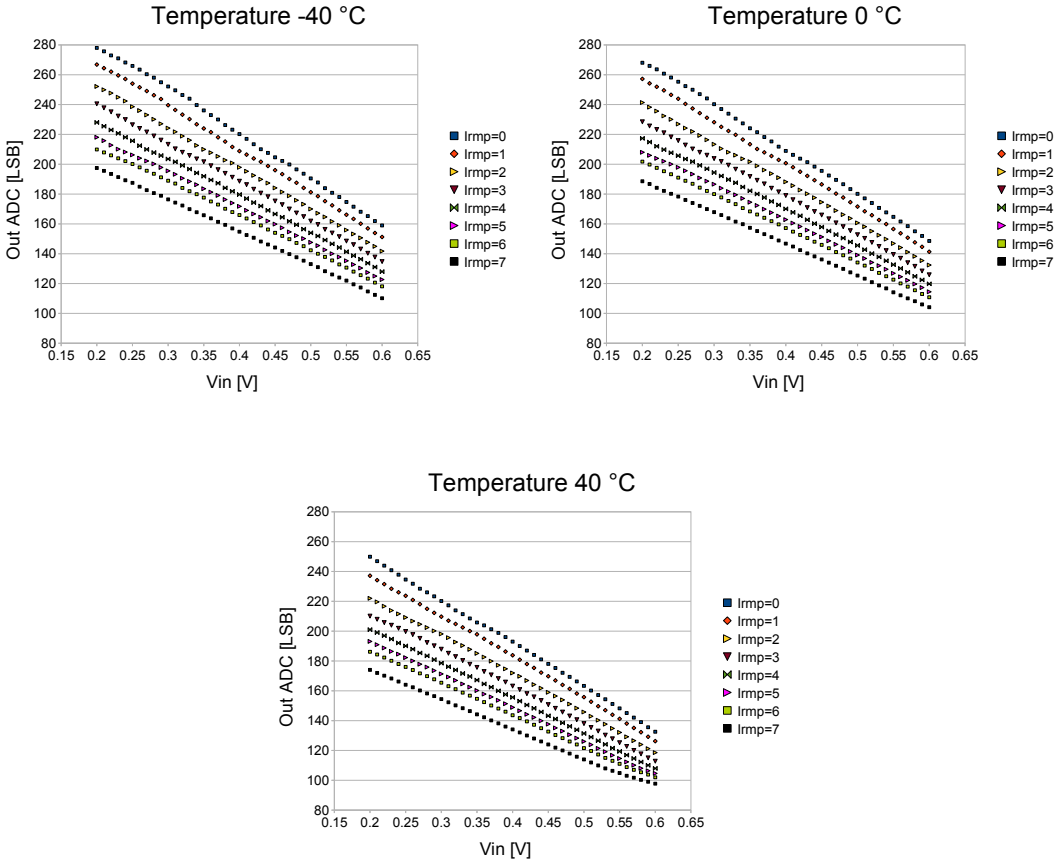


Figure 6: *Measured ADC output for input voltage range 0.2 V to 0.6 V, eight values of ramp current I_{rmp} (0–7 a.u.) and the following temperatures: -40 °C, 40 °C (two extreme temperatures) and 0 °C (temperature in the middle of the range).*

Mathematical model of circuit which describes behaviour of readout channel based on Wilkinson type ADC according to the applied voltage, is given by the linear equation:

$$Out = (V_0 - V_{in}) \cdot (S_0 - \Delta S \cdot I_{r,set}) + t_{delay} \tag{1}$$

In order to evaluate parameters like V_0, S_0, ΔS and t_{delay} the following data analysis was performed. Each output characteristic was fitted by a linear function to calculate *Slope* and *Intercept* parameters. Next, the fitting parameters were plotted as a function of temperature for each I_{rmp} value which gives eight curves (Figure 7).

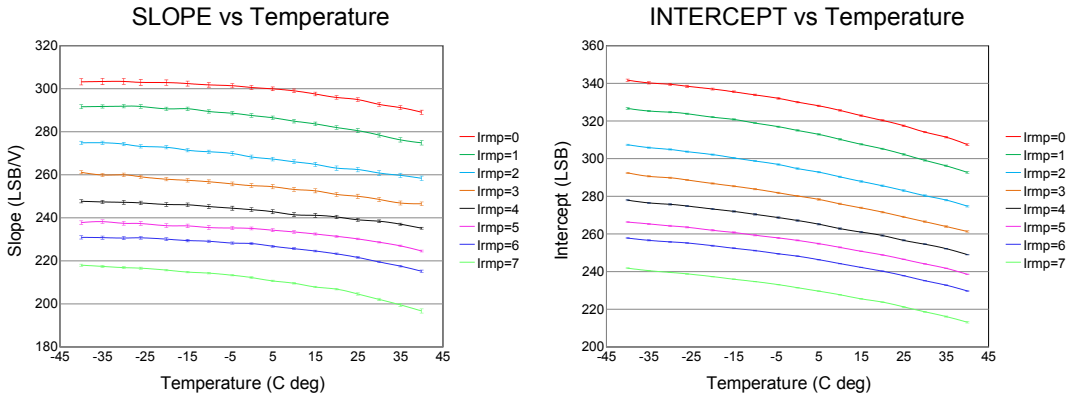


Figure 7: *Measured Slope and Intercept characteristics as a function of temperature for different I_{rmp} settings.*

Additionally, in the plots the *standard error* bars were added. Taking into account linearity of the ADC output characteristic, the *standard error* (s.e.) is an *estimate* of the *standard deviation* of *Slope* and *Intercept* parameters [6]:

$$s.e.(Slope) = RMS \cdot \sqrt{\frac{1}{n} + \frac{\bar{V_{in}}^2}{\sum_j (V_{inj} - \bar{V_{in}})^2}} \tag{2}$$

$$s.e.(Intercept) = \frac{RMS}{\sqrt{\sum_j (V_{inj} - \bar{V_{in}})^2}} \tag{3}$$

where $\bar{V_{in}}$ is mean value of input voltage. With increasing temperature the decreasing behaviour for *Slope* and *Intercept* characteristics is observed.
Plotting *Intercept* as a function of *Slope* we also get a linear behaviour which can be

expressed by the formula:

$$Intercept = V_0 \cdot Slope + B \tag{4}$$

In the Figure 8 V_0 dependence on temperature is depicted and a parabolic function was fitted to the data points. Previously mentioned S_0 and ΔS parameters can be calculated by using graph in Figure 8, because linear fitting function is given by the equation:

$$Slope = S_0 - \Delta S \cdot I_{rmp} \tag{5}$$

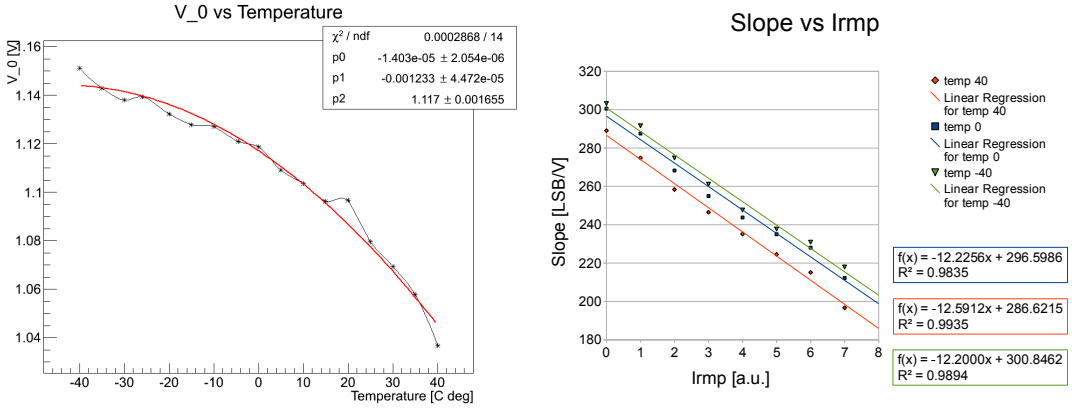


Figure 8: *Left: temperature dependence of V_0 with fitted parabolic function. Right: Slope characteristic as a function of I_{rmp} current for three values of temperature: -40 °C, 0 °C and 40 °C.*

Finally, the t_{delay} value was calculated as mean value for all data points at a given temperature and it can be expressed by:

$$t_{delay}(Temp) = (V_0(Temp) - V_{in}) \cdot (S_0(Temp) - \Delta S(Temp) \cdot I_{rmp}) - Out_{measured}(V_{in}, I_{rmp}, Temp) \tag{6}$$

In the Table 1 are circuit model parameters extracted using measurement data and in the Figure 9 the comparison of mathematical model and measurement results is shown. The measured values correspond well to the model characteristics. The deviation between both characteristics does not exceed ± 5.5 LSB.

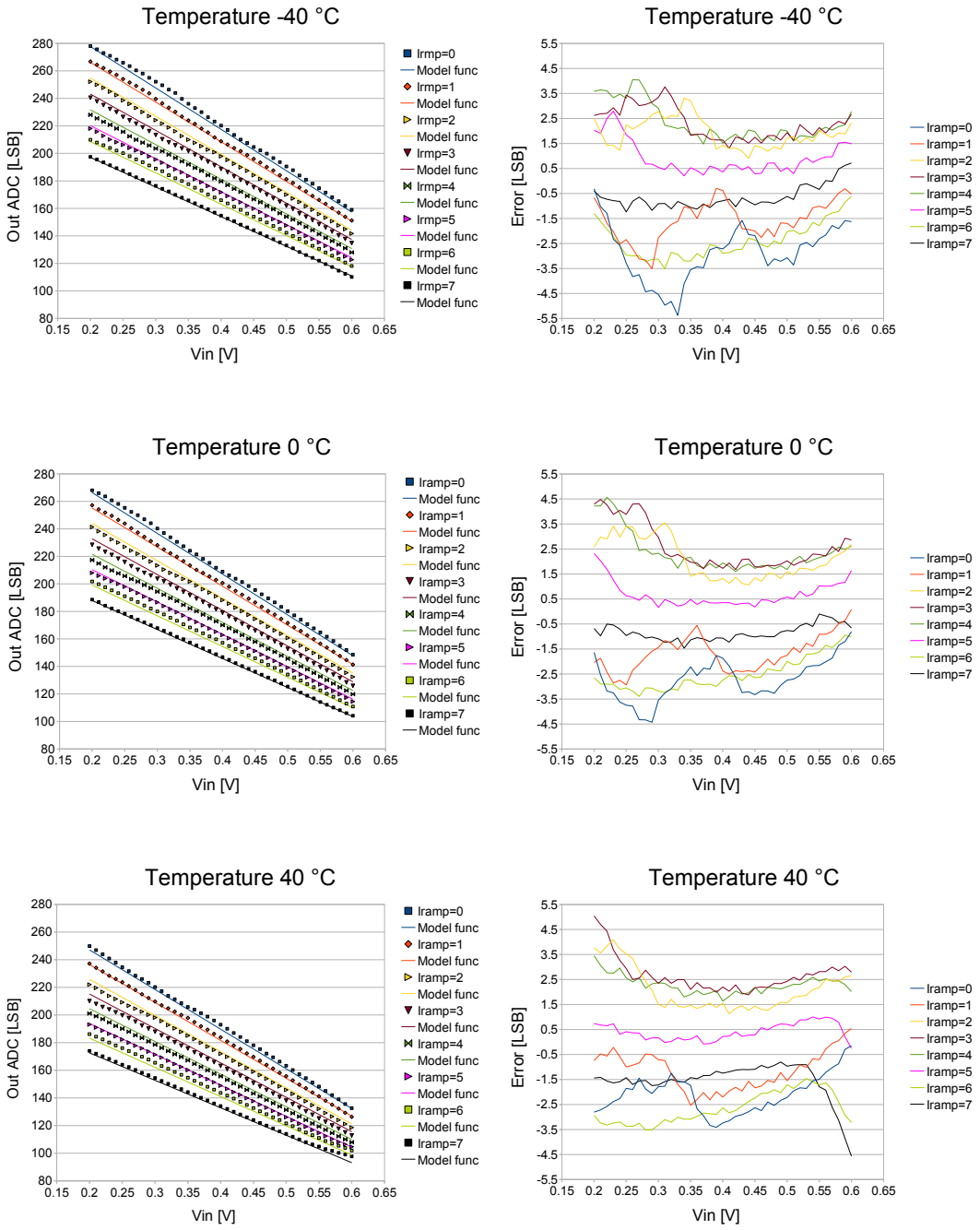


Figure 9: *Measured characteristics and circuit model comparison (left) for f_{CLK}=700 MHz and deviation between both characteristic (right).*

Table 1: *Circuit model parameters.*

Parameter\Temperature	-40 °C	0 °C	40 °C
$V_0[V]$	1.144	1.117	1.045
$S_0[LSB/V]$	300.846	296.597	286.623
$\Delta S[LSB/(V \cdot I_{rmp})]$	12.200	12.226	12.591
$t_{delay}[LSB]$	-6.286	-5.597	4.806

3.3 Simulation results

The purpose of the simulations was finding optimal setup parameters like I_{rmp} or C_{SH} values which make it working as it was measured. All simulations were performed with *Cadence* environment and the simulation cell with readout channel is shown in Figure 10.

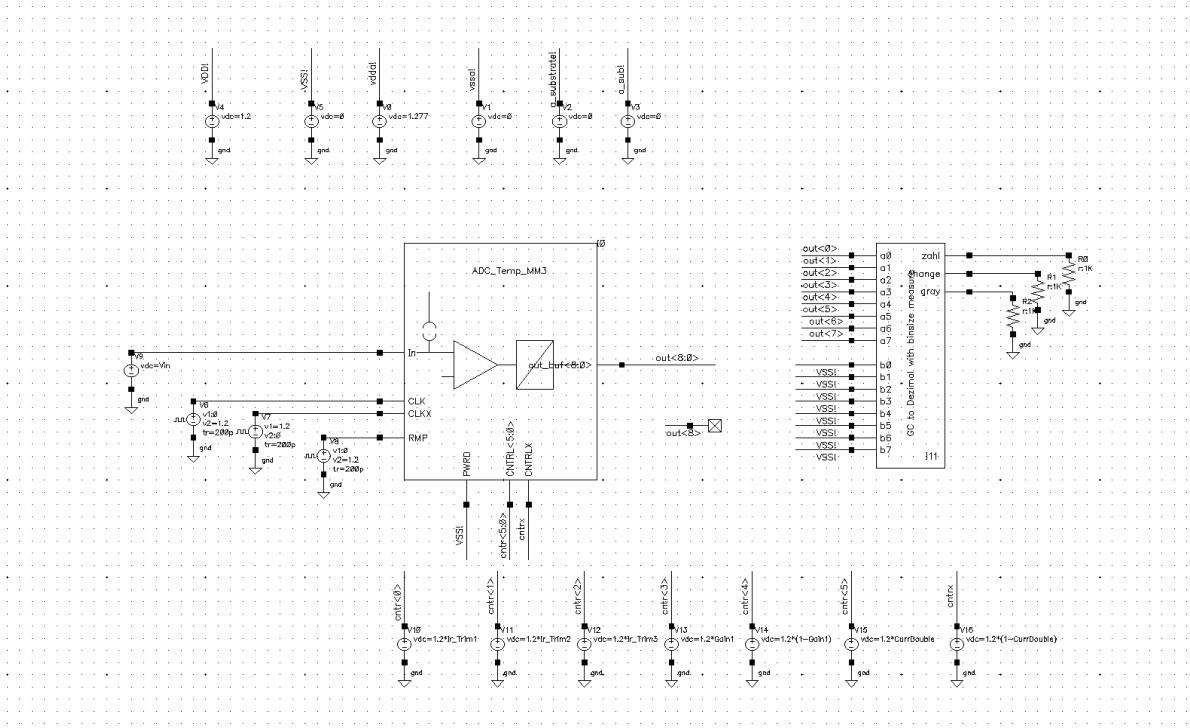


Figure 10: *Simulation schematic which was used to simulate readout channel behaviour.*

Explanation of decreasing *Slope* and *Intercept* behaviour with temperature increase was the main goal of simulations, therefore the first stage of simulations was to check output ADC with the similar working condition as during the measurements ($Gain = 1$, $CurrentDouble = 1$, $I_{rmp} = 0$ a.u., temperature: from -40 °C to 40 °C and V_{in}: from 0.25 V to 1 V). The *UltraSim* parametric analysis was used to simulation described above. Parameter which can be easily translated to the *Slope* behaviour is ramp current:

$$I_{rmp} = \frac{2 \cdot f_{CLK} \cdot C_{SH}}{Slope} \tag{7}$$

Simulation results are depicted in Figure 11 where is also shown *id* transistor current obtained through simulation for one input voltage value $V_{in} = 0.25$ V. This transistor current should correspond to the I_{rmp} which was calculated using Formula (7). The difference between both characteristics is about 60 nA.

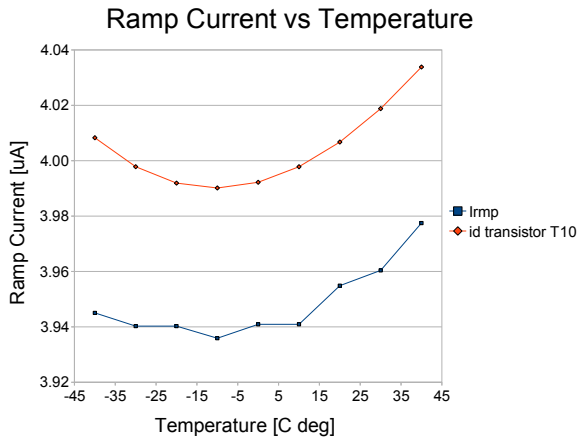


Figure 11: *Simulation results for $I_{rmp} = 0$ a.u. for parametric analysis with input voltage in range from 0.25 V to 1 V and different temperatures (blue curve) and parametric analysis of id transistor current for input voltage 0.25 V and different temperatures (red curve).*

As mentioned, the shape of *Slope* characteristic is decreasing with increase of temperature and has its maximum at about -40 °C (Figure 7). For that reason the minimum of ramp current should be visible for the same temperature value. Three types of simulations for different *Model Setup* were performed to find ramp current characteristic which corresponds to measured data. For *ssf model* (Figure 12) the minimum current value for -30 °C is observed and it best corresponds to measured characteristics. Finally, the

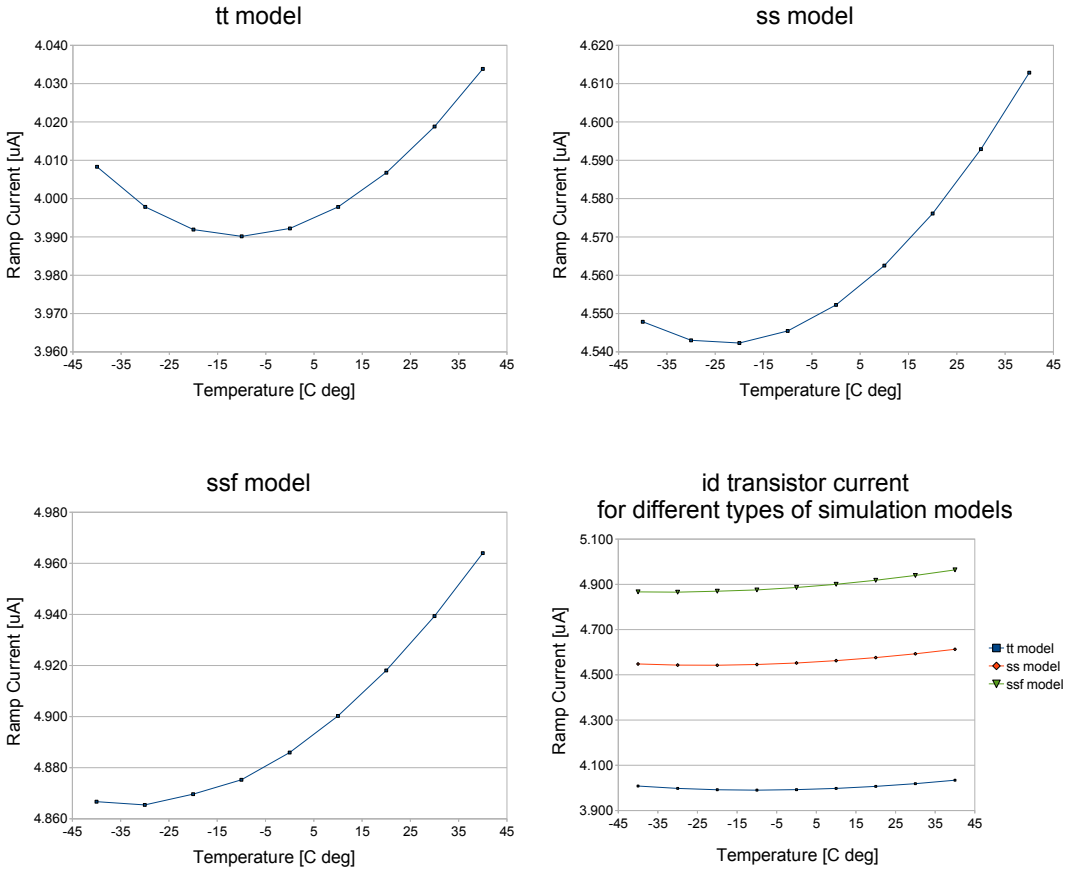


Figure 12: *Parametric simulation for three types of Model Setup with input voltage V_{in}= 0.25 V and temperatures in range from -40 °C to 40 °C.*

I_{rmp} current value can be calculated using measurement data and then obtained curve for $I_{rmp} = 0$ a.u. can be compared to simulated characteristic. As is shown in Figure 13 both curves (measured and simulated using *ssf model*) have the similar shape but they are shifted relative to each other by about 465 nA for minimum value points.Taking into account spread of C_SH value caused by technological process (which may be different of 10 % from the values used in the simulation) it is possible to tune C_{SH} value to fit measured curve to simulated characteristic. As a result the tuned value is about 10.63 % higher than simulated value and it is equal 1062 fF. In the Figure 13 the simulated and measured curve are shown, wherein the C_{SH} value to calculate measured characteristic was set so that both the measured and simulated minimum value were the same.

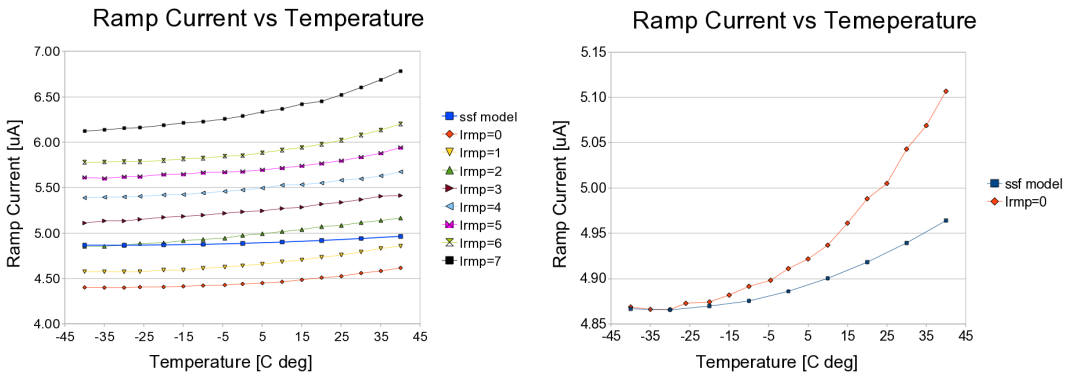


Figure 13: *Left: Comparison of calculated ramp current values for different settings of I_{rmp} parameter during measurements and simulated ramp current value. Right: Simulated (blue curve) and measured (red curve) characteristics of ramp current for C_{SH} value 960 fF and 1062 fF respectively.*

3.4 Noise measurements

RMS value (*root mean square*) gives an information about noise of measurement setup. The information about noise level was extracted from two types of measurements[2]:

- Measurements with temperature diode at the input of readout channel what means that for a give temperature the input voltage is set. For each temperature the ADC output was probed 500 times and then the mean RMS value was calculated. In Figure 15 and Figure 16 the results are shown.

- Measurements with dc voltage source at the input of readout channel. Input voltage V_{in} can be sweeped independently of the temperature. The ADC output was probed 100 times per each input voltage which gives 4100 samples in given temperature. Finally, the mean RMS value for each temperature and I_{rmp} settings was calculated. In Figure 17 and Figure 18 the results are shown.

The noise level is lower for measurements with temperature diode. This effect is caused by additional noise produced by voltage source at the input of readout channel. It is worth noting that in the second type of measurements, the fluctuations of curves are

[2]Only second type of measurements was performed by an Author

smaller. Fluctuations in first case depends not only on noise level but also on mean output ADC value (Figure 14). When mean output value is close to the center of bin the RMS takes the lowest value, whereas when the mean output value is between two bins, the RMS value is about 0.5 LSB. Maximal RMS value is visible when ADC output includes more than 3 bins.

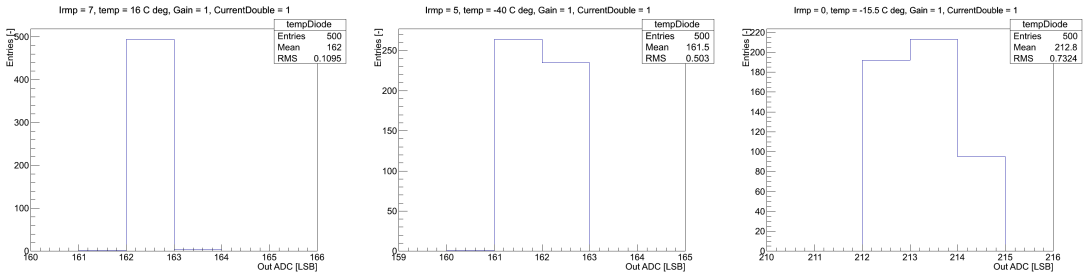


Figure 14: *Three different types of output ADC value distribution for measurements with dc voltage source.*

RMS characteristics should be inversely proportional to the ramp current value:

$$RMS \sim \frac{1}{I_{rmp}} \tag{8}$$

It can be simply check by plotting *Slope* dependence of RMS values and fitting a linear function. According to Formula 7 RMS characteristic is proportional to *Slope*. Results are depicted in Figure 19. To the data points the linear function was fitted:

$$RMS = \alpha \cdot Slope + \beta \tag{9}$$

In Table 2 obtained parameters are presented. The fit quality parameter R^2 is higher than 0.9 in most cases what confirm linear *Slope* dependence of RMS. Ultimately, the measured RMS value can be compared to simulated noise level which is about 370 μV. As the 1 LSB range is 3.125 mV, the simulated noise value corresponds to 0,118 LSB. This value is similar to measured point for temperature diode at the input (Figure 15) in temperature 16.5 °C and $I_{rmp} = 7$ a.u.

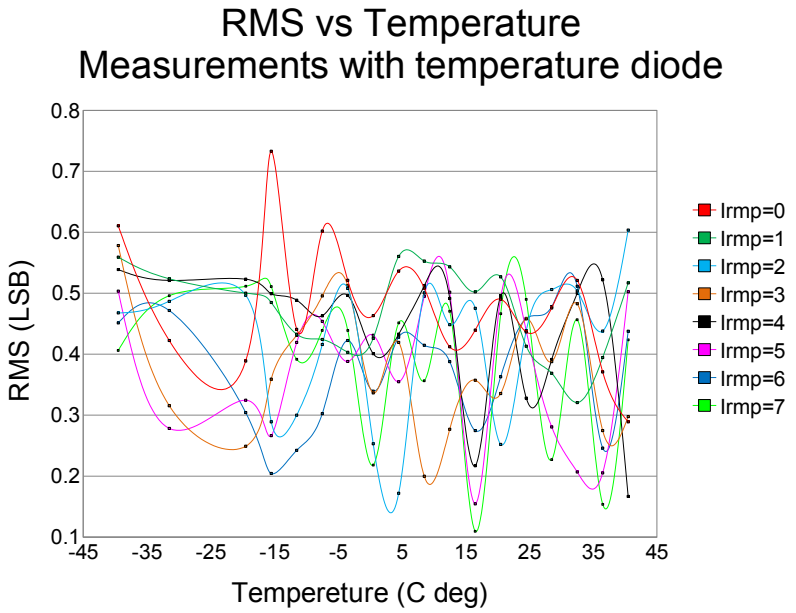


Figure 15: *RMS as a function of temperature for measurements with temperature diode at the input.*

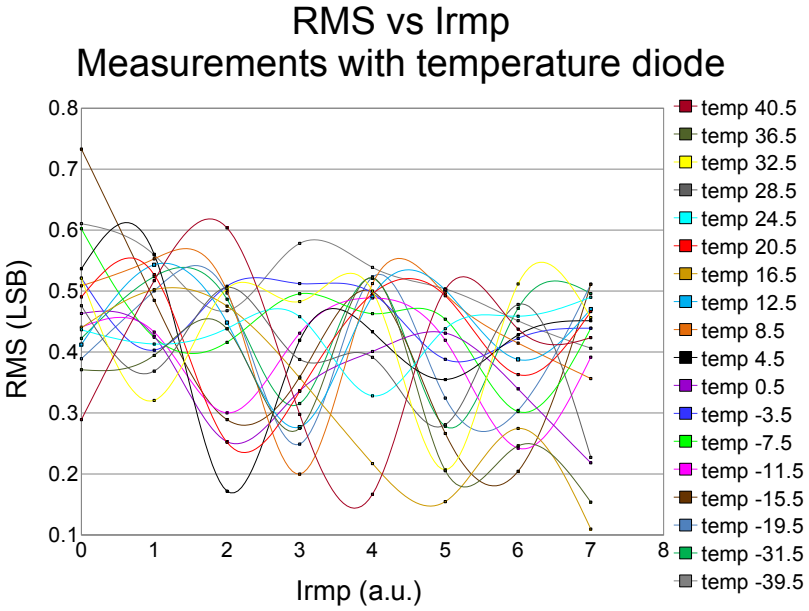


Figure 16: *RMS as a function of I_{rmp} settings for measurements with temperature diode at the input.*

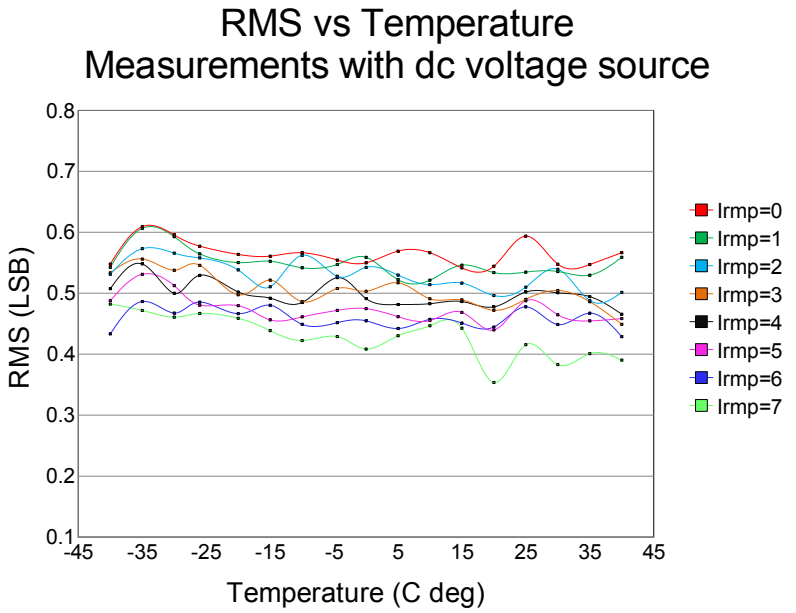


Figure 17: *RMS as a function of temperature for measurements with dc voltage source at the input.*

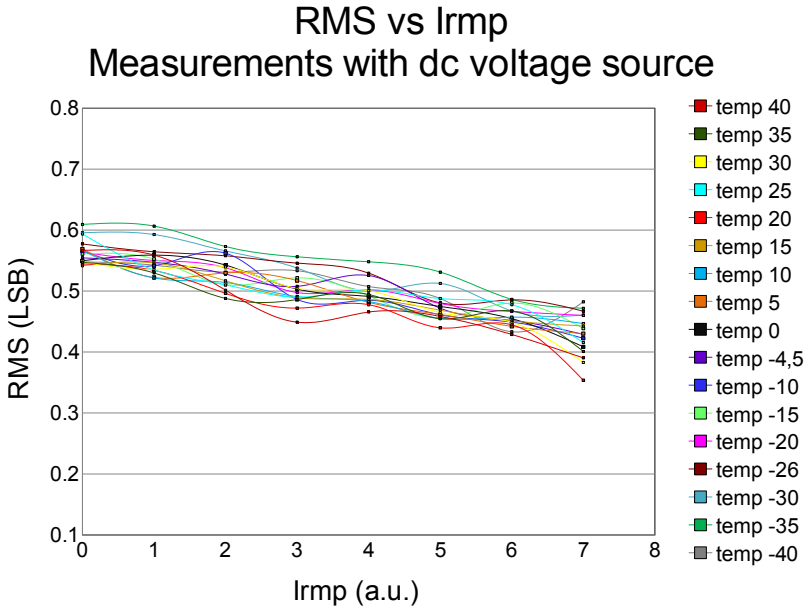


Figure 18: *RMS as a function of I_{rmp} settings for measurements with dc voltage source at the input.*

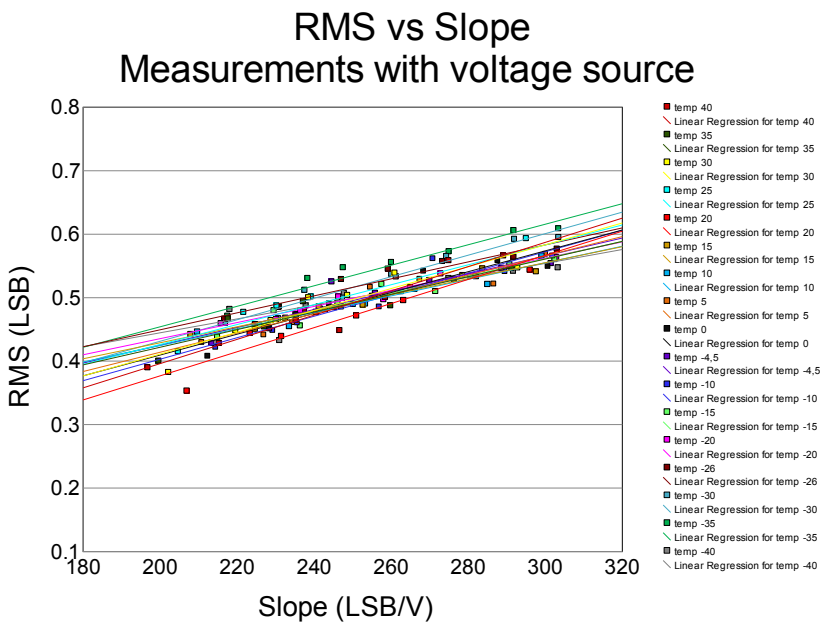


Figure 19: *RMS as a function of slope with linear regression lines.*

Table 2: *Fitting parameters for RMS characteristic as a function of Slope.*

Temperature\Fitting Parameter	α	β	R^2
40 °C	0.0019	0.0140	0.9249
35 °C	0.0014	0.1440	0.8863
30 °C	0.0017	0.0671	0.8688
25 °C	0.0016	0.1129	0.8827
20 °C	0.0019	0.0030	0.8947
15 °C	0.0013	0.1766	0.9439
10 °C	0.0013	0.1640	0.9439
5 °C	0.0015	0.1103	0.9178
0 °C	0.0016	0.0816	0.9102
-4.5 °C	0.0014	0.1436	0.8615
-10 °C	0.0017	0.0642	0.9010
-15 °C	0.0014	0.1534	0.9143
-20 °C	0.0013	0.1799	0.9656
-26 °C	0.0013	0.1799	0.9007
-30 °C	0.0017	0.0923	0.9520
-35 °C	0.0016	0.1310	0.9361
-40 °C	0.0011	0.2261	0.7098

4 Conclusions

Performing of DSSC readout ASIC for European XFEL consisted of two parts: measurements and simulation. My task during Summer Student Program was to measure temperature behaviour of prototype readout matrix and then extract the parameters which were used in circuit model application. The mathematical ADC model corresponds well to measured output. At the same time I calculated the noise level using RMS value for two types of measurement setup: with temperature diode and with dc voltage source at the input. The last part was simulation of ADC and whole readout channel in order to define ASIC working conditions. The main purpose was to find parameters responsible for *Slope* and *Intercept* behaviour as a function of temperature like ramp current and capacitance of C_{SH}. I performed simulations for different types of *Model Setup* to find temperature dependence of ramp current which is similar to measured data and I also checked the possible capacitance of C_{SH} on ASIC which may be different because of process variations.

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