

Radiation hardness of test structures fabricated by Canberra as X-ray Silicon Detectors

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ABSTRACT: The European X-ray Free Electron Laser (XFEL) will deliver 27,000 fully coherent, high brilliance X-ray pulses per second each with a duration below 100 fs. This will allow the recording of diffraction patterns of single complex molecules and the study of ultra-fast processes. Silicon pixel sensors will be used to record the diffraction images. In 3 years of operation the sensors will be exposed to doses of up to 1 GGy of 12 keV X-rays. At this X-ray energy no bulk damage in silicon is expected. However fixed oxide charges in the insulating layer covering the silicon and interface traps at the Si-SiO₂ interface will be introduced by the irradiation and build up over time.

We have investigated the microscopic defects in test structures fabricated by Canberra as a function of the X-ray dose. From the test structures we determine the oxide charge density and the densities of interface traps as a function of dose. We find that both reach maximum values at doses of ~ 10 MGy and then decrease above that dose.

KEYWORDS: Test structure; X-ray radiation damage; oxide charge density; surface current density; interface trap density.

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1. Introduction

Imaging experiments at the European X-ray Free Electron Laser (XFEL), planned to be operational in 2015, require silicon pixel sensors with extraordinary performance specifications: a dynamic range from 0,1 to 10^5 of 12 keV photons deposited in less than 100 fs in one pixel of $200\mu\text{m} \times 200\mu\text{m}$, a time interval between XFEL pulses of 220 ns, and radiation doses up to 1 GGy for 3 years of operation. To optimize the sensor performance for these requirements, especially for radiation tolerance, demands an excellent understanding of the radiation damage caused by X-rays and its effects on segmented sensors.

The maximum energy transfer to silicon atoms from 12 keV X-rays is 0.011 eV, which is far below the threshold energy of 21 eV for bulk damage [1] and therefore no bulk damage is expected. X-rays produce electron-hole pairs in the insulating layer (typically SiO_2). Some of these charge carriers produced by the 12 keV X-rays recombine, whereas those remaining either remain in the insulating layer or move to the electrode on top of the insulating layer or drift to the Si- SiO_2 interface. Once holes come close to the Si- SiO_2 interface a fraction of them will be trapped in the oxide close to the interface and produce radiation-induced fixed oxide charges. In

addition, border traps [2] and interface traps are produced: the former are located in the oxide near the Si-SiO₂ interface and can be charged up or discharged through capture and emission of electrons and/or holes; whereas the latter are at the Si-SiO₂ interface and have energy levels distributed throughout the silicon band gap and whose occupation therefore changes with band bending. They are responsible for the surface generation current. The densities of fixed oxide charges and interface traps introduced by X-rays mainly depend on the dose (energy deposition in the insulating layer), dose rate, electric field during irradiation, and post-irradiation conditions (e.g. time and temperature of annealing).

In this report, the analysis of the surface damage caused by X-rays on test structures produced by Canberra is described. The test structures were irradiated in steps up to doses of 100 MGy, in order to study the dose dependence of the oxide charge density and interface trap density, as well as of the surface current density. The performed analysis is similar and complementary to that already performed on similar structures fabricated by CiS and Hamamatsu [5].

2. The test structures from Canberra

In the context of the X-ray induced surface damage study on silicon sensors ongoing at Hamburg University, some tests structures were commissioned to Canberra. The structures were fabricated on 300 μm thick n-doped <111> substrates with a doping concentration of about $7.0 \times 10^{11} \text{ cm}^{-3}$. The insulator is made of 250 nm SiO₂. The test structures, delivered to Hamburg in June 2012, consist of MOS capacitors and gate-controlled diodes. With respect to the previous tests structures commissioned to CiS and Hamamatsu, a square gate-controlled diode is included in addition to the circular one. This allows dedicated measurements that will be detailed in the following.

These test structures are meant to measure the surface parameters of individual wafers which can not be measured on the main devices, but which can be correlated with their performance. They are therefore an essential input for the device simulations. Furthermore, the monitoring of the same fabrication-dependent parameters during the production phase allows the identification of possible processing problems before detectors are built into modules. Systematic studies of ionization-induced radiation damage including the process-dependent parameters and the electric field conditions during irradiation can be performed.

The test structures are shown in Fig. 1 and consist of one circular MOS structure and two gate-controlled diodes (circular and square). The advantage of this redundancy is to have either always an identical reference sample or to have the possibility to irradiate two identical samples under different electrical boundary conditions. The new square gate-controlled diode is formed by a $7.1 \times 10^{-3} \text{ cm}^2$ square diode consisting of six strips. The width of the gate is 100 μm , the length of the 6 parallel gates is 1000 μm , and the length of the lateral gate which connects all other 6 gates is 1100 μm (see Fig. 1d). This structure allows to connect several gates together to build a larger gate contact. It is important to study the interface generation current.

The circular MOS capacitor has a gate area of $1.767 \times 10^{-2} \text{ cm}^2$. It is used to determine the flat-band voltage and the oxide capacitance per unit area. The flat-band voltage V_{fb} describes the potential which has to be adjusted on the MOS device to flatten the energy bands. The change of V_{fb} with the dose gives a direct measurement of the **concentration of ionization-induced positive**

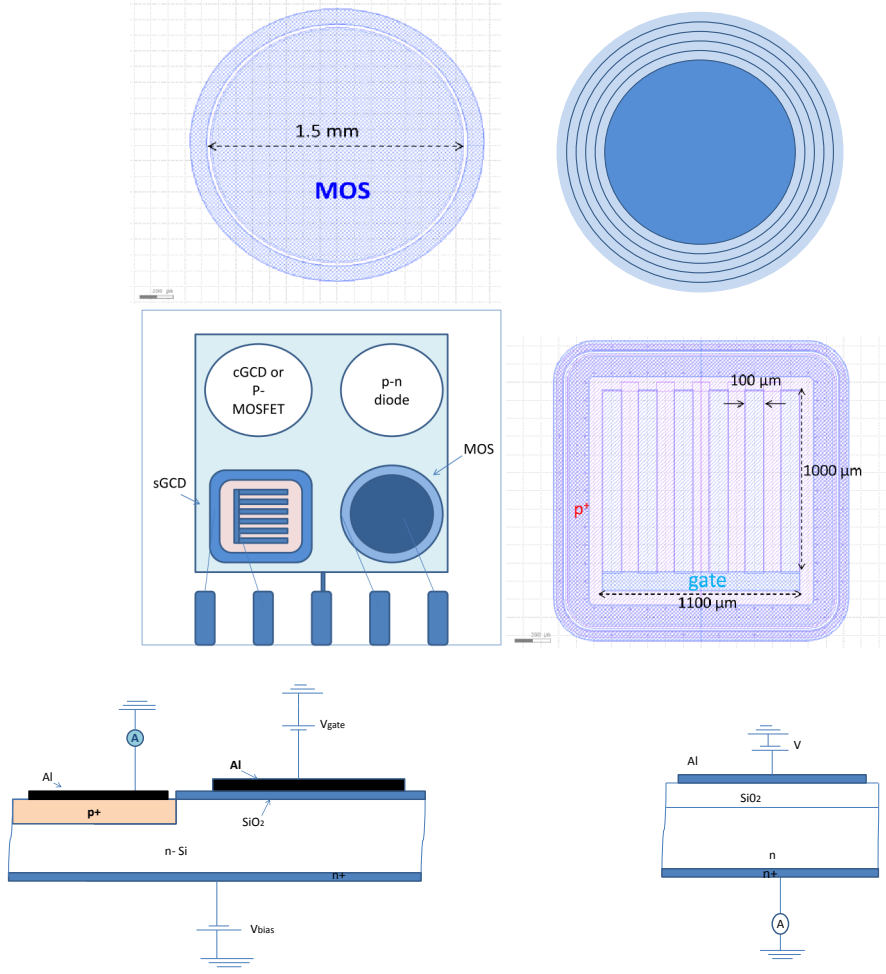


Figure 1. (a) Layout of the MOS capacitor, (b) Layout of the circular gate-controlled diode, (c) Layout of the ceramic support with the wafer on top, (d) Layout of the square gate-controlled diode, (e) Cut-view of the square gate-controlled diode, (f) Cut-view of the MOS capacitor.

oxide charges N_{ox} trapped in the oxide, only if all the charges remain not change

$$\Delta V_{fb} = \frac{q_0 \cdot d}{\epsilon_0 \epsilon_{ox}} \cdot \Delta N_{ox} \quad (2.1)$$

where d is the oxide thickness, q_0 the electron charge, ϵ_0 the dielectric constant and ϵ_{ox} the permittivity of the oxide.

2.1 General properties and measurements performed

General measurements were performed on the p^+n diode as shown in Fig. 2, 3.

Figure 2(c) shows the capacitance of the p^+n diode measured at 1 kHz, 10 kHz, 100 kHz, plotted as $1/C^2$ versus the bias voltage. $1/C^2$ increases linearly with bias voltage and saturates at the full depletion voltage V_{dep} .

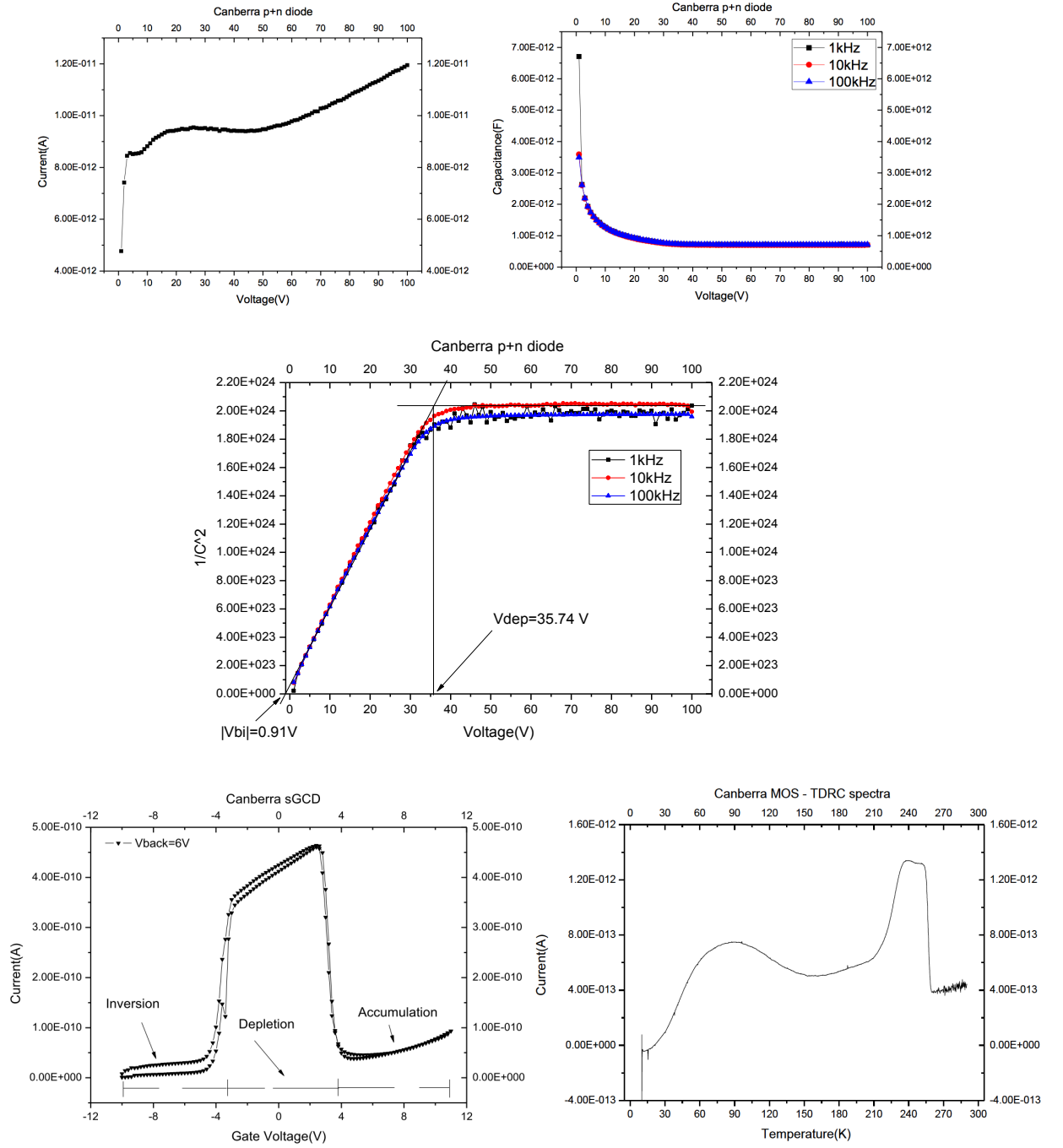


Figure 2. (a) I-V curve of the unirradiated p+n diode, (b) C-V curve of the unirradiated p+n diode, (c) Determination of the depletion voltage on the non-irradiated p^+n diode, (d) I-V curve of the unirradiated square Gate Controlled Diode, (e) TDRC spectrum for the unirradiated MOS capacitor, performed with heating rate of 0.183 K/sec.

For the simple circular p^+n diode from Fig. 1, the full depletion voltage was measured to be $V_{dep} = 35.74$ V, $C_{dep} = 0.7 \times 10^{-12}$ F and the built-in voltage $V_{bi} = 0.91$ V. Therefore the thickness

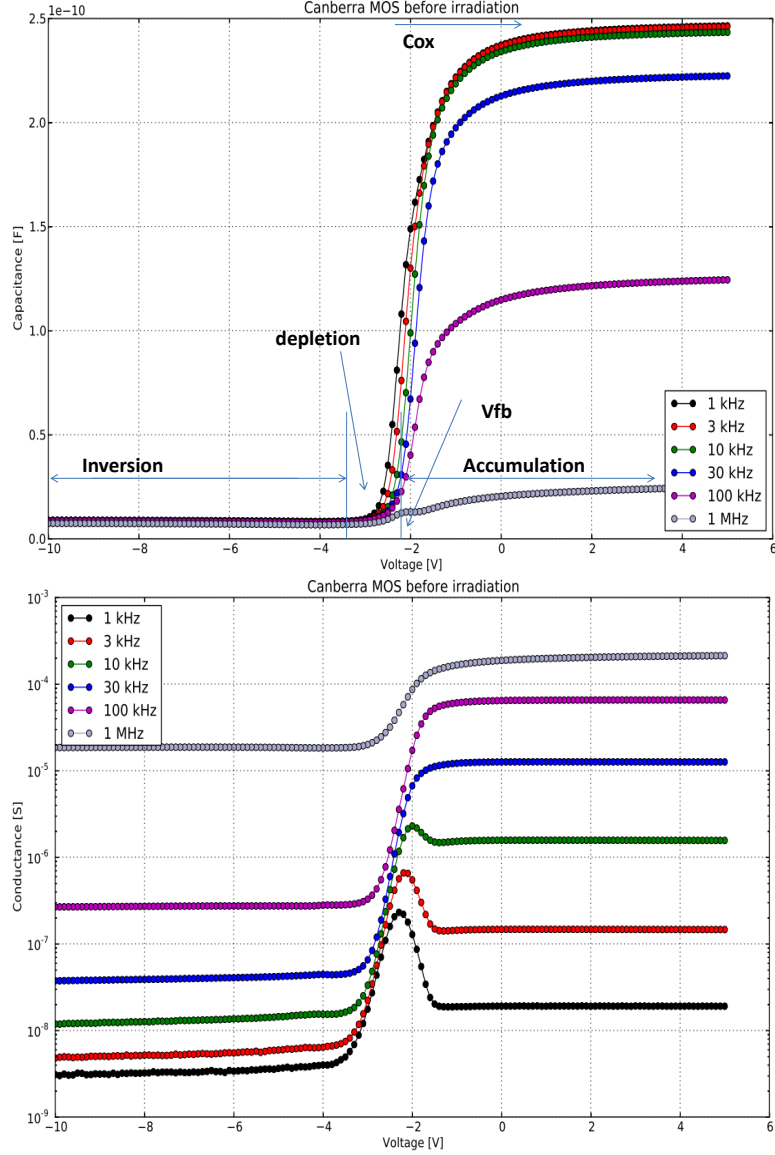


Figure 3. (C-V (top) and G-V (bottom) curves of the unirradiated MOS capacitor in different frequencies.

of the silicon bulk was calculated as:

$$t_{Si} = \epsilon_0 \cdot \epsilon_{Si} \frac{Area}{C_{dep}}, \quad (2.2)$$

$t_{Si} = 266 \times 10^{-6}$ m, where $Area = 0.0176$ cm² is the effective diode area, $\epsilon_0 = 8.85 \times 10^{-12}$ F/m and $\epsilon_{Si} = 11.9$ is the dielectric constant of silicon. The effective doping concentration for the p^+n diode was calculated as

$$N_{eff} = \frac{(V_{dep} + |V_{bi}|) \cdot \epsilon_0 2 \epsilon_{Si}}{q_0 t_{Si}^2}, \quad (2.3)$$

and found to be $N_{eff} = 6.82 \times 10^{11}$ cm⁻³.

For the square Gate Controlled Diode the IV curve was measured. Three different conditions can be seen in Fig. 2(d) and Fig. 4: accumulation, depletion and inversion. In the accumulation

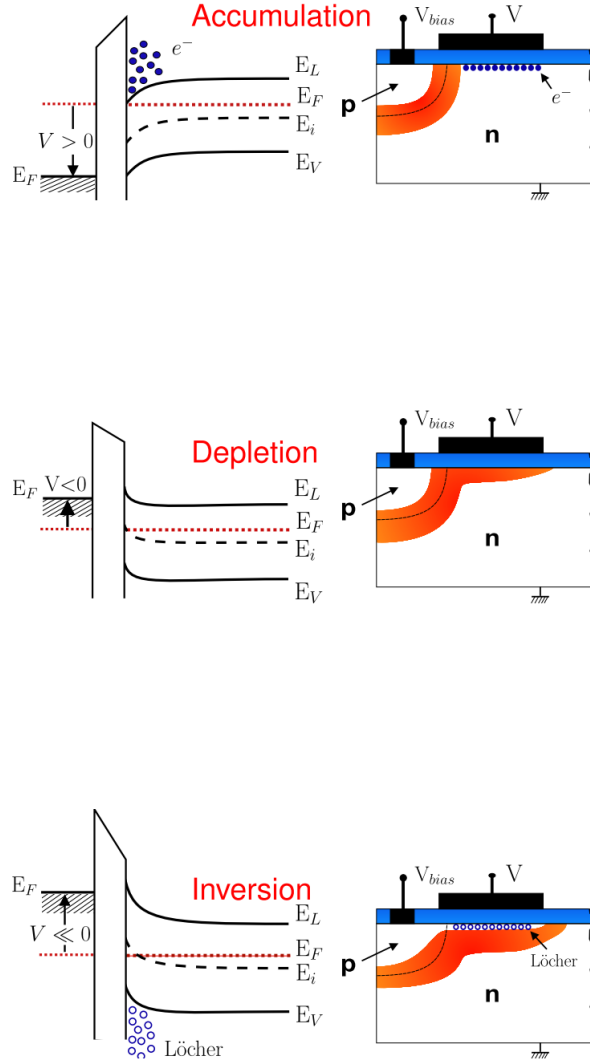


Figure 4. Energy-band diagrams for ideal MOS capacitors with n-type semiconductor substrate under different bias, for the conditions of (a) accumulation, (b) depletion and (c) inversion.

condition the total measured current is given by the sum of the bulk and diffusion current of the p+n diode:

$$I_{leak,acc} = I_{p+n,bulk} + I_{diff}. \quad (2.4)$$

In depletion, in addition to the the bulk current of the p^+n diode and MOS capacitor, which is now depleted, and to the diffusion current, another contribution comes from the surface current of the MOS capacitor:

$$I_{leak,dep} = I_{p+n,bulk} + I_{diff} + I_{MOS,bulk} + I_{MOS,surface}. \quad (2.5)$$

In inversion, the interface traps are shielded by a layer of induced holes, therefore the measured

current is given by the sum the p^+n diode and MOS capacitor bulk current and the diffusion current:

$$I_{leak,inv} = I_{p+n,bulk} + I_{diff} + I_{MOS,bulk}. \quad (2.6)$$

For the MOS capacitor the oxide capacitance (1kHz frequency) is given by the capacitance measured in accumulation conditions. According to Fig. 3, this is $C_{ox} = 2.4 \times 10^{-10}$ F. Using this value, the thickness of the SiO_2 layer was calculated as $d_{ox} = 252$ nm using Eq. 2.2. The effective doping concentration for the MOS was calculated to be $N_d = 6.7 \times 10^{11} \text{ cm}^{-3}$ using Eq. 2.3. The oxide charge density in the MOS capacitor was then calculated as

$$N_{ox} = \frac{Q_{ox} q_0^{-1}}{A_{gate}} \quad (2.7)$$

and found to be $N_{ox} = 1.42 \times 10^{11} \text{ cm}^{-2}$.

3. Irradiation with X-rays

3.1 Irradiation facility

For the irradiations, a facility has been set up [3] at the beam line F4 of HASYLAB DORIS III at DESY. The set-up is shown in Fig. 5. It consists of an adjustable Ta chopper, which permits the reduction of the full dose rate (180 kGy/s) down to 0.5%, an adjustable collimator to precisely define the region of irradiation, and a sample holder with 5 biasing lines, which is connected to a liquid cooling system to control the temperature in the range of 10 to 30 °C.

The test structures were glued and wire-bonded to a ceramic substrate, shown at the top left of Fig. 5. This holder makes the exchange and test of the structures easy and safe.

The set-up is mounted on a table, which permits computer control of both the horizontal and vertical movement of the sample enabling areas larger than the beam spot to be irradiated uniformly. A pneumatic beam shutter, for a precise determination of the exposure time to the beam, was installed close to the exit window of the beam pipe.

3.2 Beam profile at beamline F4

The beam line F4 at DORIS III provides a "white" photon beam from a bending magnet. The energy spectrum was calculated taking into account the X-ray absorption by the materials in the beam line. As shown in Fig. 7(a) the typical photon energy at the detector was 12 keV with the full width at half maximum of about 10 keV.

The profile of the X-ray beam was measured by the photocurrent in a silicon pad diode biased to 7 V. We selected this value for the voltage so that the current value in the photodiode is saturated. In this way the measurement of the current is accurate. The value of the diode current as a function of the diode bias voltage is shown in Fig. 6. An RC box was used to apply the bias voltage and change the time constant, in order to be able to measure almost a constant current during DORIS operated in 10 bunch mode.

The pad diode, glued onto a ceramic substrate as shown in Fig. 5, was placed onto the sample holder. The collimator was opened to a window of 0.2 mm \times 0.2 mm. The sample was moved in steps of 0.1 mm to scan the beam. The photon flux as a function of position was calculated from

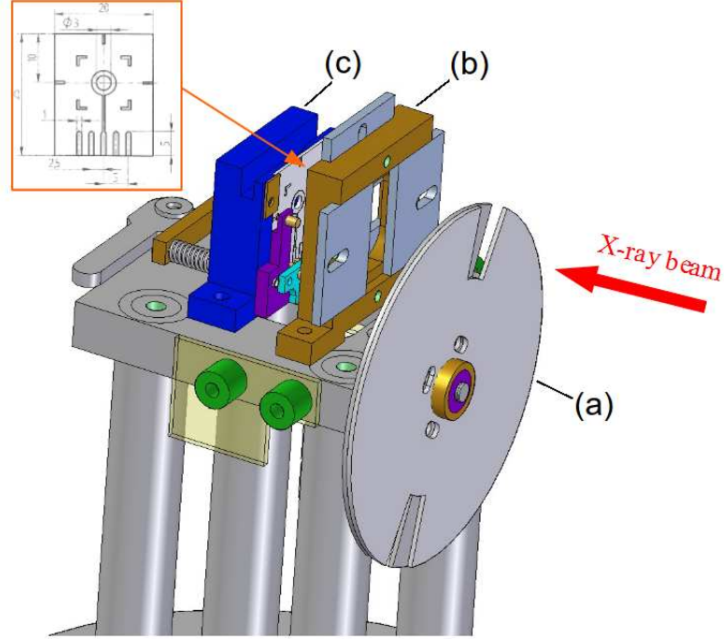


Figure 5. Set-up of the irradiation facility: Chopper (a), collimator (b), and sample holder (c) with cooling and spring mechanism. The ceramic substrate which is put into the sample holder carries test structures and sensors (shown at the top left). The entire set-up can be moved in all three dimensions by computer control.

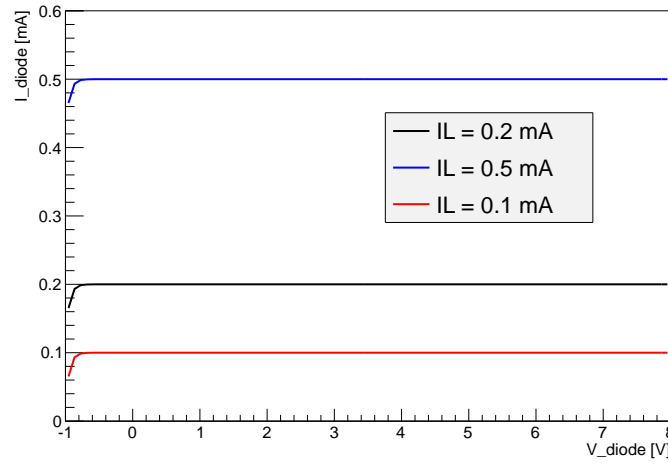


Figure 6. Diode current I_d as a function of the diode bias voltage V_d for different values of the light-induced current I_L .

the measured current, the average energy of 3.6 eV to produce one electron-hole pair in silicon and the energy deposited by the photons. The fraction of interacting photons was derived from the energy spectrum and the absorption length of X-rays as a function of energy. Figure 7(b) shows the measured two dimensional beam profile.

The horizontal and vertical profiles at the center of the beam are shown in Fig. 7(c) and 7(d). The width of the horizontal profile is about 5 mm and uniform; whereas the full width of half

maximum of the vertical profile is 4 mm and Gaussian-like. The distributions are compatible with the expectations for the synchrotron radiation of the positrons of DORIS III in a bending magnet.

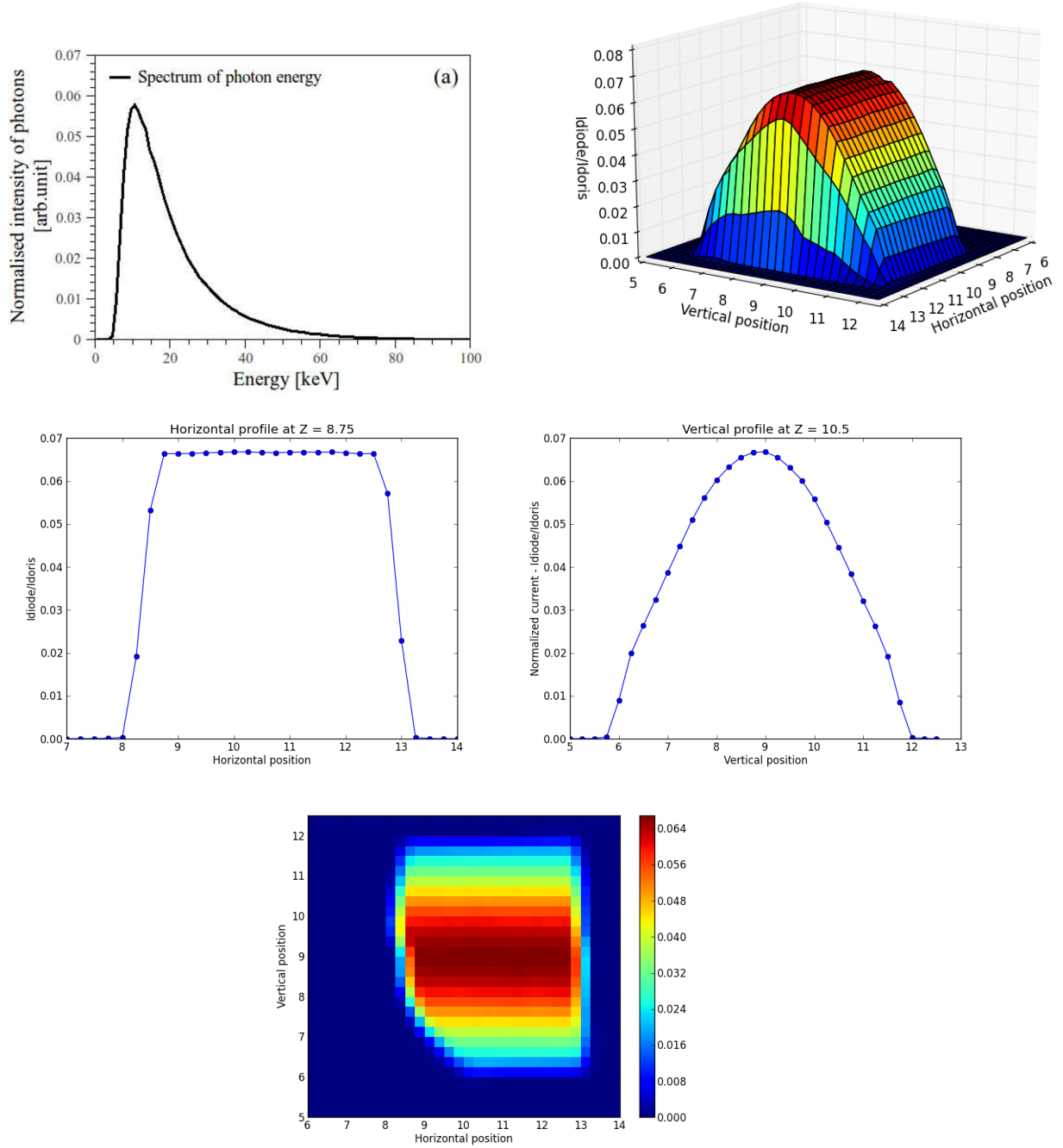


Figure 7. (a) Normalised spectrum of photon energy. (b) Two dimensional beam profile. (c) Horizontal profile. (d) Vertical profile. (e) Beam spot.

3.3 Dose calculation and irradiations on the test fields

Using the data shown in Fig. 7(a) (normalised photon spectrum) and 7(b) (the two dimensional beam profile), the average dose in the insulator can be calculated according to:

$$Dose = \frac{3.6eV \cdot R}{q_0 \rho_{Si} d_{Si} A} \iiint_{\Delta x, \Delta y, t_{irra}} J_{diode}(x, y) \cdot dx dy dt, \quad (3.1)$$

with $J_{diode}(x, y)$ the current density (A/mm²) measured by the silicon diode, t_{irra} the duration of irradiation, ρ_{Si} and d_{Si} the density and thickness of the silicon diode. A is the irradiated area of the detector, Δx and Δy the horizontal and vertical extensions of the detector in the plane perpendicular to the beam and q_0 is the elementary charge. R is the ratio of energy deposited per unit mass in the insulator ($E_{Insulator}$) to energy deposited in the silicon (E_{Si}) for the given photon spectrum:

$$R = \frac{\frac{E_{Insulator}}{\rho_{Insulator} \cdot d_{Insulator}}}{\frac{E_{Si}}{\rho_{Si} \cdot d_{Si}}}, \quad (3.2)$$

where $\rho_{Insulator}$ and $d_{Insulator}$ are the density and thickness of the insulator, respectively. For the energy spectrum given above, $d_{SiO_2} = 300$ nm and $d_{Si} = 300$ μ m, the value of R is 1.30 and is essentially independent of d_{SiO_2} for the typical oxide thickness of sensors. Without the chopper the typical dose rate in SiO₂ is 180 kGy/s, which corresponds to a flux of approximately 1.1×10^{14} photons/(mm² · s).

The results from the measurement of the dose agree within 20% with the calculations performed using the value of the current of the DORIS III beam, the field of the bending magnet and the geometry of the set-up. All the references to the dose in the text refer to the surface dose in SiO₂. The dose enhancement in SiO₂ has not been taken into account in this study [11].

4. Results on irradiated test structures

Results are shown from MOS capacitors irradiated in steps to 9 X-ray doses, in the range between 2.2 kGy and 100 MGy. Table 1 shows the identification codes of the irradiated structures and the doses at which they were irradiated.

Dose (kGy)	2.2	10	20	100	500	1000	5000	10 ⁴	10 ⁵
Structure	145-3	147-3	147-3	145-3	145-4	145-4	145-4	146-3	145-4

Table 1. History of the irradiation of the different structures.

The irradiations took between 7.5 seconds and 6 hours. The first C/G-V and I-V measurements were performed about 20 minutes after irradiations. Due to a significant annealing of the radiation induced effects already at room temperature, a quantitative interpretation of the measurements taken just after the irradiation is difficult. After these first measurements, the structures were annealed for 10 minutes in an oven with a temperature of 80 °C. Previous studies [5] show that this is sufficient to make the samples relatively stable.

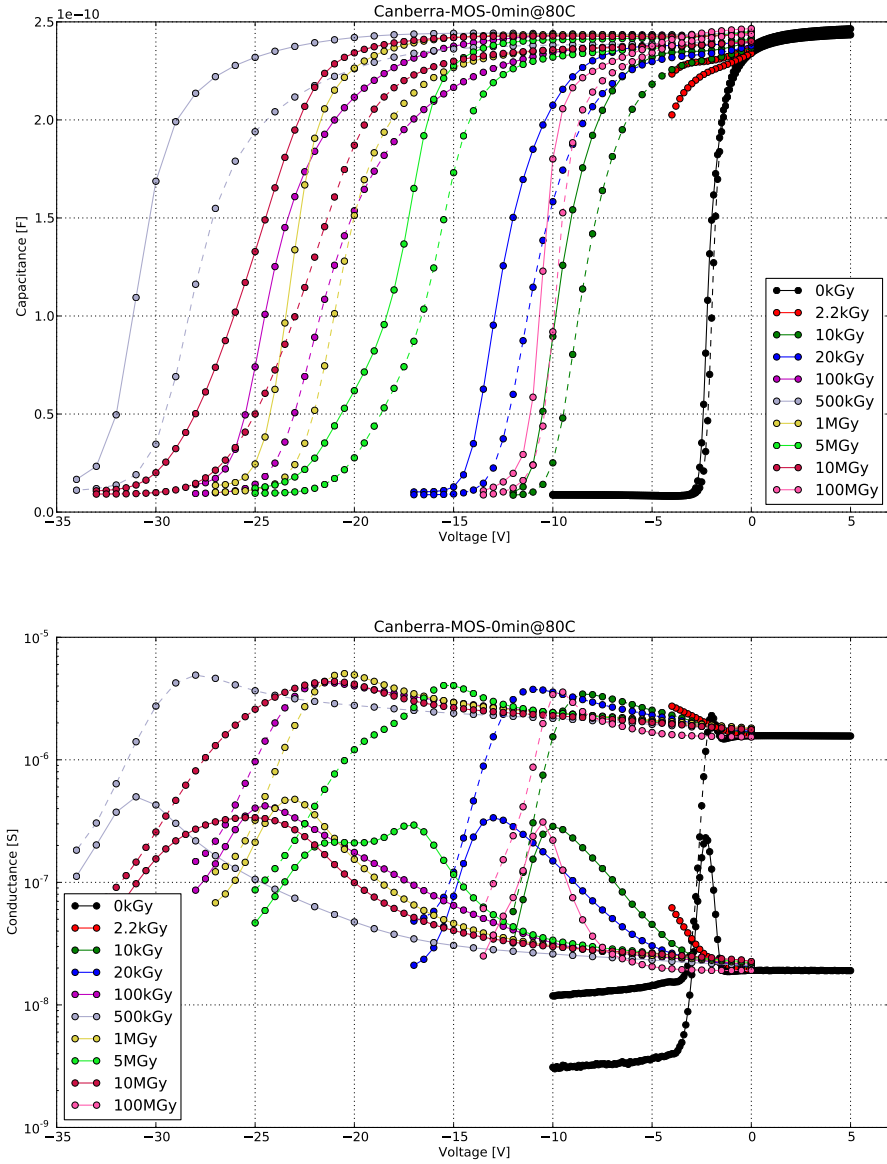


Figure 8. (a) C-V and (b) G-V curves of the MOS capacitors as a function of dose (12 keV X-rays) measured at 1 kHz and 10 kHz (solid and dashed lines) before and after annealing for 10 minutes at 80°C.

4.1 Measurement of the C/G-V and I-V curves

The Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements have been performed at room temperature. The Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) measurements have been performed using an Agilent E4980A bridge. An AC voltage of 50 mV and frequencies from 1 kHz to 1 MHz have been chosen. The voltage scan started at 0 V (strong accumulation in our case) and stopped before strong inversion was reached in order to avoid injecting holes into border traps [5]. The results of the C-G/V measurements of the MOS at 1 and 10 kHz for all the measured doses are plotted in Fig. 8 (before annealing) and 9 (after annealing).

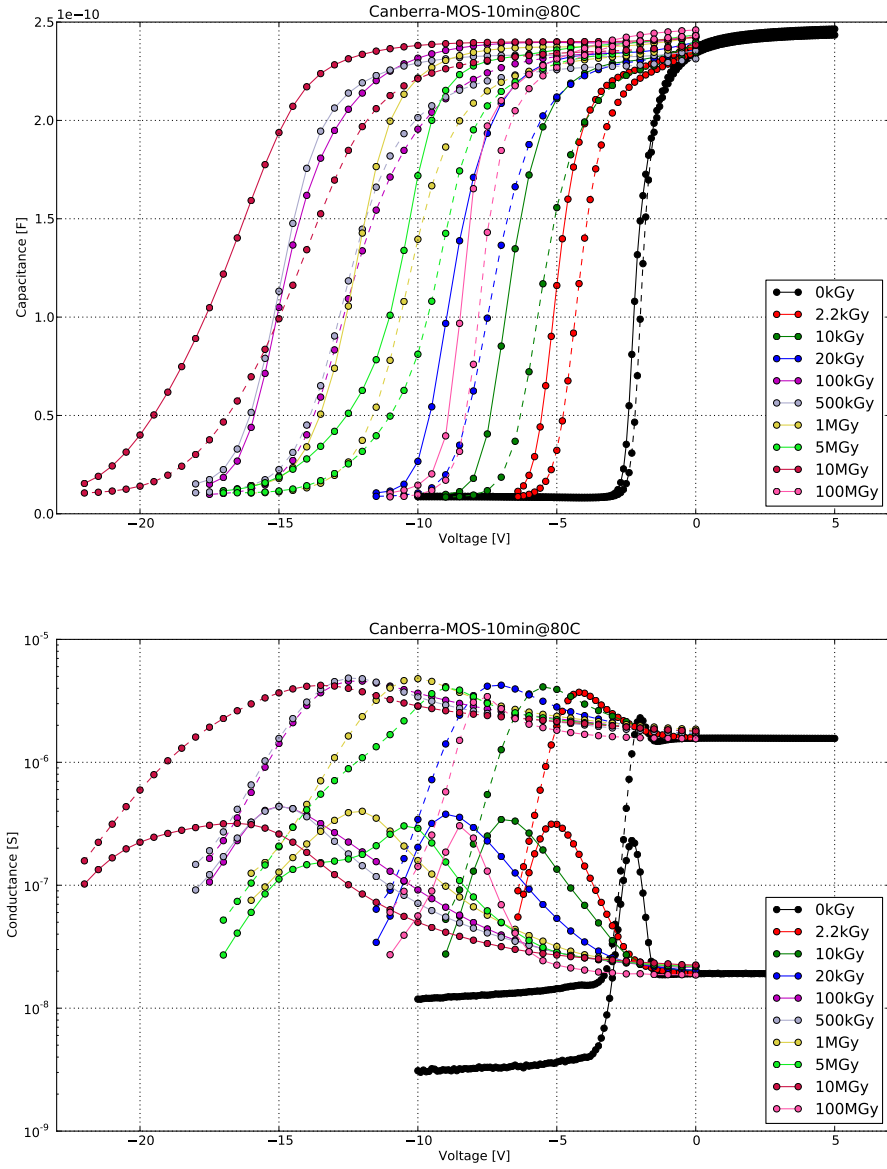


Figure 9. (a) C-V and (b) G-V curves of the MOS capacitors as a function of dose (12 keV X-rays) measured at 1 kHz and 10 kHz (solid and dashed lines) before and after annealing for 10 minutes at 80°C.

The radiation-induced interface traps can be charged or discharged by an external AC signal, and thus act like a frequency dependent capacitor as seen in Fig. 8 and 9. This effect is implemented in the model for the MOS capacitor discussed in section 4.2.1.

The results of the I-V measurement on the square gate-controlled diode for all the measured doses are plotted in Fig. 10 (before and after annealing). Compared to the I-V curve without irradiation, the leakage currents after irradiations increase by two orders of magnitude. The leakage current is mainly due to the surface generation current from the Si-SiO₂ interface regions not covered by an electron accumulation layer. The measured leakage current agrees with the surface

current of $\sim 8 \mu\text{A}/\text{cm}^2$ measured for highly irradiated gate controlled diodes [3].

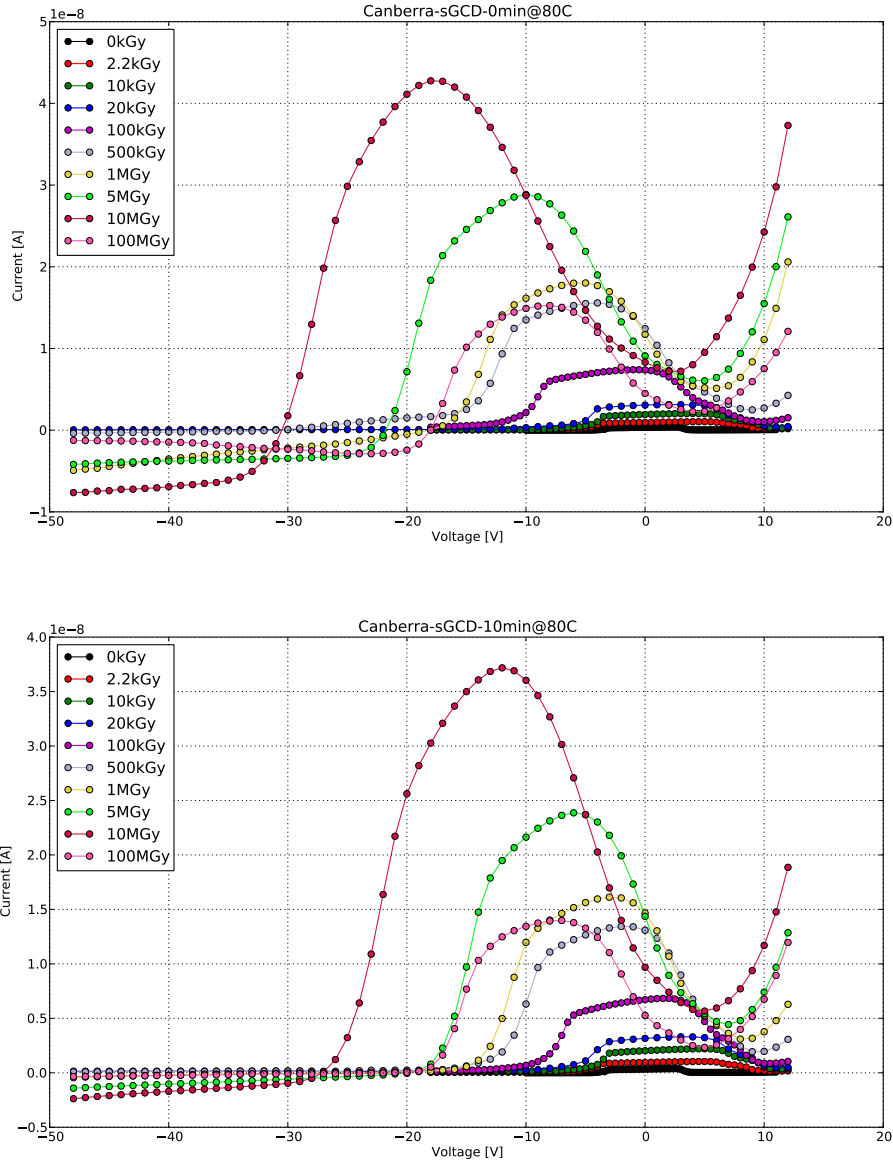


Figure 10. (a) I-V curves of the square Gate Controlled Diode as a function of dose (12 keV X-rays) measured before (a) and after (b) annealing for 10 minutes at 80°C.

4.2 Measurement of the Thermally Dielectric Relaxation Current

In order to determine the parameters and the densities of interface traps the Thermally Dielectric Relaxation Current (TDRC) technique [14, 7] was employed (see Fig. 11). The TDRC technique is a well-established tool to study majority carrier traps at the Si-SiO₂ interface of MOS capacitors. The TDRC measurement was carried out as follow: the MOS capacitor was cooled to low temperature (10 K using a helium cooling system) biased in strong accumulation to fill the interface traps

with majority carriers (with electrons for n-type silicon). At 10 K the gate voltage was changed to bias the MOS capacitor in weak inversion, in which condition traps remained filled since the temperature was too low to allow the thermal emission of the electrons. Then the sample was heated up to room temperature with a constant rate of $\beta = 0.183$ K/s. As the temperature rises the trapped electrons are gradually released through thermal emission and the trap discharge current is recorded as TDRC spectrum. In general, the TDRC spectrum is due to both Si-SiO₂ interface traps and traps in the depletion region of the bulk silicon. Fermi level scans the band gap, charges are emitted and the current is measured as a function of temperature. However, since the 12 keV X-rays only introduce interface traps, the TDRC spectrum from bulk traps can be ignored.

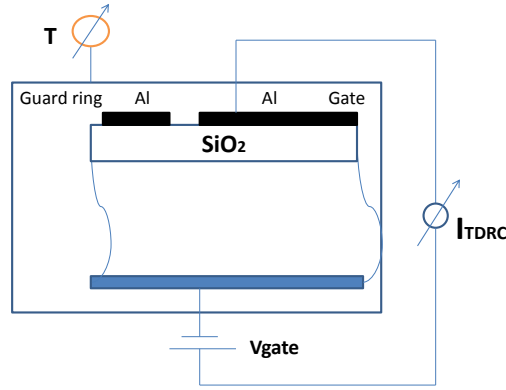


Figure 11. Layout of the TDRC measurement.

Figure 12 shows the TDRC spectrum as a function of temperature for different doses after annealing at 80°C for 10 minutes. A pronounced peak at ~225 K, corresponding to an energy of 0.60 eV as measured from the conduction band, and a broad distribution between 210 K and 70 K can be observed. The TDRC spectrum increases with dose up to 10 MGy and decreases at 100 MGy. The decrease of the TDRC spectrum is probably due to the annealing of traps at high dose rates during the longer irradiation time.

In the analysis, we assumed that the interface states-density of each trap are uniformly distributed in space with Gaussian-like energy distributions in the silicon band gap. Four Gaussian distributions were used to describe the measured TDRC spectra. The energy distribution and the density of interface states of each trap were calculated using the equations (16) and (17) in the paper of H. A. Mar [8] for separated, Gaussian distributed TDRC spectrum. For this calculation, electron capture cross sections for each trap are needed, which were obtained by minimizing the χ^2 of the difference between the measured and calculated C/G values for the frequencies 1, 3, 10 and 30 kHz at different gate voltages. The model calculation is discussed in the next section. Parameters, e.g. electron capture cross section, mean energy and full width of half maximum of each trap have been reported elsewhere [5].

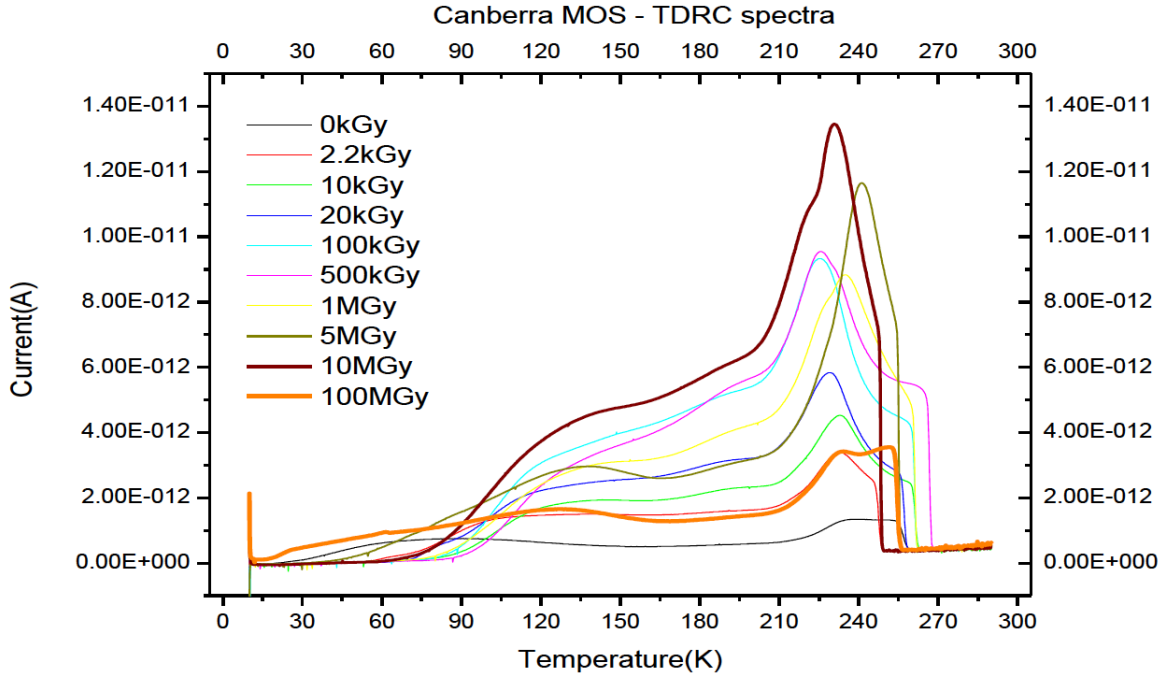


Figure 12. TDRC spectra for different doses, with heating rate 0.183K/sec after annealing for 10 minutes at 80 °C .

4.2.1 Model calculation

The following model which includes the effects of the interface traps was used to describe the C/G-V measurements of the MOS capacitors. As shown in Fig. 13, the model consists of an RC circuit. The equations to calculate the capacitance and the resistance of each element in the circuit were described elsewhere [5]. The admittance of the circuit as a function of gate voltage was calculated based on the measured TDRC spectra, evaluated electron capture cross sections, doping concentration and fixed oxide charge density, and finally compared to the measured parallel capacitance and conductance. The doping concentration of the semiconductor close to the Si-SiO₂ interface was determined from the high frequency capacitance in strong inversion following the Lindner approximation [9]. The three interface traps were assumed to be acceptors. The fixed oxide charge density N_{ox} , which just causes a shift in voltage, were extracted from the voltage shifts observed in the measured C/G-V curves.

4.3 Procedure to extract I_{surf} , N_{ox} and N_{it}

The interface generation current I_{surf} is caused by generation of charge carriers in the interface,

$$I_{surf} = q_0 n_i S_0 A_{gate}, \quad (4.1)$$

where n_i is the intrinsic charge carrier concentration (assumed in the calculations to be 10^{10} cm^{-3}), A_{gate} the gate area and S_0 the interface generation velocity. Assuming a homogeneous distribution of the interface states across the band-gap, S_0 is given by

$$S_0 = \sigma v_{th} \pi k_B T D_{it}, \quad (4.2)$$

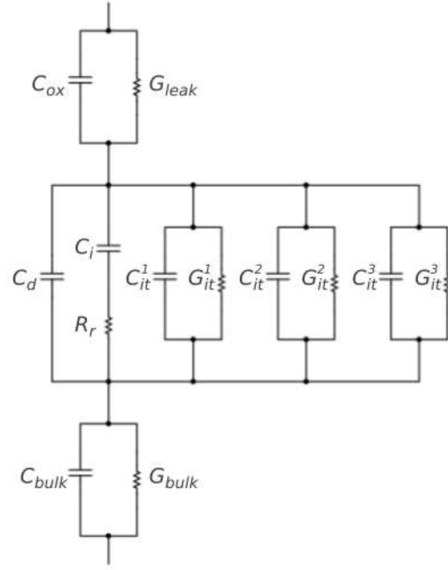


Figure 13. Model with three interface traps used to calculate the C/G-V curves for the MOS capacitors: C_{ox} and G_{leak} is the capacitance and conductance of the insulator; C_d , the capacitance of the depletion layer; C_i , the inversion capacitance due to minority carriers accumulating at the interface; R_r , the recombination/generation resistance; C_{it}^i and G_{it}^i , the capacitances and conductances due to interface traps; C_{bulk} and G_{bulk} , the capacitance and conductance of the non-depleted silicon bulk. The relations between C_{it}^i and G_{it}^i and the microscopic properties of the traps are given in [5].

with σ being the effective capture cross-section for electrons and holes of the interface trapping centers, which depends on the available free energy levels in the band gap, v_{th} the thermal velocity of the minority carriers, k_B the Boltzmann constant, T the absolute temperature and D_{it} the interface state density in $\text{cm}^{-2} \text{eV}^{-1}$.

For the determination of the interface generation current I_{surf} with a gate-controlled diode a fixed reverse bias voltage V_{bias} is applied to the diode and the current is measured as a function of the gate voltage V_{gate} . The method is shown in Fig. 14.

The generation-recombination centers at the Si-SiO₂ interface contribute to the total current, visible as a sharp increase in the IV curve in the middle voltage region. Furthermore, the bulk generation current of the depleted area under the gate string, which grows with increasing gate voltage V_{gate} , contributes to the measured current. At the inversion voltage an inversion layer under the oxide is formed screening the contribution of the interface generation current. For gate voltages more negative than the inversion voltage the total generation current remains constant because the gate depletion region is pinned to its maximum depth. If we call I_{aver} the average value of the current at inversion, i.e. at the lowest measured voltages, as depicted in the Figure, I_{surf} can be calculated for different doses as $I_{surf} = I_{max} - I_{aver}$ (see Fig. 14) and then used to extract the surface current density:

$$J_{surf} = \frac{I_{surf}}{A_{gate}}. \quad (4.3)$$

The interface trap and oxide charge densities were extracted from the TDRC spectra combined with the C-V and G-V curves by using a Mathcad program implementing the model described else-

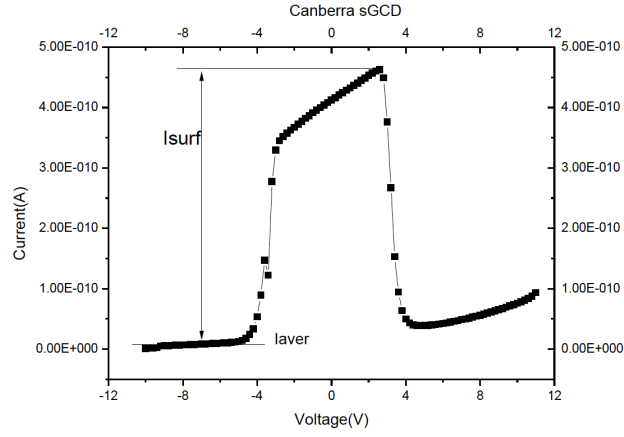


Figure 14. Method to calculate the interface generation current.

where [5] (see also section 4). The TDRC spectrum was used to extract four different Gaussian distributions representing the density and location of interface traps in the band gap. These distributions were used as input in the Mathcad program to extract the amount of interface traps in the band gap, N_{it} . The density of oxide charges N_{ox} was adjusted in the program together with the capture cross sections to get the best fit of the C-V and G-V curves. An example of the resulting C-V and G-V curves compared with the calculations from the model is shown in Fig. 15.

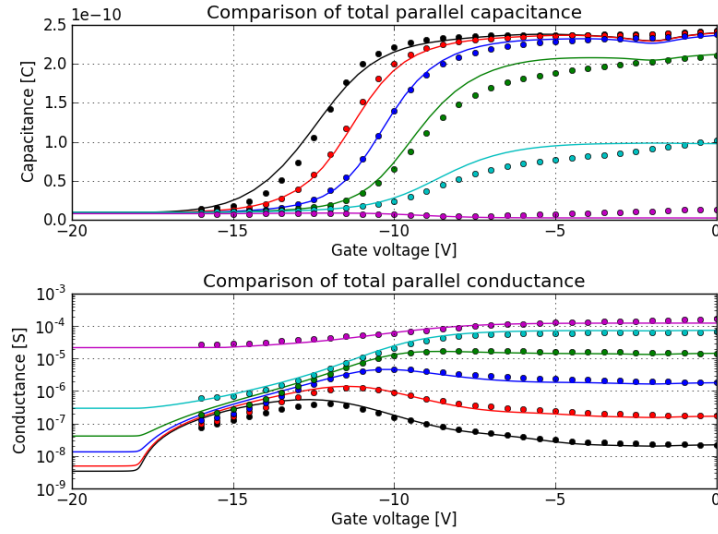


Figure 15. Example of (a) CV and (b) GV curves: the data are compared with the calculations provided by the Mathcad program, for dose 1MGy after annealing for 10 minutes at 80°C.

As a cross check, the interface trap density was extracted also by directly integrating the TDRC spectrum for every dose:

$$N_{it} = \frac{1}{A_{gate} q_0} \int_0^{250} \frac{I_{TDRC}(T)}{\beta} dT. \quad (4.4)$$

The obtained results were always compatible with those given by the Mathcad program.

4.4 Dose dependence of J_{surf} , N_{ox} and N_{it}

Figures 16 and 17 show the dose dependence of J_{surf} , of the interface generation velocity S_0 and of the density of the oxide charges and interface traps, N_{ox} and N_{it} .

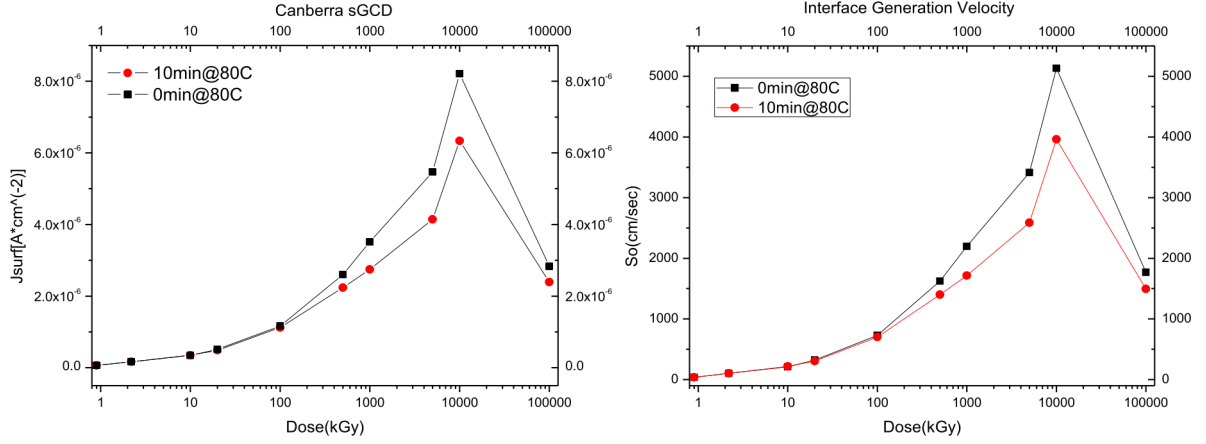


Figure 16. (a) Surface Current Density J_{surf} of the Square Gate Controlled Diode and (b) Interface Generation Velocity S_0 as a function of dose (12 keV X-rays) measured before and after annealing for 10 minutes at 80°C.

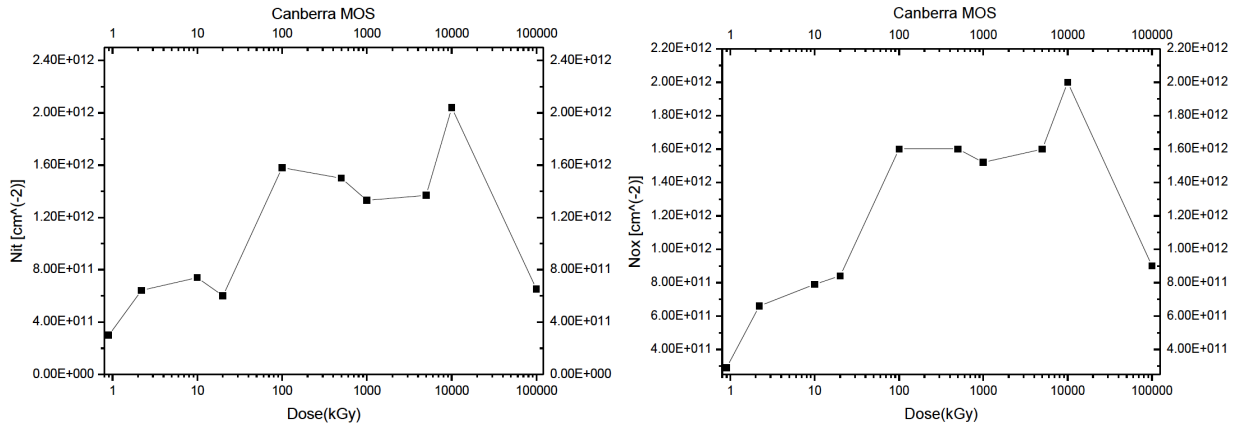


Figure 17. (a) Interface Traps Concentration N_{it} of the MOS capacitor and (b) Oxide Charge Concentration N_{ox} as a function of dose (12 keV X-rays) measured after annealing for 10 minutes at 80°C.

In all the cases for all the measured quantities an increase is observed up to a dose of 10MGy, with a subsequent decrease to 100MGy. Detailed studies for searching the reason why the densities of N_{ox} , N_{it} and J_{surf} sharply drop at 100MGy should be continue in the future.

5. Summary and outlook

We have measured the characteristics of MOS capacitor and square gate-controlled diode fabricated by Canberra. These structures were irradiated in steps from 2.2kGy to 100MGy. At each step the C/G-V, I-V and TDRC curves were measured. This allowed the determination of the interface traps

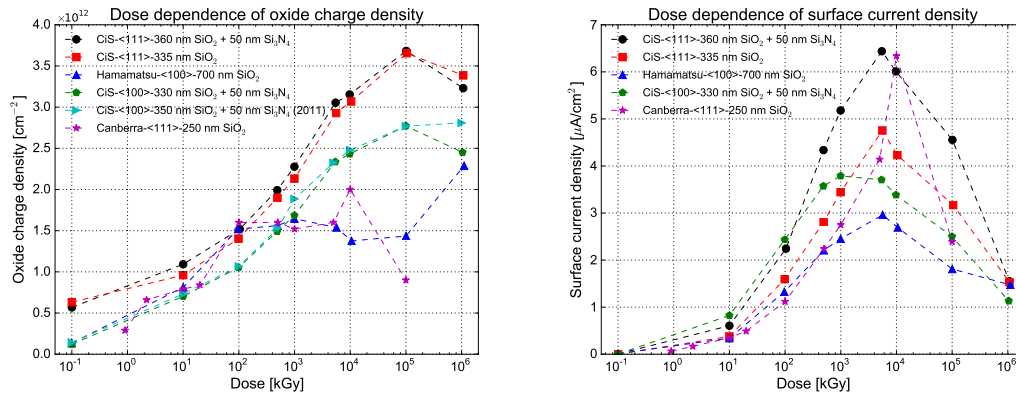


Figure 18. (a) Oxide Charge Concentration N_{ox} as a function of dose (12 keV X-rays) measured after annealing for 10 minutes at 80 °C for different companies and (b) Surface Current Density J_{surf} as a function of dose (12 keV X-rays) measured after annealing for 10 minutes at 80 °C for different companies.

and oxide charge density as well as the surface current and the surface generation velocity. In all the cases an increase of the density is observed at 10MGy with subsequent decrease at 100MGy. This study complements that already performed on similar structures from CiS, Hamamatsu and we can compare the results as shown in Figure 18.

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