



UNIVERSITY PARIS-SUD XI
MAGISTERE OF FUNDAMENTAL PHYSICS
YEAR 2011-2012

Studies of the front-end electronics of the Analog HCAL.

Author:
Eldwan BRIANNE

Supervisors:
Felix SEFKOW
Mark TERWORT

At DESY (Deutsches Elektronen-Synchrotron)
85 Notkestraße, 22607 Hamburg
27 May to 3 September 2012.



international linear collider



September 3, 2012

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Acknowledgments

I would like to thank my supervisor Mark Terwort and my Mentor Felix Sefkow for their support along these 3 months. Also welcome to a new member in the AHCAL Group named Leo born during my stay at DESY.

Thanks very much to Mathias Reinecke, Oskar Hartbrich, Benjamin Hermberg, Katja Krueger for their support and help to answer my questions.

Concerning the summer program, thanks to Andrea Schrader, Olaf Behnke and Doris Eckstein for the organisation work and all the advice they gave us.

I was really pleased to participate in this summer program. I was able to meet lots of people from different countries and I recommend it. During this summer program, I visited lots of places (Amsterdam, Berlin, Lübeck..) and this program was an unforgettable experience. Thanks to Irina, Diana, Kilesh, William, Daniel, Mark, Aiveen, Lizzy, Sander and everyone for everything and hope to see you again maybe at DESY next year.

I hope to return to DESY for doing my PhD next year.

Studies of the front-end electronics of the Analog HCAL

Abstract

A prototype of an analog hadronic calorimeter for the ILC, a future linear accelerator, is currently developed at DESY. The aim is to build a fully capable detector with fully integrated readout electronics.

This report is focused on the study of the readout ASIC SPIROC particularly on the time measurement (TDC). The time resolution achieves 100 ps in ILC mode and 1-1.5 ns in testbeam mode.

Further aspect of SPIROC are studied in this report.

Résumé

Un prototype de calorimètre hadronique pour l'ILC, un futur accélérateur linéaire, est actuellement en développement à DESY. Le but est de réaliser un détecteur embarquant toute l'électronique (SPIROC) permettant de recueillir les données.

Ce rapport se focalise sur l'étude de l'électronique frontale de l'AHCAL notamment sur la mesure du temps (TDC). La résolution du temps approche 100 ps dans le mode ILC et 1-1.5 ns dans le mode testbeam.

D'autres aspects de la puce électronique SPIROC sont étudiés plus profondément dans ce rapport.

1 Introduction

1.1 The International Linear Collider

The International Linear Collider (ILC) (Fig. 1.1) is a project for a lepton collider. It is a e^+e^- collider with a center of mass energy up to 500 GeV, and will allow an upgrade to 1 TeV in the second stage (in comparison the LHC works at 8 TeV now and is designed to be at 14 TeV). There are two candidate sites for the ILC, a flat site or a mountain site (both in Japan) but it is not decided yet.

This is a linear collider because of the synchrotron radiation which limits the maximum energy for a circular accelerator (the radiation is proportional to $1/m^4$). The importance of the ILC project is that it will be used to do precision measurements of known particles (top quark, Z boson...) or new discovered particles (like the light Higgs Boson at 125 GeV) with great accuracy because the background is much less with lepton-lepton collisions than pp collisions. Also this will permit to find signs of new physics like SUSY particles (neutralino, chargino...).

The ILC is planned to have two separate detectors based on complementary technologies. For now, two concepts have been verified, the Silicon Detector (SiD) and the International Large Detector (ILD). This is a real challenge for everyone because the detector has to be designed in a such way that it allows to change the detector position within a day and with a sub-millimeter even nanometer precision.

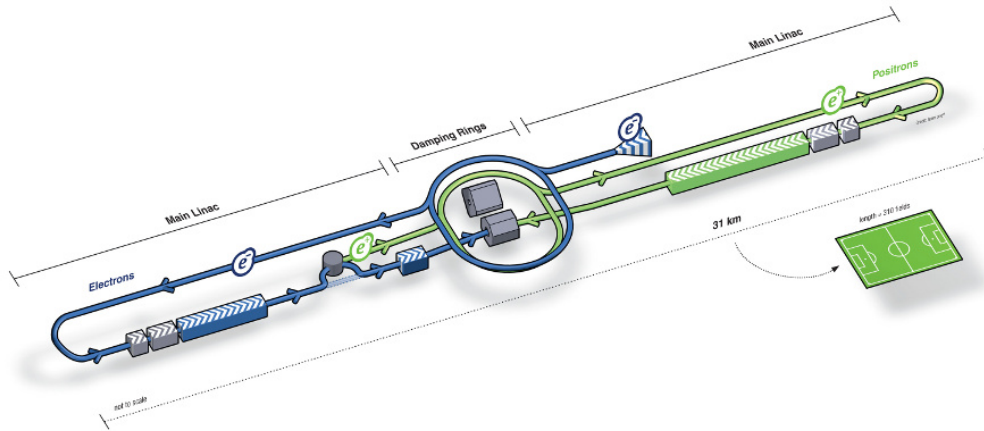


Fig. 1.1: Scheme of the International Linear Collider. It plans to be 30 km long to achieve a center of mass energy of 500 GeV.

1.2 The International Large Detector

The International Large Detector (ILD) (Fig. 1.2) is a barrel and endcaps detector consisting of many specialized sub-detectors around the interaction point. The concept of this detector is to achieve a high energy resolution combining particle flow algorithms and high granularity for the ECAL and HCAL to trace single particles in jets.

The different parts of the detector are :

- The Vertex Detector (VTX) using five single or three double layers of silicon pixel sensors which enables the measurement of the position of the interaction point with an extreme accuracy.
- The Time Projection Chamber (TPC) consists of a chamber full of gas which is ionized when a charged particle passes through. This allows a spacial tracking in a large volume (up to 224 points per particle track).
- An electromagnetic calorimeter (ECAL) using layers transverse to the beam axis either of silicon pixel or scintillation strips for sensors and Tungsten as absorber.
- An Hadronic calorimeter (HCAL) with a high granularity using steel or tungsten absorbers. Three technologies are under study : an analog, a digital or a semi-digital readout.
- The coil and a yoke to channel the magnetic field (4-5 Tesla) and track muon particles with scintillator strips.

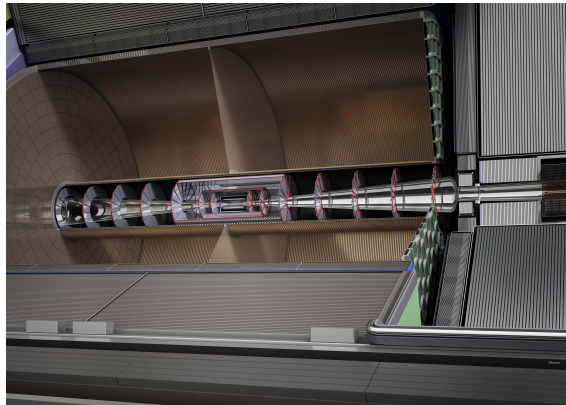


Fig. 1.2: Overview inside the ILD detector showing the vertex detector and the Track Particle Chamber (TPC).

1.3 The Analog Hadronic Calorimeter

The Analog Hadronic Calorimeter (AHCAL) is one of the concepts designed for the ILD (Fig. 1.3) and is actually in development at DESY. This calorimeter is based on an analog readout using scintillator tiles segmented in layers of $3 \times 3 \text{ cm}^2$ individually and read out by a silicon photomultiplier (SiPM). This segmentation is used to achieve the maximum resolution in energy and separation of individual particles in a shower. A full layer is specified to be 18 mm thickness, 10 mm of tungsten, 3 mm for the tile and only 5 mm for the electronics. All the tiles are read out individually. Over 4 million channels, integrated electronics is the only way to read out so many channels efficiently.

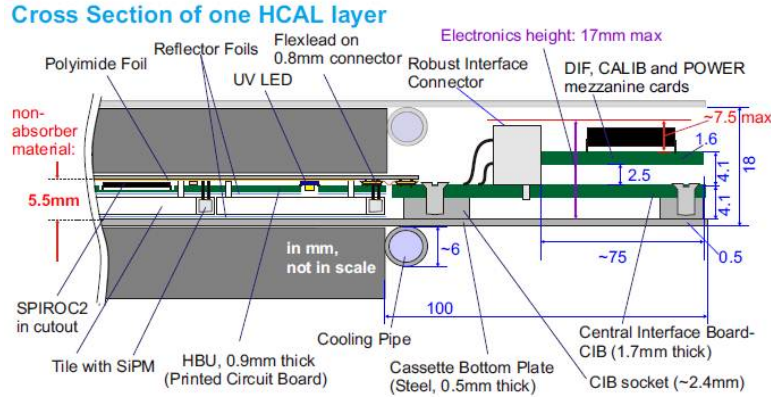


Fig. 1.3: Scheme of the actual layout for the AHCAL.

1.4 The AHCAL Design

The integration design is to use 48 layers of absorbers and between them the readout electronics. For this the SPIROC ASIC, capable to readout SiPM signals, has been designed at the LAL in France. It is capable of reading 36 SiPM with an auto-trigger mode, an high and low gain to cover a large range of fired silicon pixels and a TDC (time measure) designed for 100 ps resolution. The electronic layer is composed of 6 HBUs (called slab) in length per layer, hosting 24 SPIROCs so in total 2592 tiles. The main revolution is the power pulsing which enables to reduce the power consumption. We expect to achieve a power consumption of $40 \mu\text{W}$ per channel. The HBU also has onboard a light calibration system (LCS) using LEDs to calibrate each SiPM (equalization of the response in order that all the channel have the same gain).

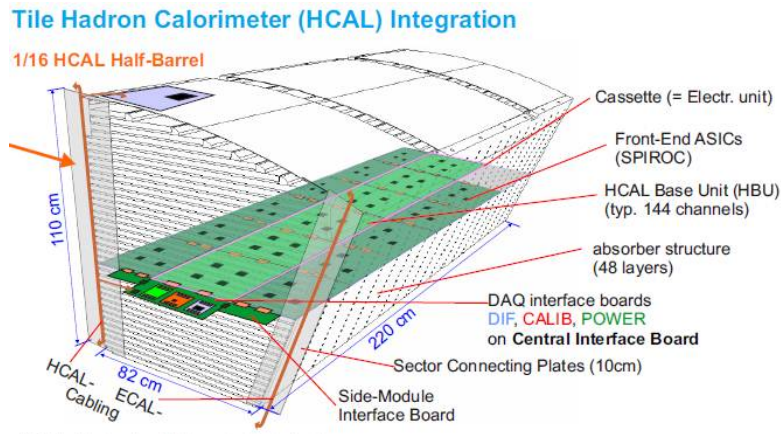


Fig. 1.4: Mechanical Design for the AHCAL.

2 Measurement on the TDC

2.1 Why a time measurement ?

The time measurement can be used to improve the performance of the AHCAL in combination with the high granularity and particle flow algorithms. An hadronic shower is not instantaneous as an electromagnetic shower, its propagation is slow due to neutral hadrons for example thermal neutrons which can stay in the calorimeter for several seconds without interaction. The design of the AHCAL permits to have a timestamp on each tile. By applying time cuts overlapping showers can be separated during reconstruction (Fig. 2.1).

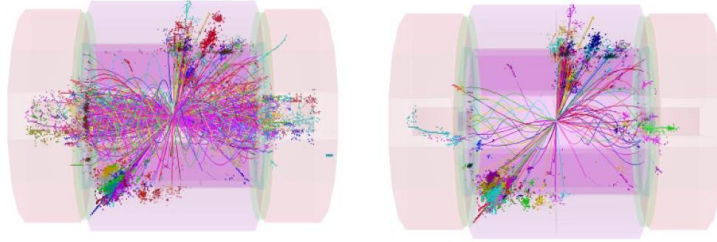


Fig. 2.1: Simulation of an event. The picture on the left is the event in total. The picture on the right is applied with a time cut of 5 ns.

2.2 Working Principle

The TDC on the SPIROC chip (Fig. 2.2) is realized by a capacitor which is charged with a constant current, the capacitor voltage increases linearly. Then when the trigger fires, the current is switched off. The voltage of the ramp is a direct measure for the time which can be read using an ADC. At each clock cycle, the ramp is reset and this creates a dead time in the TDC. To avoid that, two separate ramps are used (Dual TDC) which are activated at alternating clock cycles. The switch between the two ramps is done by a multiplexer.

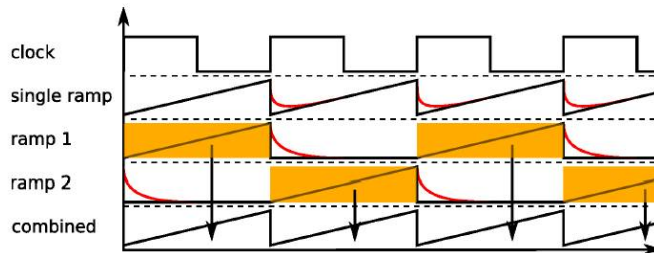


Fig. 2.2: Principle of the TDC dual ramp in SPIROC. A multiplexer is switching between the two ramps.

2.3 The TDC modes in SPIROC

Two modes are available in SPIROC, the ILC mode and the testbeam mode. These modes differ principally by the used clock frequency. The switching between the modes can be done in the slow control file of each ASIC.

- ILC mode :

The ILC mode uses a 5 MHz clock (200 ns ramp length), it is designed to fit for the time between the bunch of lepton in the ILC. The TDC design resolution is about 100ps.

- Testbeam mode :

The testbeam mode uses a 200 kHz clock (5 μ s ramp length) but can be chosen. A long ramp is used because the beam has no fixed bunch structure and the objective is to reduced the dead time to maximize the amount of data taken. The design resolution in that case is 1 ns.

2.4 Setup for the time resolution measurement

The setup (Fig. 2.3) is composed of one HBU with 4 SPIROC2b chips. The HBU has a detector interface board which controls the ASICs (provide clock frequency, external trigger...) and also the data acquisition by USB interface. To configure the board, a Labview software creates each slow control files (configure the chip) for the ASIC and calibrates the board. For injecting a charge into the chip, a pulse generator can deliver a pulse synchronized to the clock, which properties (width, lead, traling, amplitude..) can be changed.

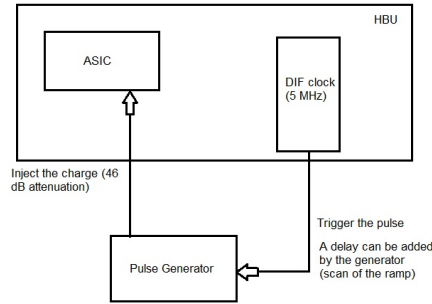


Fig. 2.3: Simplified Scheme of my experimental setup.

For most of the measurements, 100 cycles and 16 triggers were used for having a good statistical distribution.

2.5 Definition of the resolution

The main important goal of the measurements is to quantify the resolution of the TDC. The total resolution is defined as :

$$\sigma_{tot} = \frac{\sqrt{\sigma_{histo}^2 + \sigma_{fit}^2}}{slope_{fit}}$$

σ_{histo} represents the statistical fluctuation of all the histograms of all the measurements. σ_{fit} is the standard deviation of the fit from the data. $slope_{fit}$ is used to convert the resolution from a TDC value to a time value in nanoseconds.

2.6 Measurements on the TDC

2.6.1 ILC mode TDC ramp

For this measurement, the SPIROC chip is set to auto-trigger mode. By variation of the delay between trigger and pulse output on the pulse generator, a scan of the TDC ramp can be done. The delay was done in steps of 5-10 ns.

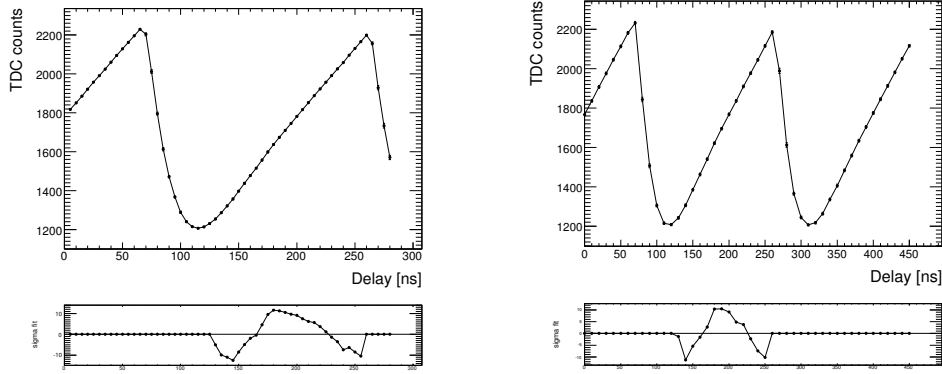


Fig. 2.4: Measurement of the TDC ramp for channel 3 and 4.

These plots (Fig. 2.4) show the TDC ramp for two different channels. Despite the multiplexer, one can see a long non-linear region corresponding to a deadtime (no time measurement valid). On the first view, the ramps seem to be straight and can be fitted to determine the resolution of the ramp. A closer inspection reveals a kink roughly in the middle of the ramp.

The ramps were fitted by several methods (all the ramp or the lower part or the upper part of the ramp). Because as we can see on the plots, the ramp is not a straight line but has a curvature around the middle thus decreasing the resolution. An overview is given in the table below :

Statistical error : $\sigma_{stat} = 0.151$

Channel	Ramp	Part	σ_{fit}	Slope	σ_{tot} [ns]
3	1	lower	1.60	7.65	0.21
3	1	upper	1.12	7.03	0.16
3	2	lower	0.87	7.42	0.12
3	2	upper	0.54	6.80	0.08
3	1	all	3.20	7.35	0.436
3	2	all	2.52	7.14	0.354
4	1	all	0.67	6.91	0.1
4	2	all	3.15	7.33	0.43
4	2	lower	2.6	7.75	0.34
4	2	upper	0.76	7.01	0.11

Table in ILC mode for channels 3 and 4.

As we can see most resolutions are in the range of 0.15 - 0.35 ns when fitting the upper or lower part of the ramp, which is still far from the designed resolution. The main factor is the σ_{fit} which means that one way to improve the resolution is to increase the ramp slope.

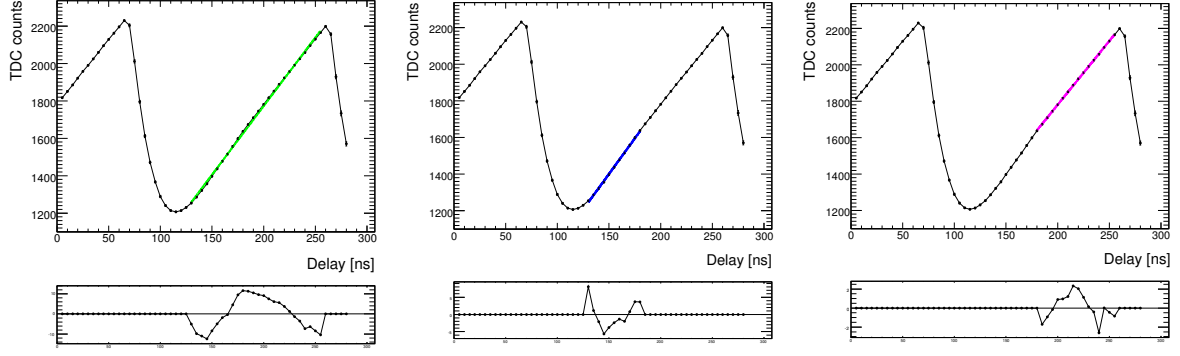


Fig. 2.5: Several plots with the fitting function as : $y(x) = a * x + b$. As we can see on the residues plots, the ramp is not straight therefore decreasing the resolution.

Moreover, there is nothing specific to tell on which ramp we take the measurement. Maybe except with the parity of the Bunch Crossing ID (BunchXID) if it is odd or even number because at each start ramp signal a BunchXID is generated. But this number seems to be not reliable at the beginning and the end of the ramp (Fig. 2.6). As the ramp 1 and 2 have slightly different slopes, this adds an uncertainty thus decreasing the resolution further.

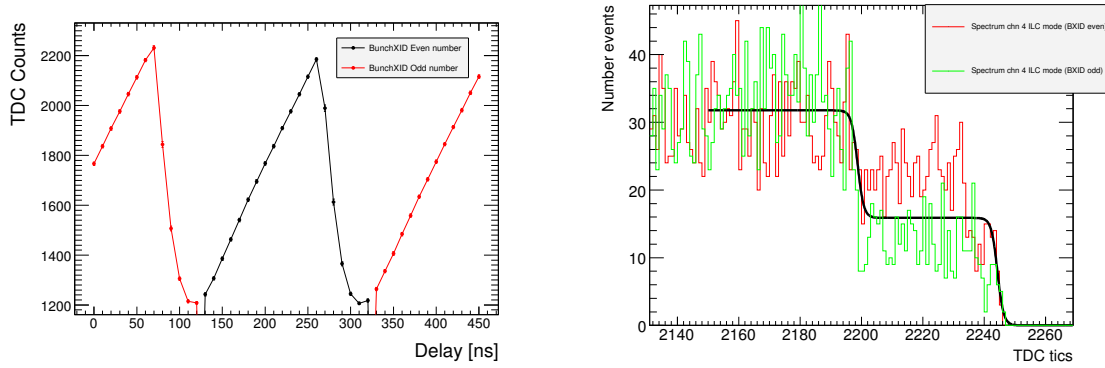


Fig. 2.6: The plot on the left is the TDC ramp filtered with the BXID. As we can see, normally we could separate the two different ramps by this number. But the plot on the right shows the higher part of the TDC spectrum using the filter. This plot shows that the BXID seems to be not well defined at the end of the ramp.

2.6.2 Spectrum ILC mode

For this measurement, the pulse generator is set to fire random distributed pulses into the chip. We obtain a TDC Spectrum (Fig. 2.7). A spectrum can highlight some characteristics of the ramp as the different heights between the two ramps. This difference can be easily fitted by a double step function.

In this case, the pulse generator does not have a random trigger mode but in auto mode with a distance between pulses more than the length of a ramp is enough if in the DAQ software the distance trigger is high enough to get a least one trigger.

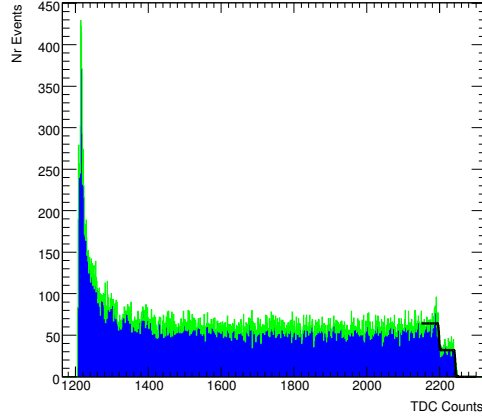


Fig. 2.7: TDC Spectrum of the channel 3 in ILC mode.

This spectra shows two characteristics. The influence of the deadtime and the ramps heights. As shown on the plot, there is lots of events in the first part, these events are in the deadtime (about 35% of the ramp length). This demonstrate that in ILC mode the deadtime is not negligible and reduces the dynamic range usable. The different height between the ramps seems to be the same for all the channels including a certain uncertainty. The ramp height differs up to 45 TDC counts (so around 5 ns of length difference).

2.6.3 Improvement of the slope

As said in the section above, in order to improve the resolution, the slope of the ramp must be higher. On the HBU, a bias point is responsible for the ramp slope for all channels. So soldering a resistor on this point increases the current therefore increasing the slope and also the dynamic range of the TDC.

For the measurements, different resistors from 30 k Ω to 8 k Ω were soldered. A resistor below 5 k Ω cannot be used because the current would be too high and would damage the chip.

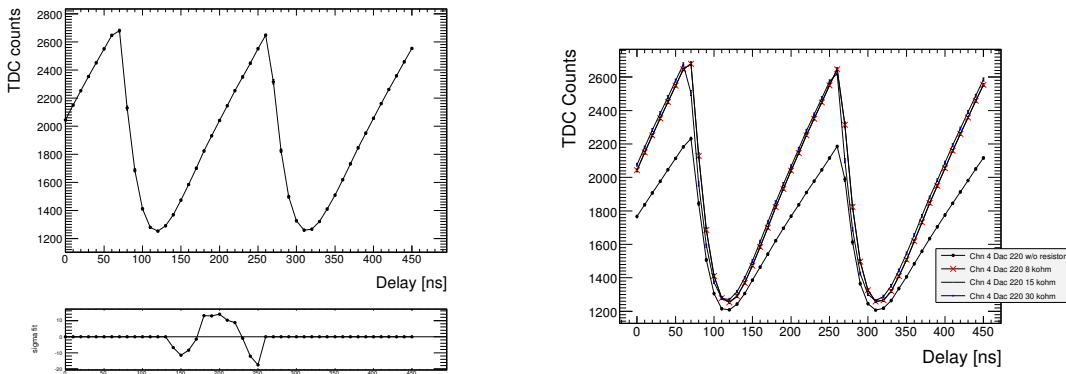


Fig. 2.8: A 8k Ω resistor has been soldered on the left plot, we can see that the slope of the ramp is more deep and also the dynamic range is about 1200 ADC tics. The right plot shows a comparison between the ramp in function of the value of the resistor.

As we can see (Fig. 2.8), on the right plot, all additional resistors lead to very similar slopes, which is larger than without resistor. By interpolation, a resistor between an 'infinite' value and $30\text{k}\Omega$ would give a slope between 7 and 10.5 TDC/ns .

Here is a table for the different values of resistor :

Statistical error : $\sigma_{stat} = 0.156$

Statistical error : $\sigma_{stat} = 0.197$

Channel	Ramp	Part	σ_{fit}	Slope	$\sigma_{tot}[ns]$
4	1	lower	0.13	11.33	0.018
4	1	upper	1.87	10.38	0.18
4	2	lower	0.2	10.30	0.02
4	2	upper	2.36	10.24	0.23
4	1	all	2.00	10.84	0.19
4	2	all	3.44	10.46	0.33

Channel	Ramp	Part	σ_{fit}	Slope	$\sigma_{tot}[ns]$
4	1	lower	2.5	11.32	0.22
4	1	upper	2.01	10.22	0.19
4	2	lower	2.95	10.63	0.28
4	2	upper	1.58	10.08	0.16
4	1	all	4.03	10.79	0.37
4	2	all	2.65	10.43	0.25

Fig. 2.9: Table with the total resolution. The left table is for a $8\text{k}\Omega$ resistor, the average resolution $\sigma_{tot} = 0.20\text{ ns}$. The right table is for a $30\text{k}\Omega$ resistor, the average resolution $\sigma_{tot} = 0.25\text{ ns}$.

2.6.4 Testbeam mode TDC ramp

For this measurement, the same setup is used as in ILC mode. The difference is between the clock frequency of the DIF which changes from 5 MHz to 200 kHz (the frequency can be adjust as we want). This means that the ramp length is up to $5\text{ }\mu\text{s}$.

A frequency of 250 kHz has been chosen to do a first measurement. The delay was done in 200 ns steps.

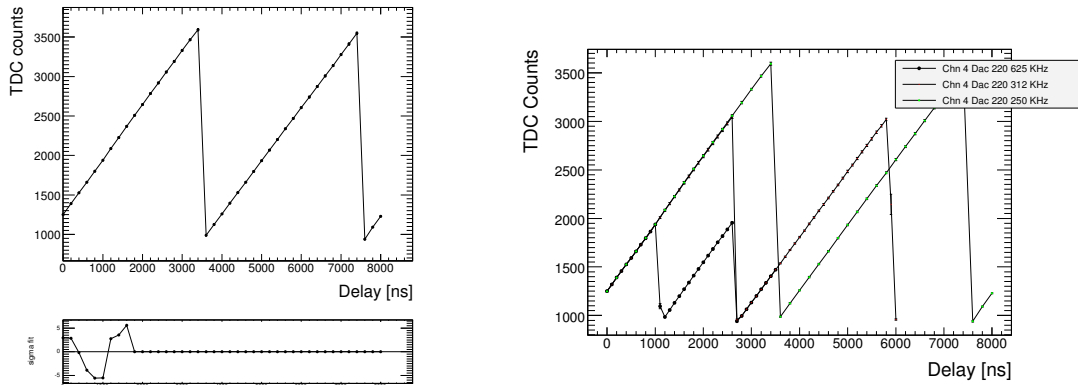


Fig. 2.10: The left plot is the TDC ramp of channel 4 in Testbeam mode (250 kHz). The relative deadtime (falling of the ramp) is smaller than in ILC mode because of the ramp length which is longer. The dynamic range is bigger (2000 TDC ticks). The right plot shows a comparison of the ramp depending of the frequency of the clock chosen. The lower the frequency is lower the larger the ramp is and larger is the dynamic range.

Then the same measurements were done but using different frequencies in order to choose an optimal clock frequency.

As we can see (Fig. 2.10), on the right plot, related to the frequency, the dynamic range used is less than 1000 TDC ticks for the high frequency up to more than 2000 TDC ticks for the frequency of 250 kHz . A frequency higher than 200 kHz has to be kept in order to improve the resolution by soldering a resistor in the slope bias point and avoid a saturation of the TDC.

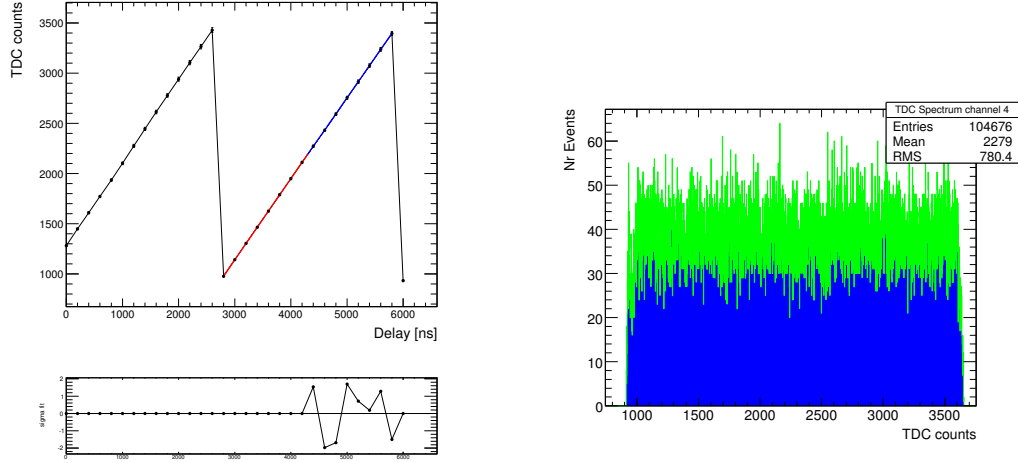


Fig. 2.11: The left plot is the TDC ramp of channel 4 using a frequency of 312 kHz and with a resistor of 120k Ω soldered to the slope bias point. The right plot is the spectrum of the TDC in Testbeam mode. As we can see, the spectrum is flat indicating that the deadtime (70 ns) is negligible.

Then as in ILC mode, a spectrum of the ramp (Fig. 2.11) was done using a frequency of 250 kHz without any resistor soldered to a bias point.

The spectrum is completely flat indicating that there is no deadtime (or it is small relative to the length of the ramp). And also both ramps seem to have the same height.

Then, as in ILC mode, the ramp was fitted by a linear function taking into account that the pulse generator used had a problem when a delay of 2 μ s was used (jump in the accuracy). Here is a table regrouping the results for the testbeam mode :

Frequency : 250 kHz

Statistical error : $\sigma_{stat} = 0.16$

Channel	Ramp	Part	σ_{fit}	Slope	σ_{tot} [ns]
4	1	lower	1.06	0.698	1.53
4	1	upper	0.39	0.682	0.61
4	2	lower	0.59	0.674	0.91
4	2	upper	0.51	0.671	0.79
4	1	all	2.92	0.695	4.21
4	2	all	0.49	0.673	0.78

Frequency : 625 kHz

Statistical error : $\sigma_{stat} = 0.216$

Channel	Ramp	Part	σ_{fit}	Slope	σ_{tot} [ns]
4	1	lower	0.52	0.685	0.83
4	1	upper	0.91	0.687	1.36
4	2	lower	0.60	0.711	0.89
4	2	upper	0.40	0.681	0.67
4	1	all	0.91	0.683	1.37
4	2	all	1.59	0.694	2.31

Table result in testbeam mode for different frequencies : 625 kHz and 250 kHz. The overall resolution for the TDC in testbeam mode is around 1-1.5 ns.

The design resolution seems to be achieved but we have to look in detail for improving the linearity of the ramp and the dynamic range thus the resolution to achieve a goal

under 1 ns.

2.7 Resolution

In this part, we focus on the best compromise we could choose for the TDC ramp. One of the most important part is the deadtime, in fact we don't want a long deadtime because for every event recorded in this period, the time information is lost. Because of the design of the chip (use of a multiplexer between the dual ramp), the deadtime is relatively constant around 70 ns. Which in ILC mode, correspond to about 30% of the ramp length. For the testbeam mode, the deadtime is determined by the frequency we use. The plot (Fig. 2.12) shows the relative deadtime versus the frequency.

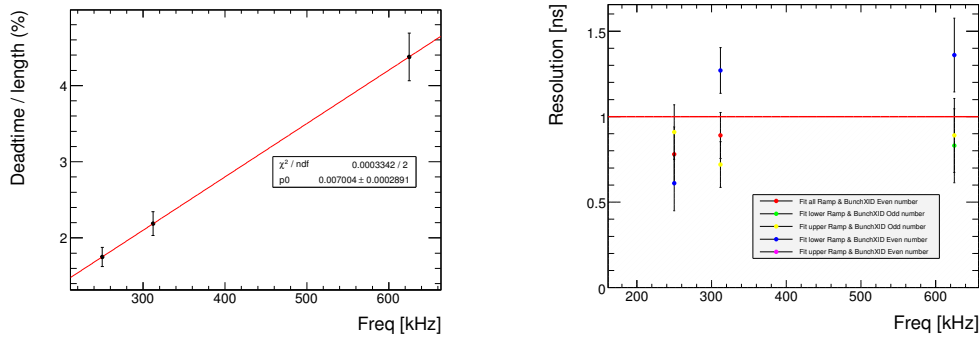


Fig. 2.12: The left plot shows the dependency of the clock frequency and the relative deadtime. The choice of a smaller frequency enables a deadtime around 1%. The right plot shows the resolution versus the frequency, for a clock of 250 kHz the resolution achieved is less than 1 ns.

Then what we have to take in account is the resolution of the ramp and also the dynamic range usable. The plot above shows the resolution in testbeam mode relative to the frequency. As we can see, the best compromise seems to use a frequency lower than 312 kHz because the deadtime is around 2-2.5% of the ramp and the resolution around 1-1.5 ns while conserving a good dynamic range for the TDC (1500-2000 TDC tics).

2.8 Conclusion

In this part, measurements have been performed on the linearity and resolution of the TDC ramp.

In ILC mode, the overall resolution is around 100-250 ps determined by fitting both ramps in two parts with a linear function. Due to a kink in the middle of the ramp, one linear fit does not give good results. The spectrum measurements give a direct measure of the different height between the ramp and can be fitted. The difference is around 50 TDC tics which of course decreases the resolution and it cannot easily be corrected for because we can't distinguished the ramp and know the origin of the measurement.

In testbeam mode, an average resolution of 1-1.5 ns has been achieved which is close to the design resolution for this mode. A comparison has been done between different frequencies to have the best compromise between deadtime, resolution and dynamic range. Also a measurement has been done while increasing the ramp slope which gives a better resolution and thus could achieve a resolution better than 1 ns.

3 The Time Walk effect

This part is focused on a problem we encounter on the SPIROC chip concerning the time measurement.

3.1 What is this effect ?

The effect called Time Walk is an effect in the chip concerning the slow shaper (Fig. 3.1). The slow shaper is used for shaping the signal arriving from the SiPM, it shapes the signal in order that the maximum of the signal is on the Hold time value (Value when the chip can do an amplitude measurement). But the shape of the signal depends on the amplitude. In fact, high amplitude signals have to be shaped faster than low amplitude signals to arrive at the maximum at the same Hold time. Because of that, a high signal passes the threshold before a low signal and thus there is a time difference between the trigger.

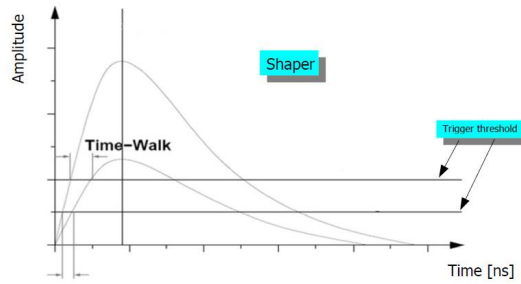


Fig. 3.1: Scheme of the time walk effect.

3.2 Measurements with charge injection

The main part of my work was focused on the characterization of this effect in order to incorporate it into the simulation and digitization.

3.2.1 ILC mode

For this measurement, the pulse generator is still triggered by the DIF board and connected to a channel on the HBU. The ASIC is set to auto-trigger mode and by variation of the voltage of the pulse (so the amplitude), the time walk can be measured by plotting the TDC value (time) as a function of the ADC value (Amplitude). This measurement was done for several channels.

As shown in Fig. 3.2, the different channels seem to have a different shape for the time walk indicating that we can't use a single function with the same parameters for all channels to characterize this effect. Also, there is an offset channel to channel and because of this the channels can't be compared directly in time. This channel-to-channel variation was not expected at first and implicates that we have to correct this first in order to compare time trigger between channels.

The fitting is done using an inverse function with 4 parameters :

$$Time = [0] + [1]/(ADC^{[3]} - [2])$$

[0] is the time offset, [1] the curvature, [2] is an ADC offset and [3] is a polynomial parameter.

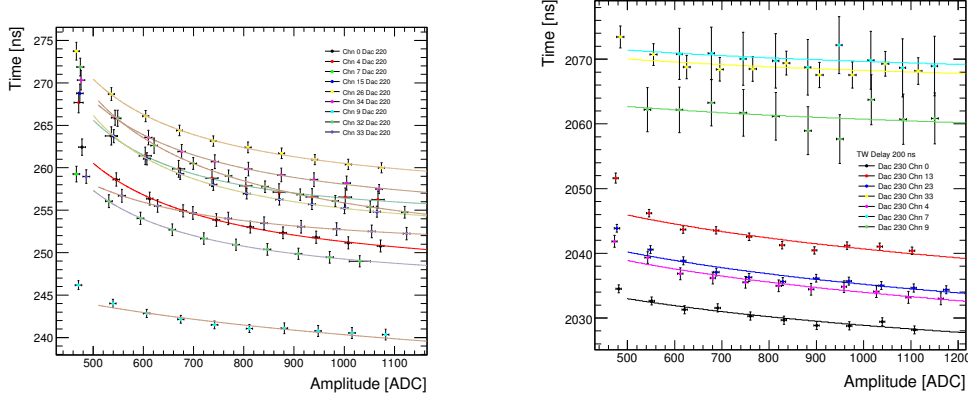


Fig. 3.2: The time (TDC) versus the Amplitude (ADC) for several channels, determined with charge injection. The left plot is done in ILC mode. And the right plot in testbeam mode (errors bars divided by a factor of 10). The absolute time values have an arbitrary offset, the important is the relative offset between the channels. As shown on the plots, the offset channel to channel seems to be much larger in testbeam mode than in ILC mode.

ILC mode :

Channel	[0] (ns)	[1] (ADC.ns)	[2] (ADC)	[3]	χ^2
0	246.074	6520	283.892	1.06	0.09
4	254.109	5.66e6	84320	2.13	0.11
7	245.258	8155	472.47	1.13	0.06
15	251.018	31010	1532.75	1.32	0.02
26	255.386	5324	292.758	1.04	0.18
34	252.865	9199	390.991	1.11	0.12
32	246.138	518	30.72	0.64	0.05
33	250.281	182357	1342.51	1.63	0.06

Table Results of the fitting in ILC mode.

3.2.2 Testbeam mode

The same setup as in ILC mode is used. The only difference is that the clock frequency of the chip is set to 250 kHz (ramp length of 4 μ s). On the plot (Fig. 3.2), the effect is the same as in ILC mode but the errors bars on the plot are huge. That is why, an investigation of the origin of this was done. The first idea was to look at the histogram of each memory cells in order to see if there is a difference between the TDC value of all memory cells.

Testbeam mode :

Channel	[0] (ns)	[1] (ADC.ns)	[2] (ADC)	[3]	χ^2
0	1032.16	1025.52	0.013	0.006	4.35
13	1042.9	1034.43	0.016	0.007	11.63
23	1039.19	1031.02	0.015	0.007	9.86
33	1042.43	1032.63	0.01	0.002	1.56
4	1037.96	1013.96	0.03	0.007	3.17
7	1044.39	1032.97	0.009	0.002	0.43
9	1040.84	1027.92	0.011	0.003	1.87

Table Results of the fitting in Testbeam mode.

3.2.3 Investigation on the memory cells

In SPIROC, each event is stored in a memory cell. As in the acquisition software the number of events (or number of trigger) can be chosen, further an event by event analysis can be done. In this case, an amplitude around the MIP signal (voltage of 0.6 V) was chosen. Here (Fig. 3.3) are the histogram obtained for two different channels in testbeam mode.

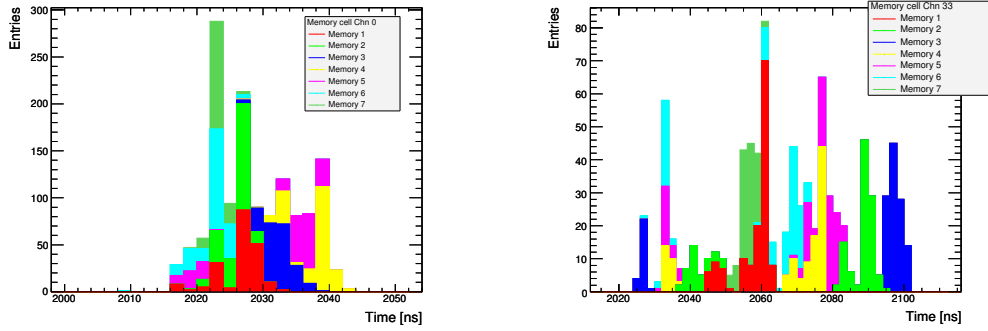


Fig. 3.3: These plots show the distribution of the time (TDC) on two different channels. Each color corresponds to a different memory cell. For some channels the distribution is wider leading to an increase of the error on the mean value.

As we can see on these plots, there is a spread of the TDC value due to the memory cell which does not have the same value for all channels (including the RMS). Also we can notice that the effect is more important on some channels (like in this case for channel 33). This means that for the timing correction, the memory cell spread and the offset channel to channel has to be taken into account.

3.3 Measurements with the Light Calibration System (LCS)

In the AHCAL prototype, there is a calibration system using LED pulses. This calibration system is used for setting the right pre-amplifier setting for each channel in order to achieve the same overall gain for each channel. This setting is the most important part of the calibration of the system, it should be corrected set in order to have the best gain on all channel and distinguish a single pixel spectra from the LED. The LED sends a pulse into the scintillator tile and the light is detected by a silicon photo-multiplicator. The amplitude of the LED pulse is controlled by the DAQ software (max 10 V).

3.3.1 ILC mode

For this measurement, different voltages for the LED were applied (corresponding to different amplitude) then the TDC value depending on the amplitude has been studied.

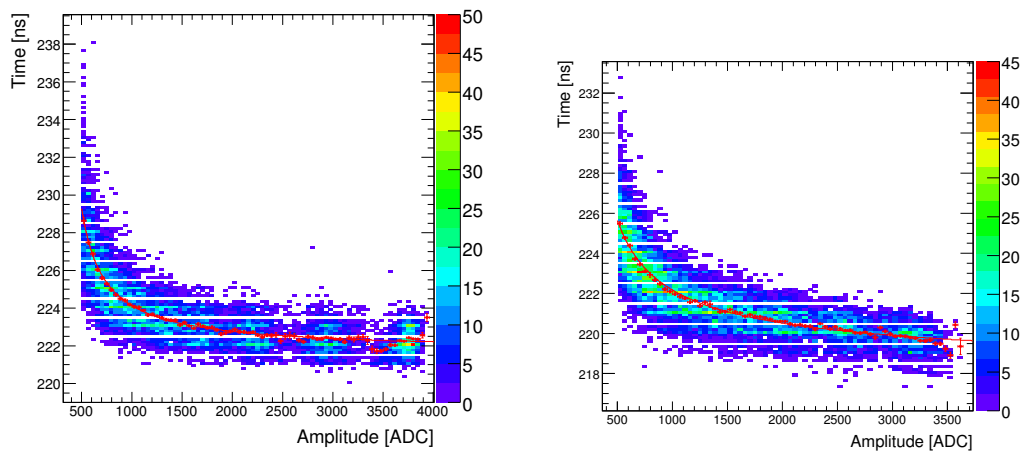


Fig. 3.4: Time as a function of the Amplitude on two different channels in ILC mode, measured with the LED system. Even with the LED system, there is this tendency that the time increases at low amplitudes. Notice that there is a spread around the mean, this spread is probably due to the fact that the amplitude of the LED pulse is not always constant and also that the trigger logic of the LED can have a small delay on each pulses explaining this spread.

The behavior (Fig. 3.4) is the same as charge injection. There is just a spread around the mean value of the histogram. This spread is due to the fact that the LED pulse has not always the same amplitude but there is a fluctuation in the voltage inducing the spread. Also the spread is maybe related to the fiber and the 'time constant' of it. This time constant has an impact on the SiPM pulse which make the width of the pulse longer than a normal SiPM pulse (around 30 ns against 5-10 ns).

3.3.2 Testbeam mode

The same setup is done in testbeam mode. As shown in Fig. 3.5, the spread on the plot is much larger than in ILC mode. This is due to the fact that in testbeam mode, the TDC ramp has a low slope (less than 1 TDC tics/ns) which makes it more sensitive to noise and also the memory cells offset which can make the spread larger.

Then a timing correction procedure for several channels including the memory cell problem has to be found. This correction will be used for the testbeam at CERN in November with 4 new HBU received at the beginning of August.

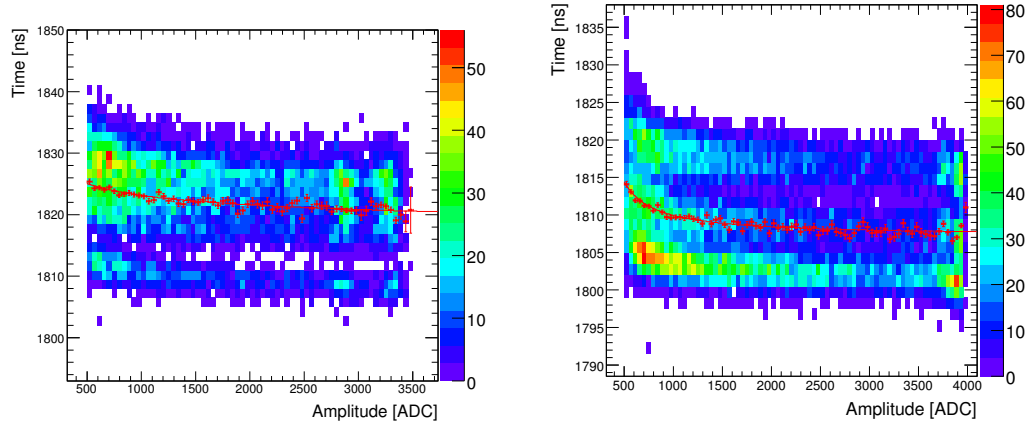


Fig. 3.5: The same as Fig. 3.5 but in testbeam mode. These plots highlights that in testbeam mode, the spread is much wider mostly because of the slope of the TDC ramp which is smaller than 1 TDC/ns therefore more sensitive to noise.

3.4 Correction procedure

This procedure was developed and tested with the data I have measured. To build a procedure which is working, data from several channels was taken. The procedure is illustrated in Fig. 3.6. A fit for each memory cell for a channel is done (upper left) and then the average curve is built (lower left). Like that an average offset for a channel is calculated then this procedure is repeated on several channel (upper right). This procedure has to be efficient and fast to achieve a good resolution in time and be applied to a full layer of 4 HBU (i.e. about 600 channels...).

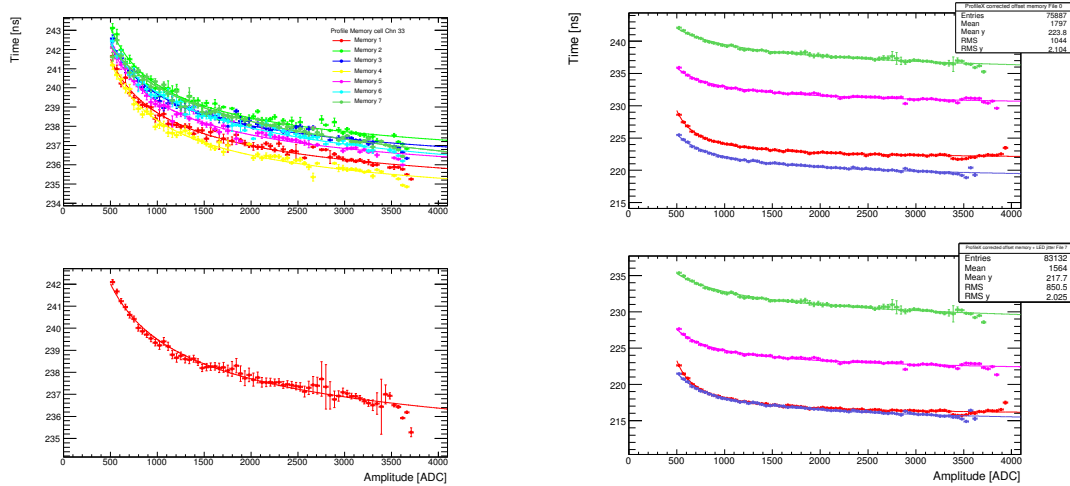


Fig. 3.6: Plots representing the correction procedure. First, an analyze of the spread of the memory cells on a channel (upper left) then building the average (lower left). Finally applying this procedure to several channel in order to calculate the channel to channel offset (upper right). Taking into account an effect of the LED system, the trigger of the pulse and the actual pulse is not at the same time on all channel thus this value needed to be calculate and subtracted (lower right) given by a table done by Wuppertal on one HBU, see below.

In fact, this jitter corresponds to a time delay between the trigger of the LED pulse and the actual pulse. Here (Fig. 3.7) is a map measurement done on one of the new HBU,

as we can see the delay variate from 0 ns to 10 ns.

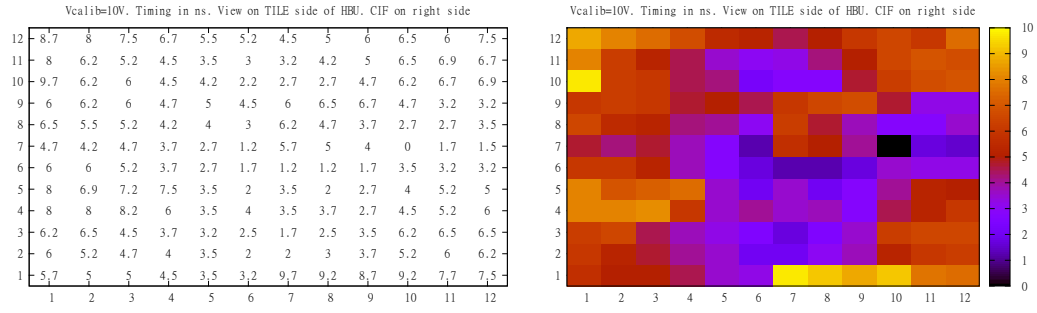


Fig. 3.7: Table of the LED jitter between the LED trigger and the pulse. This was done by some colleagues at the University of Wuppertal.

Then the timing correction procedure enables us to calculate each offset between the channel and give us a lookup table for each chip, each channel on each HBU.

Here is the lookup table for the 4 channels analyzed :

Chip	Channel	Moy_offset	LED_Jitter	Offset_corrected
0	0	221.585	6	215.606
0	23	228.006	8.3	219.634
0	33	229.488	6.7	221.523
0	9	217.145	4	212.586

This procedure needs to be extend to a complete HBU giving a lookup table for each HBU.

4 Conclusion

4.1 General Conclusion

I worked during 3 months at DESY during the summer student program, in this report my work is presented. Some measurements have been performed on the linearity and resolution of the TDC and the time walk effect in SPIROC2b. The measurements have been done using charge injection and the light calibration system (LCS).

Concerning the measurements on the TDC, in ILC mode, a resolution of 150-200 ps is achieved by fitting the TDC ramp in two parts with a linear function. The ramp is not straight enough to have a good resolution using one fit (a kink is present in the middle, probably due to a bias point instability). Doing a spectrum of the TDC, a height difference between the ramp can be noticed and fitted. Also because the TDC uses a dual ramp with different heights, the resolution is decreased as long as there is no sure way to distinguish the ramps. By soldering a resistor on the bias point of the slope, a better dynamic range is used and a better resolution is achieved close to the design resolution.

In testbeam mode, an average resolution of 1-1.5 ns has been achieved. Using the same fit method because of a shift in the timing of the pulse generator around 2 μ s. A comparison between the frequency to use has been done and shows that a frequency around 250 kHz is a good compromise between dynamic range and relative deadtime. Also a resistor can be soldered to the bias point in order to increase the resolution. The TDC spectrum shows no apparent features. A performance around the design resolution of 1 ns is achieved and could be improved by increasing the ramp slope.

In a second part, the time walk effect in SPIROC2b has been analyzed. This effect has been studied in both modes using charge injection and the LED calibration system. In ILC mode, with charge injection, the time walk effect seems to be characterized by an inverse function. The measurements were done on several channels in order to see if one parametrization could be use. As the plots show one function with the same parameters cannot describe all the channels and also because of this offset, the channels cannot be compared. The spread between the channel is around 30 ns. In testbeam mode, this effect seems to be larger the spread is around 45 ns and also the error bars are huge on some channels. This effect has been investigated and revealed a memory cell offset that has to be corrected too.

Finally using the LED Calibration System, a timing correction procedure has been prepared. This procedure corrects the memory cell offset, an LED jitter between the pulse and the trigger and calculates the channel to channel offset. This procedure has to be fast and accurate in order to conserve a good resolution for the time.

4.2 Outlook

A testbeam is on schedule for November at CERN therefore the calibration for the 4 HBUs has to be done. We dispose of 8 weeks of testbeam at DESY in order to calibrate all the channels (around 600). The MIP calibration for all the channel has to be done. Time calibration using the LCS can be cross checked using a lead plate in front of the beam to generate an electromagnetic shower. Also an online monitor has been prepared and can be used in this period to debug it and be ready for November.

Appendix

A. Commissioning of the 4 HBU for testbeam at CERN

There is a testbeam planned at the SPS (Super Proton Synchrotron) at CERN for November 2012. The setup will consist of a layer placed at the end of the DHCAL (Digital HCAL) which is composed of 4 HBUs assembled in a square. Therefore we received 5 new HBUs. Four HBU were equipped with SPIROC2b and the last one with the prototype of SPIROC2c.

The commissioning is composed of several phases :

- Measurement and configuration of the Input DAC. This phase consist to configure the regulator for the voltage of each SiPM on each channel. Each SiPM has a definite optimum voltage (give by ITEP) but the board has only one power supply for all channels (about 50 V) so the input DACs enable to configure the voltage for each SiPM.
- Measure a SPS with 100 fF to determinate the original gain.
- The next phase is the pre-amplifier curve (Fig. 1). This is done channel-wise with the LCS. A curve is done to determine the gain in function of the pre-amplifier configuration. With this curve, we choose a gain, called the cell gain, in our case the gain choose is 26 ADC tics per pixel. Then we configure the pre-amplificator on each channel and do an LED run to check the gain by fitting a single pixel spectrum. This phase is very important because this allows us to estimate the ADC value corresponding to the MIP using the formula : $MIP = Gain * Light Yield$. So choosing a gain of 26 and the light yield is around 15 pixel per MIP, the MIP is around 400 ADC tics which we have to add the pedestal (around 200 ADC tics).

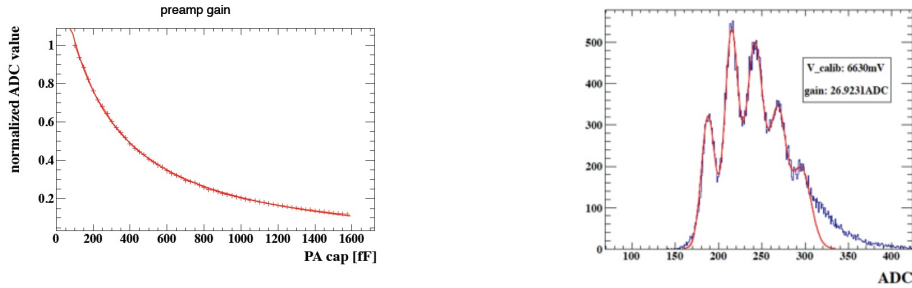


Fig. 1: The left picture represents the ADC value depending of the pre-amplifier capacitance (normalized to 100 fF). With this plot for all the channels, a gain is chosen (in our case the gain is 26) and determine the pre-amplificator for each channel. This is done in order to equalize the response of the SiPM. Then an LED run is done in order to check the gain by fitting the Single Photon Spectrum.

- Then the trigger threshold must be set. A compromise has to be done : low threshold for optimal efficiency and high threshold for low noise rate. In order to know this, a noise measurement on each board has to be done. Finally this give us the global threshold to use depending of the noise rate and the beam rate.
- After this we can send each HBU in testbeam (here at DESY) to measure a MIP spectrum and do some physics (timing of the shower, energy measurement...) and also the timing compensation can be done (test with the 4 HBUs...).

B. A new prototype : SPIROC2C

This chapter is focused on the new prototype for the ASIC : Spiroc2c. Some measurements have been performed in order to see if some problems encountered in the Spiroc2b has been solved.

First of all, we need to configure the chip correctly concerning the Hold time. This time has to be chosen correctly that the chip measures the voltage at the maximum of the amplitude. Thus we perform a holdscan. We can change 3 values in the slow control file of the chip, Trigger, Hold Value and Reset Column (called Delay cells). Here is the results shown above :

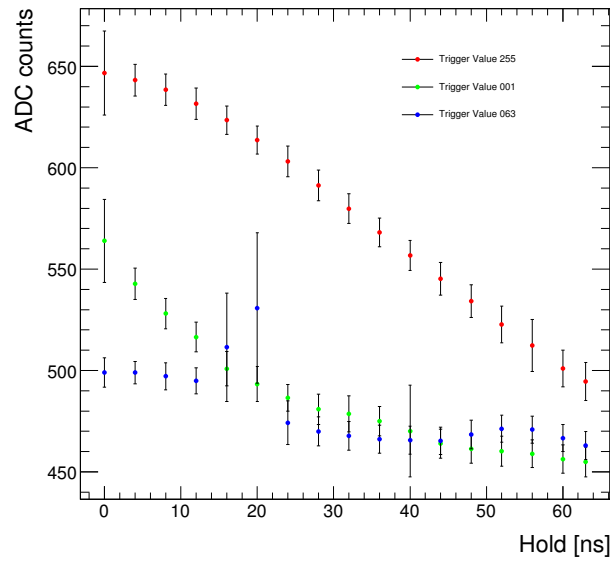


Fig. 2: Holdscan of the SPIROC2c. The trigger value is set to 1 and the Hold value and Reset Column are changed by step of 4 ns.

As shown (Fig. 2), there is a problem with this scan, normally we should be able to see the pulse after the slow shaper. But it seems that the maximum of the pulse is at the beginning, there must be some kind of shift done by the ASIC. Further investigations are needed to understand how this new prototype is working.

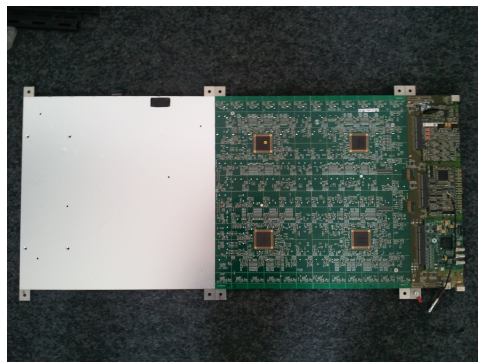


Fig. 3: Picture of the board with the SPIROC2c.

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