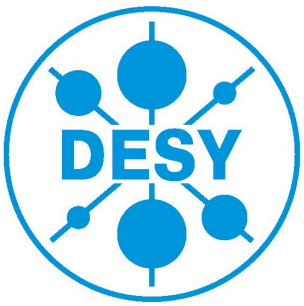

Investigation of the time measurement capabilities of the SPIROC2b ASIC

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Abstract

A basic prototype for an analog hadron calorimeter for a future linear collider detector is currently being developed by the CALICE collaboration. The aim is to show the feasibility to build a realistic detector with fully integrated readout electronics. In this report ADC and TDC measurements on the readout ASIC designed for implementation in the calorimeter are presented. The ADC response has been shown to be linear for wide ranges of input charge in both available gain modes. The TDC achieves a time resolution of $\sim 300\,\mathrm{ps}$ in ILC mode and $\sim 3\,\mathrm{ns}$ in testbeam mode. Also some ideas for further resolution improvements are given.

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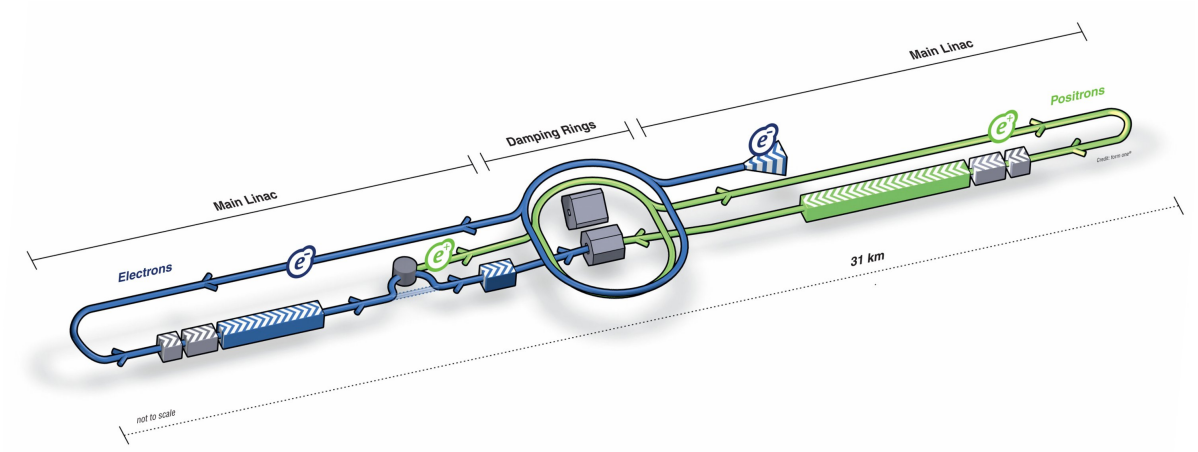


Figure 1: Schematic of the ILC beamlines.

1 Introduction

1.1 The International Linear Collider

The *International Linear Collider* (ILC) is a planned e^+e^- linear collider with a center of mass energy of 500 GeV or even 1000 GeV. The linear setup is needed, because the maximum collision energy in any reasonably sized ring is limited by the emitted synchrotron radiation. It is planned to be built in a 30 km long underground tunnel at a still to be determined location. Figure 1 shows a sketch of the current beamline design.

In opposition to the LHC located at CERN, which is a *pp* collider, the collision participants in the ILC will be leptons and thus have no (known) substructure. This greatly increases the achievable measurement precision, which is why usually lepton-lepton colliders are used to measure already known particles (i.e. the Higgs-Boson still to be found at the LHC) with great accuracy. Still a high power lepton-lepton collider can be used to find signs of new physics, although the maximum center of mass energy of a proton-proton machine is usually higher (by the time the ILC will be built, the LHC will most certainly run at 14 TeV).

It is planned to have two separated multi-purpose detectors at the ILC. As a linear collider naturally only has one interaction point, the two detectors have to be designed in such a way, that a fast switch between them is possible within a day. This is an enormous challenge on the engineering side, as the detector has to be put into place with sub-millimeter precision. The final focus magnets are part of the detector and require even higher precision in the nanometer region. At the moment there are two verified detector concepts, the **Si**ilicon **D**etector (SiD) and the **I**nternational **L**arge **D**etector (ILD).

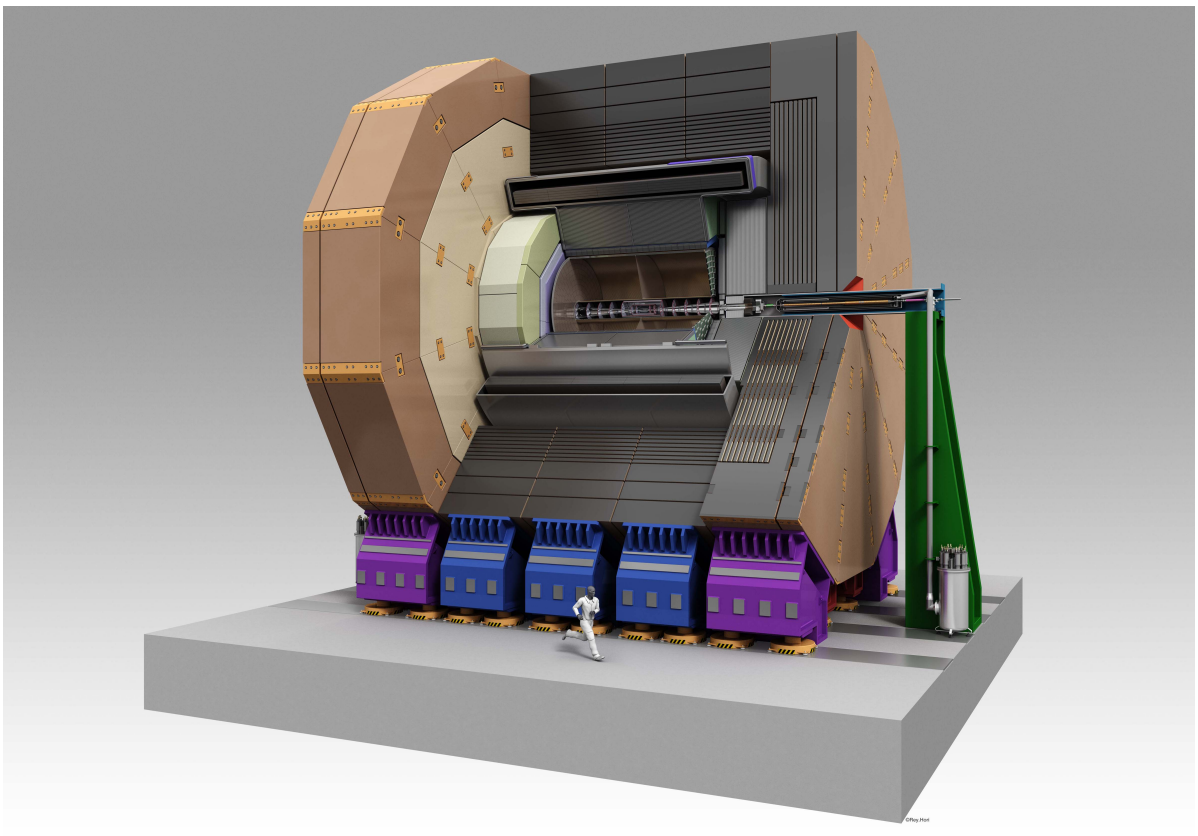


Figure 2: Cutaway schematic of the ILD concept.

1.2 The International Large Detector

As other large multi-purpose detectors like ATLAS or CMS, the *International Large Detector* (ILD) is designed to be a barrel shaped detector consisting of many specialised detectors layered around the interaction point. To achieve maximum energy resolution with the particle flow concept, the granularity in the calorimeters has to be as high as possible to trace single particles even in jets.

The most important parts of the ILD from the inside to the outside are ([1]):

- Five to six layers of silicon pixel detectors for maximum precision vertex tagging. (VTX)
- Two layers of silicon strip detectors around the VTX for improved tracking and to fill the gap to the TPC. (SIT)
- A large volume time projection chamber, optimized for maximum spatial resolution with up to 224 points per particle track. (TPC)
- An electromagnetic calorimeter with up to 30 samples transverse to the beam axis, either of Si-W or scintillator-W type. (ECAL)

- A very fine granular hadronic calorimeter using steel absorbers (for 500 GeV ILC) or tungsten absorbers (for a multi TeV machine like CLIC), two competing technology proposals with (semi-)digital and analog readout. (HCAL)

- The iron return yoke to channel the flux of the magnetic field and serve as a muon filter, equipped with scintillator strips on the outside to detect muons.

1.3 The Analog Hadronic Calorimeter

The ILD is designed to deliver jet energy resolutions of $\sigma_E/E \approx 30\%/\sqrt{E[\mathrm{GeV}]}$. To achieve this, it is needed to combine particle flow reconstruction with an extremely fine segmented (both transverse and parallel to the beam axis) ECAL and HCAL. The **A**nalog **H**adronic **CAL**orimeter (AHCAL) approaches this requirement by segmenting its scintillator layers into $3\times3\,\mathrm{cm}^2$ tiles individually read out by a silicon photomultiplier (SiPM) directly inside the tile.

In transverse direction each layer has 10 mm of W-absorber (16 mm in case of a steel absorber). The maximum thickness of one full layer including the scintillator and readout electronics is specified to be 18 mm for the tungsten version, which after subtracting 3 mm for the scintillator itself leaves only 5 mm for the electronics and all casing per layer.

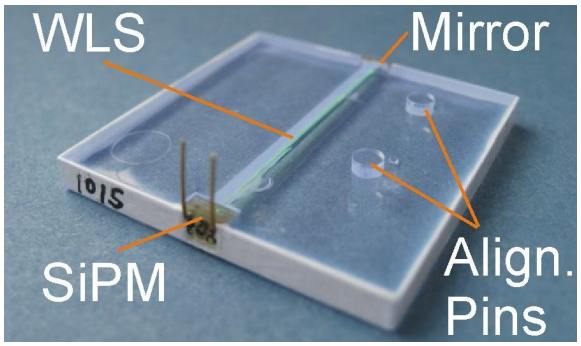


Figure 3: Tile with mounted SiPM.

1.4 The Engineering Prototype

To match these challenges the AHCAL engineering prototype (fig. 4 & 5) is in development at DESY. The goal is to create readout electronics capable of doing all the necessary A/D conversion fully integrated into the active layer while maintaining a power consumption of less than 25 μW per channel [3].

For that task the SPIROC ASIC for SiPM readout has been designed at LAL, France. It is capable of reading up to 36 SiPMs, has a built-in auto trigger, two different gain modes to cover the range from 1 up to 2000 fired SiPM pixels and a TDC with up to 100 ps designed time resolution. Each SPIROC has 16 analog memory cells per channel which are read out in the free time between bunchtrains.

The proposed setup consists of 36 cm×36 cm PCBs (**H**CAL **B**ase **U**nit) hosting 4 SPIROCs each for a total of 144 tiles per PCB. These PCBs can be coupled into strings of 6 to form a *slab*. The HBU also has an onboard LED calibration system with one SMD LED per scintillator tile to calibrate the gain of each SiPM via single photon spectra from short LED pulses.

SPIROC features covered further in this report are first the selectable preamplifier capacitors to compensate for differing gain in the SiPMs and the TDC in two modes of operation.

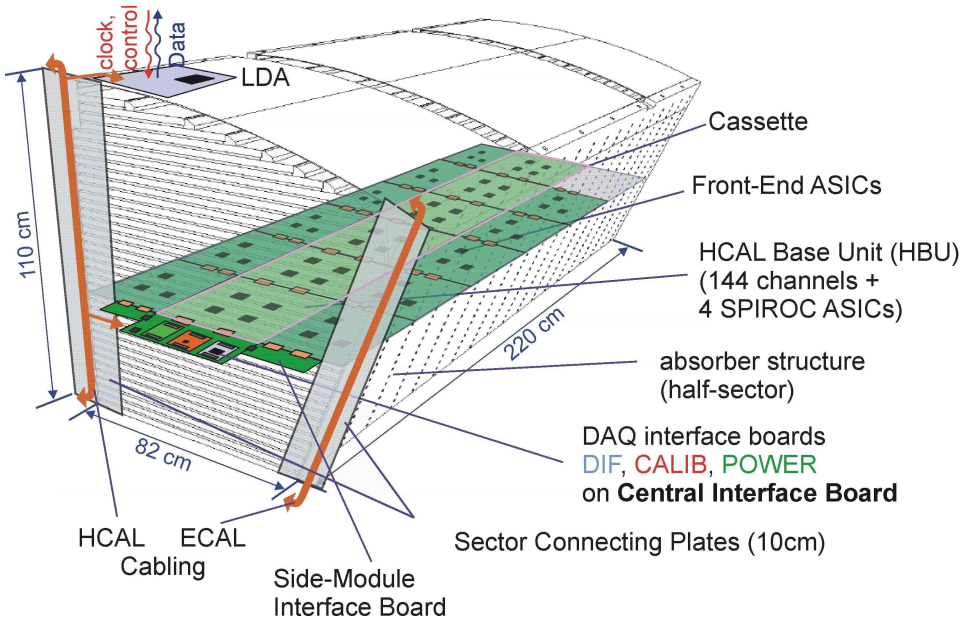


Figure 4: 1/16 AHCAL half-barrel with 48 layers containing three slabs each.

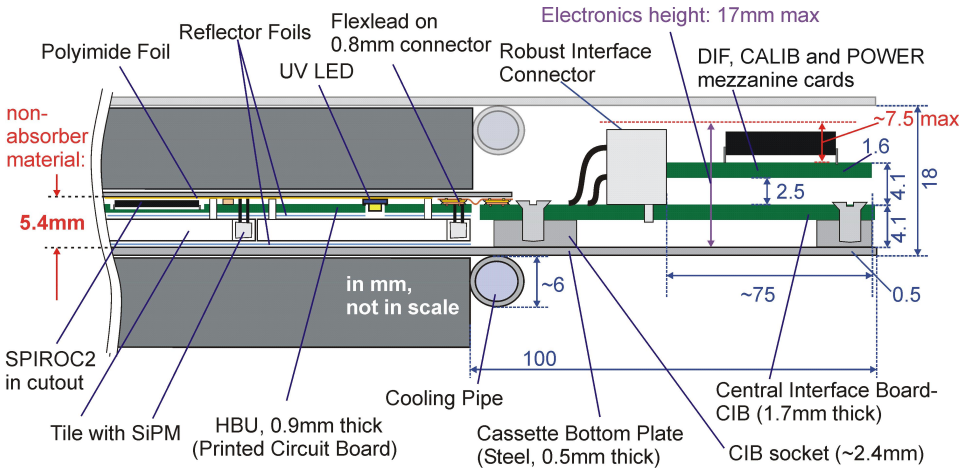


Figure 5: Cross section of one layer of the AHCAL.

2 Linearity measurements on the input ADC

To get used to the hard- and software of the engineering prototype, some input ADC linearity measurements were done with the HBU. The SPIROC2b has selectable feedback capacitors in the preamplifiers of each input channel. The SiPM gain varies even between SiPMs of the same production cycle which makes individual calibration a necessity. To reduce the amount of software compensation of different gains, a fitting preamplifier capacity can be chosen to roughly equalize the hardware gain of each SiPM readout chain. The feedback capacity can be chosen from 25 fF to 1575 fF in 25 fF steps.

The SPIROC chip offers two gain modes at a fixed gain ratio of ten. The high gain mode is used to generate single pixel spectra for calibration purposes and also for smaller signals in the range of single MIPs. The low gain mode is supposed to offer full dynamic range up to 2000 fired pixels. An auto gain mechanism switches automatically between both modes to use the suitable gain for each signal.

2.1 Data taking

To measure linearity and gain of the setup, specific charge from a pulse generator was injected into different input channels.

For each point in the following plots 100 readout cycles were taken into account, consisting of 16 single measurements each. However, only the first 8 of these measurements per readout cycle were used, as some of the analog memory cells on the SPIROC give consistently too small values. Additionally the SPIROC will occasionally (up to 15% of readouts) output zero instead of the real ADC value. That is a known problem in the digital chip part, as an error in setting the analog memory cell would result in a measurement on pedestal level around 200 ADC counts. Ignoring all ADC reads with zero value works, but decreases statistics further. To measure the full dynamic range of both modes, the auto gain was disabled during these measurements.

2.2 High gain

For the measurements in high gain mode between 1 pC and 14 pC were injected into three different input channels of one SPIROC. This was done for four different preamplifier capacities (100 fF, 125 fF, 150 fF, 200 fF). Figure 6 shows the measurements done for channel 35. Statistical fluctuations per measurement are of the order of 1%. Up to 9 pC injected charge the response is linear (before reaching saturation) for all preamplifier capacities, extending up to 12 pC for 200 fF preamplifier capacity and possibly more for bigger capacitors. From pedestal level (∼200 ADC counts, see fig. 9) to saturation (∼2500 ADC counts) only around 11 of the 12 bits ADC range are used. The other channels generally show a similar behaviour (see fig. 7). The most notable difference is the different use of output dynamic range on channel 5, which coincides with an extended dynamic input range in the low feedback capacity range. As the slopes from channel 5 do not deviate as much as the dynamic range from the other channels (see fig. 8),

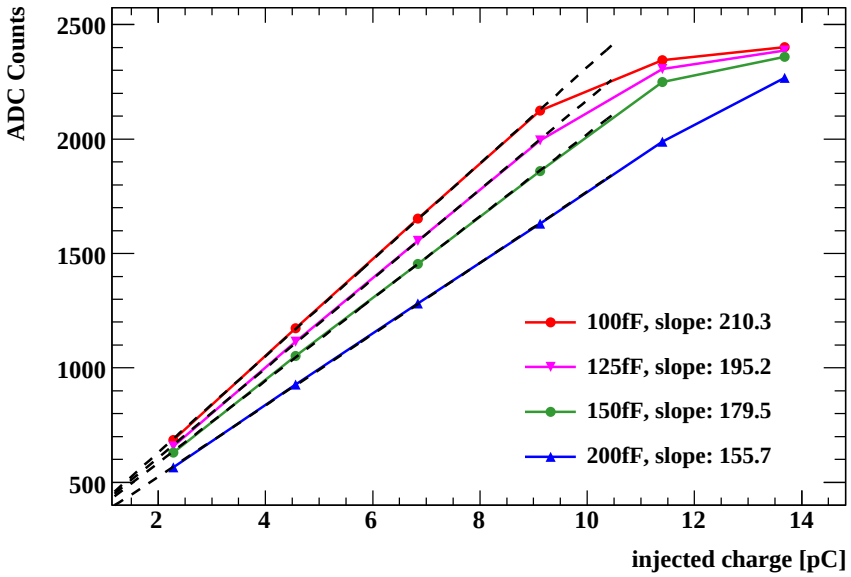


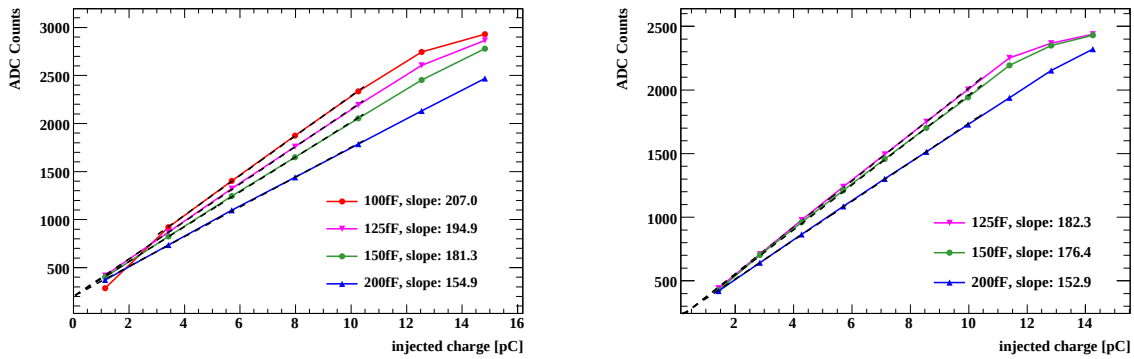
Figure 6: ADC response in high gain mode on channel 35 for different preamplifier capacities.

channel 5 has an overall better performance than the other probed channels and thus should be used to further investigate how to improve the performance of other channels.

In fig. 8 the dependency between ADC slope and preamplifier capacitor is shown. It is notable that for a doubled feedback capacity the ADC slope does not reduce to one half as would be expected. Potentially the selectable feedback capacity is in parallel to a fixed feedback capacity. In general, the measured ADC slopes are similar for different channels although there are outliers like the 125 fF slope on channel 35. Apart from that outlier, slopes from different capacities do not overlap. In conclusion the selectable preamplifier capacities can be used to adjust the gain of single channel readout chains in a wide range, although the exact bounds on that were not determined as only a small sample of feedback capacities have been tested.

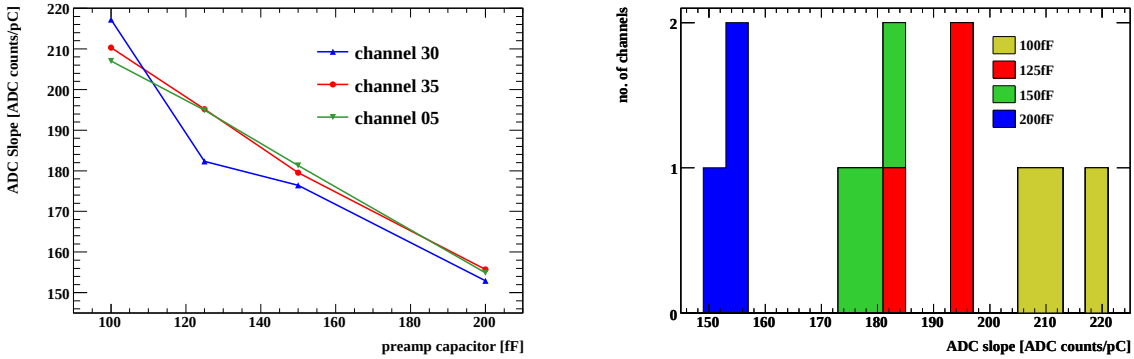
2.2.1 Pedestal shift

A pedestal shift is the unintentional effect that injection of charge into one channel lowers the pedestal level of other channels, i.e. stressing one channel will change the measurement of other channels on the same chip. To investigate this the feedback capacity was changed for a channel that had no charge injected. This measurement gives insight into the pedestal shift for different feedback capacities, shown in fig. 9. The measured ADC slope changes at around the same factor as in the other measurements, although on an absolutely much smaller scale. The pedestal shift is not well understood yet and needs further investigation.



(a) channel 5 (b) channel 30

Figure 7: ADC response in high gain mode for different preamplifier capacities.



(a) slope/capacity dependence (b) distribution of ADC slopes

Figure 8: ADC slope in high gain mode for different feedback capacities.

2.3 Low gain

The low gain mode was investigated for channel 5 using the same feedback capacities as before in the range of injected charges from 5 pC to 190 pC. As the dynamic output range of the pulse generator is limited, different attenuators had to be used for the lower and upper part respectively. The upper part (27 pC to 190 pC) is shown in fig. 10. Good linearity is observed until ∼130 pC input charge which, depending on the SiPM gain, equals to around 1500-2000 fired pixels. The preamplifier saturates around 3000 ADC counts, which is around the saturation level observed in high gain mode for that channel. As channel 5 has already been shown to be the channel with the best used ADC range, it might be interesting to see if other channels also show similarly equal ADC range uses.

The lower part (6 pC to 28 pC, fig. 11.(a)) also shows linear behaviour as expected, reaching well into the high gain region. However, the fitted slopes do not match between the lower and higher part. This is most probably due to the used attenuators not acting

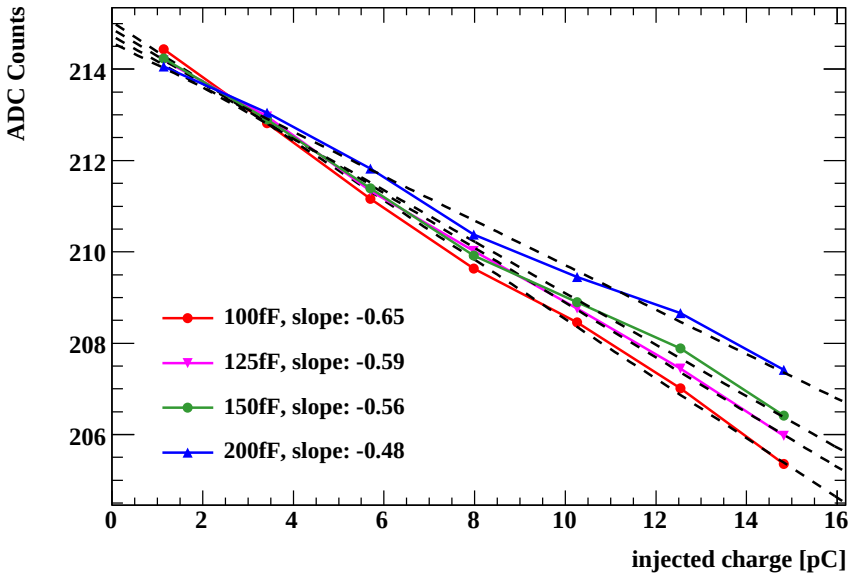


Figure 9: Pedestal shift of an unloaded channel for different feedback capacities.

as expected, which also means that the given charge values are not necessarily absolutely exact. This does not extend to the linearity itself as relative changes in charge should not be affected.

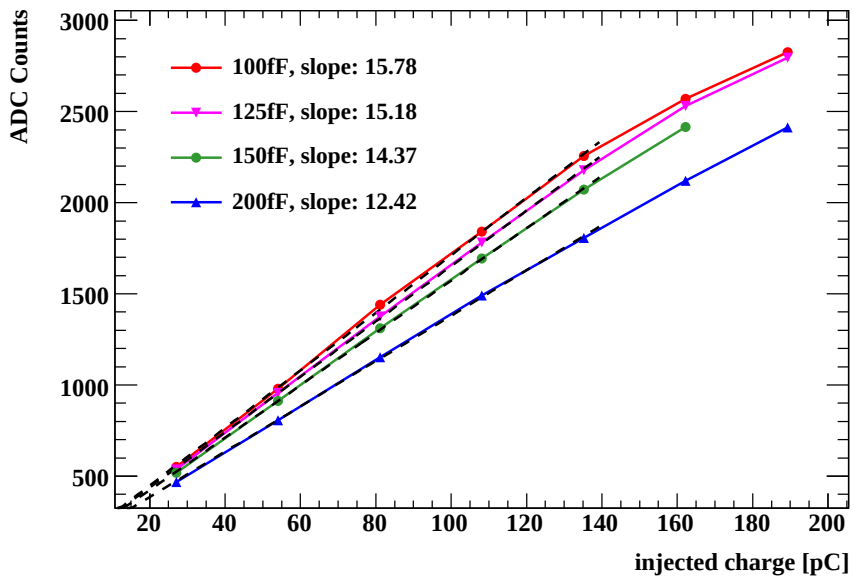
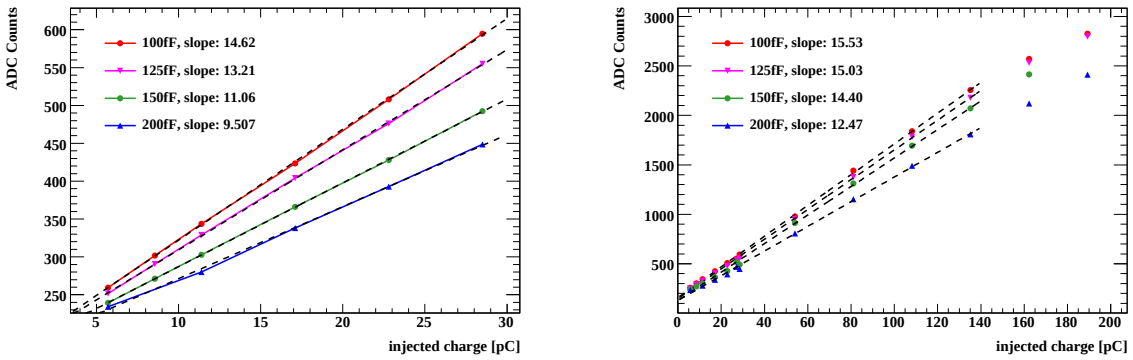


Figure 10: ADC slope of channel 5 in low gain mode, upper range.



(a) lower range

(b) combined range plot

Figure 11: ADC slopes of channel 5 in low gain mode.

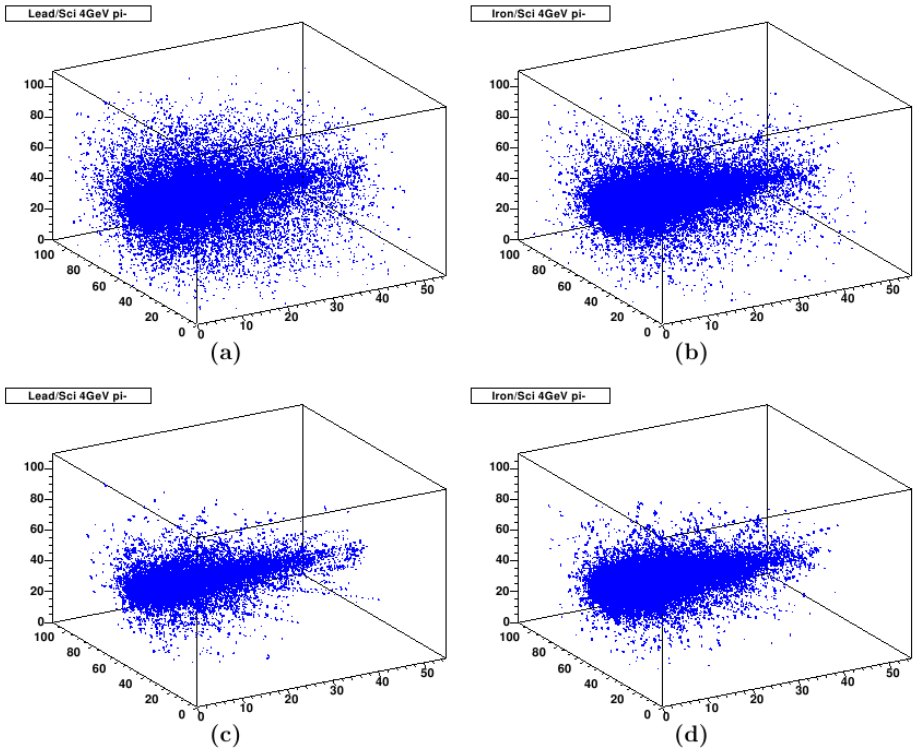


Figure 12: Simulated shower from a 4 GeV pion for lead (a) and iron absorbers (b), (c) and (d) show the same shower with a timecut on $t < 5$ ns [2].

3 Measurements on the TDC

3.1 Motivation

In combination with the high granularity, precise timing can take part in improving the performance of the AHCAL. It is known that the hadronic part of a particle shower is not necessarily as instantaneous as the eletcromagnetic part, but due to the formation of neutral particles, has a slower propagation speed. The most extreme form of that are neutrons at down to thermal energies which can float through the detector without interaction for seconds and more. So if it is possible to tag every AHCAL trigger on each tile with a timestamp, timing cuts can be applied on the developing showers which helps in separation of overlapping showers during reconstruction. Simulations for iron and lead absorbers show, that the decrease in shower extension is more notable for lead than for iron when applying a 5 ns time cut (see fig.12). Lead is not a considered option for the AHCAL but it is expected for a tungsten calorimeter to behave similar to lead in this regard as the atomic numbers are in similar regions.

Another aspect of a high resolution timing in hadronic showers is the verification of shower simulations. As hadronic showers in general are not perfectly well understood (especially the low energy fraction), simulation of such processes has to be verified by

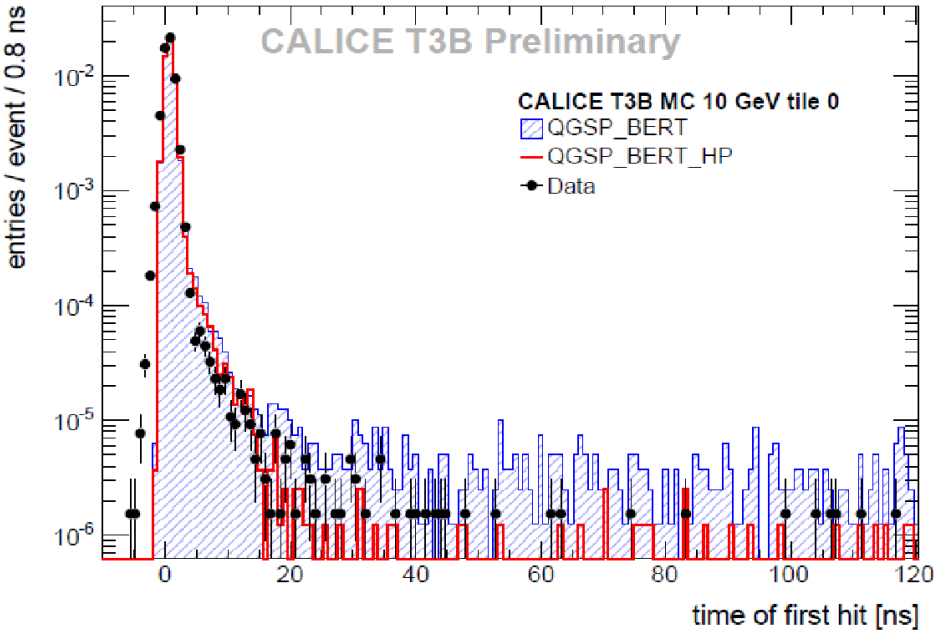


Figure 13: Measured radial time development for a hadronic shower in the tungsten AHCAL prototype in comparison to simulations [4].

experimental setups. For that a highly granular, time resolving calorimeter is needed. A first proof of concept for that has been realised in one of the recent AHCAL test beams with only one row of 15 scintillating tiles at the downbeam end of the AHCAL [4]. Comparison with the ILD standard for hadronic shower simulation, GEANT4 with the physics list QGSP_BERT, has already shown that the agreement between data and measurements is better when using the high precision extension QGSP_BERT_HP (see fig. 13). Such a measurement for a full 3D calorimeter would enlighten the issue further.

In the search for new physics a good time resolution in the AHCAL could also be beneficial. (For example the lifetime of a late decaying particle could be measured by exploiting the timing information from the calorimeters).

3.2 TDC working principle

The TDC on the SPIROC2b chip is realised as a time to amplitude converter (TAC). A capacitor is charged with a constant current which increases the capacitor voltage linearly. Once the auto trigger fires, the current is switched off. The resulting voltage on the capacitor is then a direct measure for the time the capacitor was charged, which can be read out using an ADC. At the beginning of each measurement the voltage ramp has to be reset which creates some deadtime in the TDC. To circumvent that reset deadtime, two separate voltage ramps are used (*dual ramp TDC*) which are activated at alternating clock cycles. That gives each ramp time to reset while the other one is

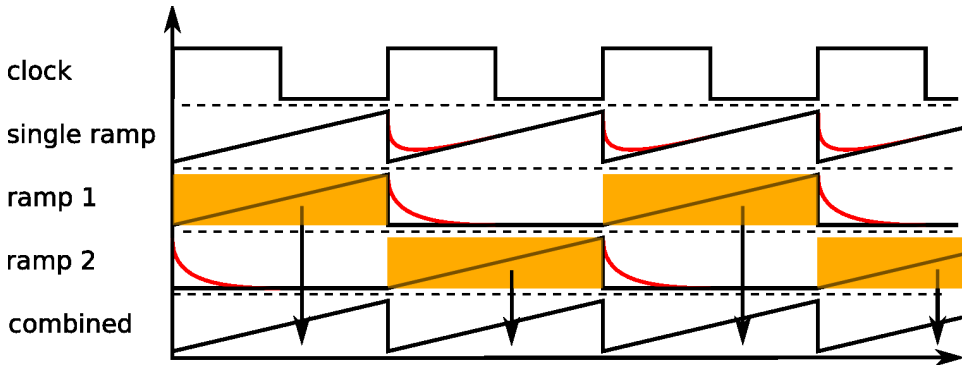


Figure 14: Schematic working principle of a dual slope TDC, reset effects are shown in red.

ramping up. The switching between ramps is done by a multiplexer. A schematic for this is given in fig. 14.

3.3 SPIROC TDC modes

The SPIROC2b chip features two different TDC modes called *ILC mode* and *testbeam mode*. They differ primarily in the length of the TDC ramp. Switching between modes can be done in the slow control for each ASIC. As the bunch clock is provided externally, all SPIROC chips have to work in the same TDC mode.

3.3.1 ILC mode

In ILC mode the TDC ramp is configured to match the planned ILC bunch crossing frequency of 5 MHz, resulting in a 200 ns ramp length. The design resolution for ILC mode is 100 ps.

Measurements in ILC mode were done in a similar way to the ADC measurements. 50 cycles of 16 triggers were used for each point. The TDC does not suffer from the memory cell voltage drop, so all 16 triggers could be used. Zero reads also occur in the TDC, although much more rarely ($\ll 1\%$).

As the use of the dynamic range of the TDC was unsatisfactory in the beginning, a 10 kΩ resistor was soldered on the bias point responsible for fine tuning the TDC slope. Decreasing that resistor below 10 kΩ does not increase the ramp slope further but may introduce saturation effects.

3.3.2 Testbeam mode

In testbeam mode there is no fixed bunch structure to be met, so the timing can be flexible. The goal is to increase the ramp length to minimize deadtime from multiplexing while still meeting a resolution of about 1 ns. For this a ramp length of 5 μs (200 kHz) has been implemented.

In addition to the TDC ramp slope, the bunch clock has to be adjusted as well. This is done in the firmware of the detector interface board. However the modifications in the firmware timing introduce a fixed timing shift between the TDC memory cells. This issue is resolvable in the future. As a temporary workaround only one memory cell was used for each measurement. 100 cycles with 8 triggers each were taken per measurement.

For the testbeam mode (if not explicitly specified otherwise) no resistors have been soldered to any bias points.

3.4 Definition of resolution

Resolution is the central benchmark for the TDC. The total resolution is defined as

$$\sigma_{tot} = \frac{\sqrt{\sigma_{stat})^2 + \sigma_{fit}^2}}{m_{fit}}. \tag{1}$$

The statistical fluctuation of each measurement σ_{stat} can be read off the histogram of all the single measurements for one point. σ_{fit} is the deviation of the fit from the actual data. For this the differences between fit and data for the fitted range are filled into a histogram of which the standard deviation is calculated. The slope of the fitted linear function m_{fit} is used to convert the resolution from TDC counts into a unit of time.

3.5 Measurement in ILC Mode

3.5.1 TDC ramp

For measurements of the ramp shape in ILC mode, the pulse generator is set to be triggered by the DIF board while the SPIROC is set to auto trigger mode. By variation of the delay between trigger and signal output on the pulse generator the TDC ramp can be scanned. This was done in steps of 2-5 ns. The resulting plot is shown in fig. 15.

The ramp length is around 220 ns, a bit more than expected. As this is a simple timing issue (bunch clock frequency less than 5 MHz) it should be no problem to fix this in the DIF firmware if needed. Obviously the deadtime between the two ramps needs to be worked on. This seems to be due to a too slow multiplexer, as ramp reset effects should have been eliminated by the TDC scheme (see fig. 14). The deadtime is around 100 ns, nearly 50% of the 220 ns ramp length. Around 1400 TDC counts of dynamic range are used even after increasing the ramp slope via a bias point resistor. That is approximately one third of the full 12 bit dynamic range of the TDC. It is also apparent that the different ramps have different starting and end heights. Finally from pure eye judgement it can be seen that the ramp is not straight everywhere but has a curvature.

As a first try, a straight fit was done for the full invertible part of each ramp, shown in fig. 16. As could be expected from the shape of the ramp itself, the fit has large deviation from the data points which causes a resolution far from the 100 ps design aim. The structure of the fit residual shows non random structure, in particular two distinct

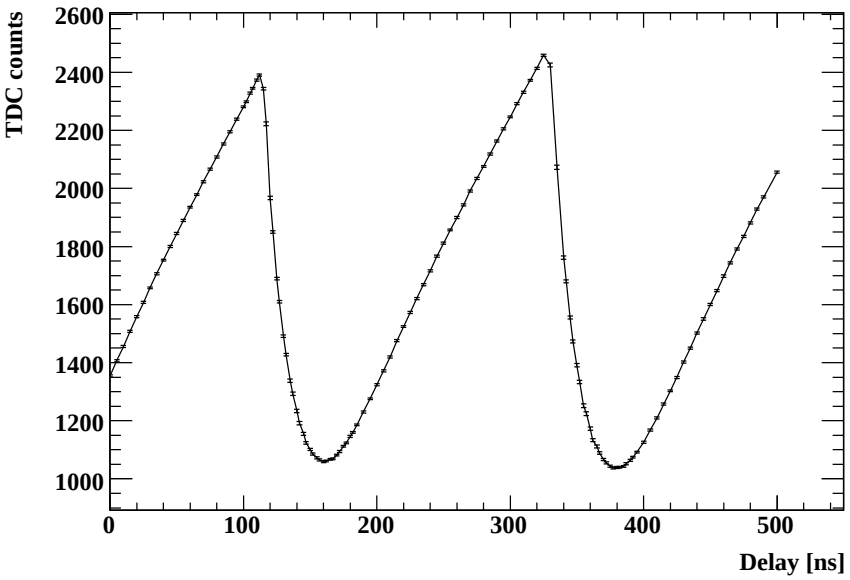


Figure 15: Measured TDC ramp in ILC mode, channel 5.

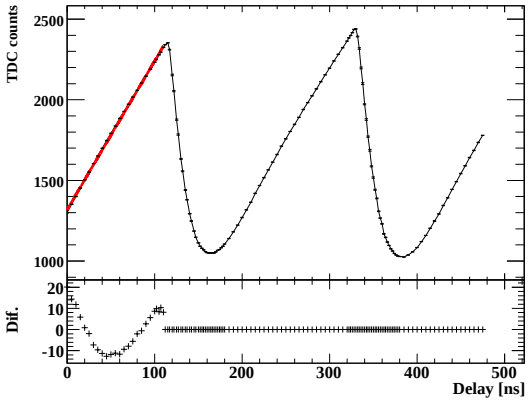
slopes in the first and second part of each fit respectively. Thus fitting the range with two separate straight lines might improve the achieved time resolution. This is shown in fig. 17.

By fitting two separate slopes per ramp the TDC resolution increases significantly. A complete overview over all fitted resolutions is given in table 1.

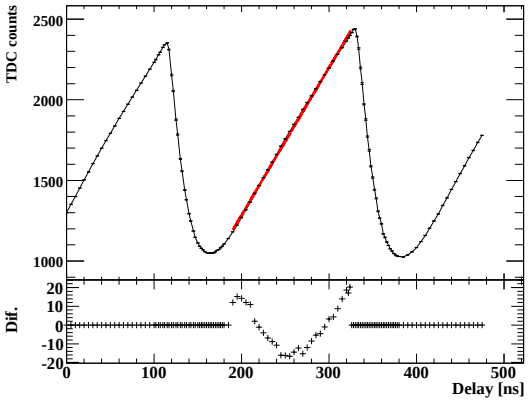
Table 1: Fitted TDC resolutions for ILC mode.

chn	ramp	part	σ_{stat}	σ_{fit}	slope	σ_{tot} [ps]
30	1	lower	1.22	2.26	9.92	259
30	1	upper	1.26	1.55	8.76	228
30	2	lower	1.18	2.39	9.77	272
30	2	upper	1.33	2.66	8.63	344
5	1	lower	1.17	3.42	9.79	369
5	1	upper	1.24	1.43	8.77	216
5	2	lower	1.22	2.18	9.70	258
5	2	upper	1.38	2.60	8.76	336

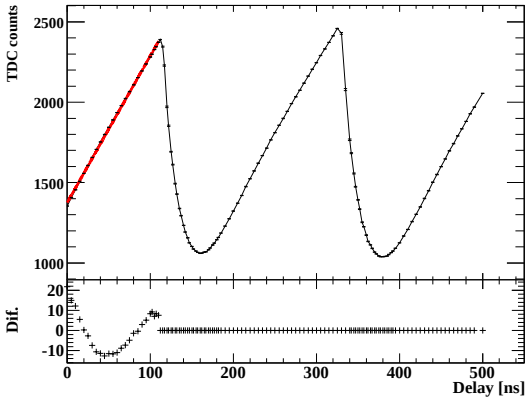
Most resolutions are within a range of $250 - 350\,\mathrm{ps}$, which is still a factor of three away from the design but at least a factor of three nearer than the single straight fit. It is notable that for most fits σ_{fit} is the main contributor to the total resolution. Only for the upper part of the first ramps σ_{fit} and σ_{stat} are nearly of the same value. This means that for most parts an improvement in either the fit or the ramp itself would



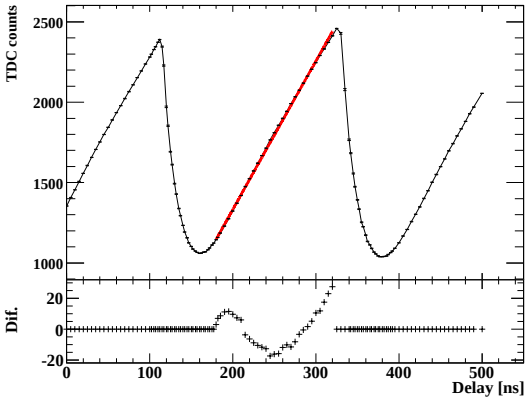
(a) channel 5, $\sigma_{tot} = 1.042\,\text{ns}$, slope: 9.21



(b) channel 5, $\sigma_{tot} = 1.309\,\text{ns}$, slope: 9.15



(c) channel 30, $\sigma_{tot} = 1.046\,\text{ns}$, slope: 9.14

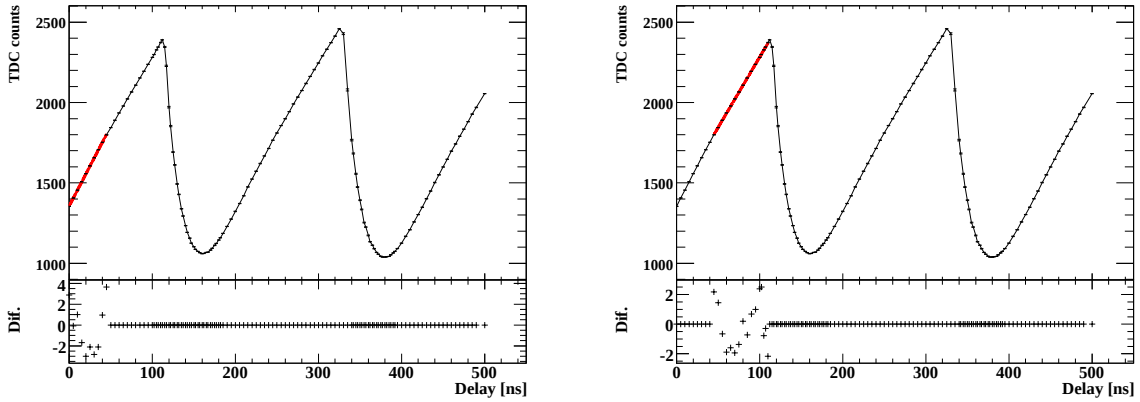


(d) channel 30, $\sigma_{tot} = 1.350\,\text{ns}$, slope: 9.14

Figure 16: Fits over the full ramp.

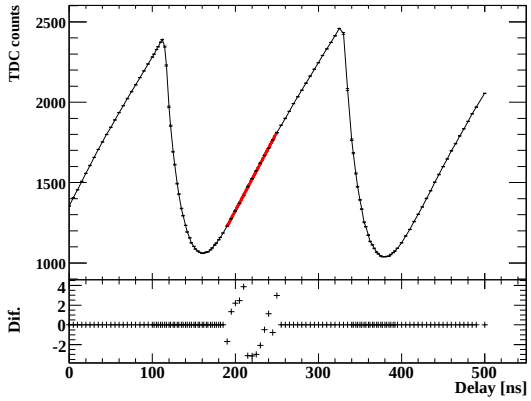
cause a substantial improvement in resolution, whereas such improvements would not lead to better results for those cases where the statistical error is already governing the results. If the ramps would be perfect and only statistical fluctuations were defining the total resolution, the value would be around $125 - 150\,\text{ps}$. As it is probably much harder to decrease the statistical uncertainty than improving the ramp linearity (at least to the point where both have around the same impact), the easiest way to increase the resolution further is increasing the ramp slope. As mentioned before this has already been tested on one specific bias point, but still more than 50% of the dynamic range is unused.

There is no specific bit to tell on which of the two TDC ramps a measurement was taken except for the even/odd parity of the *bunch crossing ID* (a counter for bunch clock cycles). The parity of the bunch crossing ID seems to get lost sometimes during measurements, so it is not a reliable way of telling the two ramps apart. As ramp 1 and ramp 2 may have slightly different slopes, this adds uncertainty on the measurement thus decreasing resolution. To estimate the resolution without strict ramp assignment, the ramps were fitted again in two separate parts each, but with a fixed slope of the

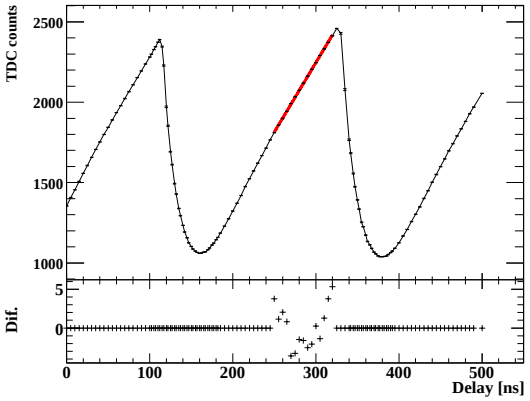


(a) channel 30, $\sigma_{tot} = 258.1\,\text{ps}$, slope: 9.92

(b) channel 30, $\sigma_{tot} = 223.6\,\text{ps}$, slope: 8.76



(c) channel 30, $\sigma_{tot} = 273.9\,\text{ps}$, slope: 9.77



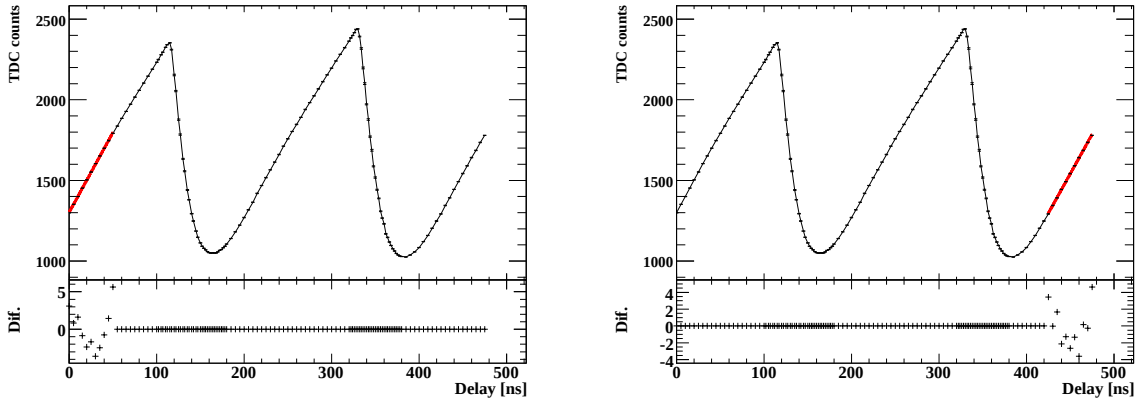
(d) channel 30, $\sigma_{tot} = 337.7\,\text{ps}$, slope: 8.63

Figure 17: Fits over half ramps, channel 30.

average of the fitted slopes. The results are shown in table 2. With the exception of the upper part of ramp 2 on channel 5, which shows an unusual strong decrease in resolution, resolutions do not worsen more than 10%. However, as it is unknown on which ramp a measurement is done, as a conservative upper limit the worse of the two resolutions for one of the ramp parts has to be used for eventual calculations involving the resolution.

After the reset of ramp 2 on channel 5, ramp 1 should be measured for higher delay values. To check the consistency of the measurements the ramp part that was measured twice is fitted and compared, depicted in fig. 18. It is very astonishing that the fitted slopes have more than 10% difference from each other. As ramp 1 itself has a lot smaller statistical deviation than 10%, this can only be an effect of the pulse generator, but further investigations have to be done on this topic.

Regarding all the mentioned characteristics of the ILC mode TDC ramp the central question has to be whether it is possible to use the ILC mode in a testbeam physics prototype environment. Via configuration of the different delay lines it should be possible to set the ramp timing that the first triggered (zero delay) events are in the beginning of the usable TDC ramp (similar to how this measurements were done). This limits the



(a) channel 5, $\sigma_{tot} = 290.7\,\text{ps}$, slope: 9.90 (b) channel 5, $\sigma_{tot} = 275.9\,\text{ps}$, slope: 9.78

Figure 18: Fit comparison of the same ramp.

Table 2: TDC resolutions for ILC mode for averaged ramp slopes.

chn	ramp	part	σ_{stat}	σ_{fit}	slope	σ_{tot} [ps]
30	1	lower	1.22	2.54	9.84	286
30	1	upper	1.26	1.92	8.70	264
30	2	lower	1.18	2.75	9.84	304
30	2	upper	1.33	3.21	8.70	400
5	1	lower	1.17	3.60	9.75	388
5	1	upper	1.24	1.43	8.77	216
5	2	lower	1.22	2.20	9.75	258
5	2	upper	1.38	4.40	8.77	526

maximum measurable time to around 100 ns (until the ramp is switched) and creates timing noise for every trigger in the area of 100-200 ns timestamp. However, this is an acceptable tradeoff as most of the events should be contained in the first 100 ns. Also no energy measurement is lost, only the time assignment would be wrong. So with minor restrictions it should be possible to use the ILC mode for physical measurements in a future testbeam.

3.5.2 ILC mode ramp spectrum

If the pulse generator is set to fire flat distributed random pulses into the SPIROC2b, a TDC spectrum can be obtained. Such a spectrum reflects some of the TDC characteristics of one channel as shown in fig. 19. The difference in minimum values during reset is reflected in the distance between the two peaks at the beginning of the spectrum. The difference in ramp heights can very clearly be seen in the steps at the end of the spectrum. These can be easily fitted with a double step function to determine ramp height differences from the spectrum.

The pulse generator does not have a random pulsing mode, but it has proven to be enough if the pulse generator is set into auto mode with a pulse distance of much more than the length of one ramp. All spectrum measurements for the ILC mode were done with 81.3 μs delay between pulses. To have each acquire period long enough to catch at least one trigger, the *trigger_dist* value in the DAQ software has to be set sufficiently high.

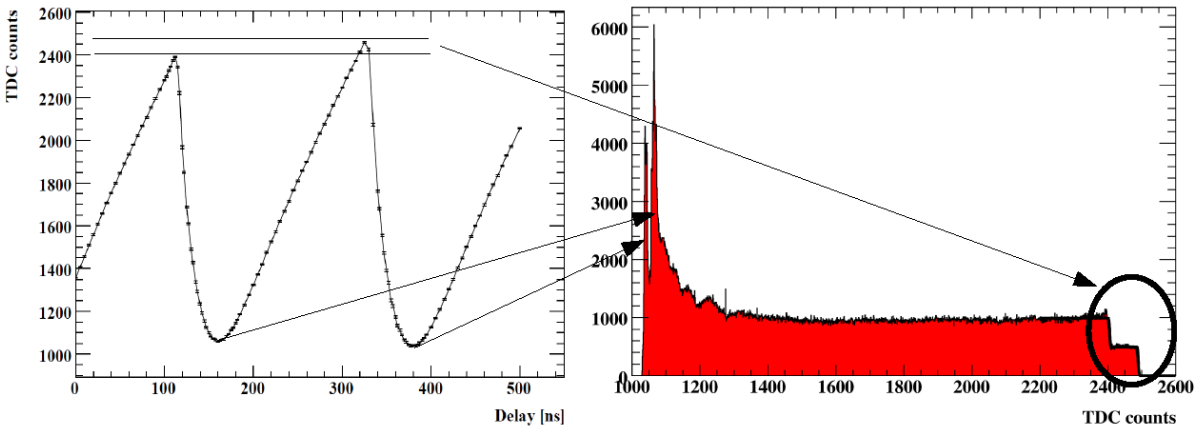


Figure 19: TDC ramp characteristics reflected in spectrum measurements.

To investigate a possible correlation between input ADC load and measured TDC value, the spectrum of channel 30 has been measured with 2.85 pC, 5.7 pC and 8.55 pC injected charge. The stacked plot of these spectrums in fig. 20 shows that all the visible features in the spectra are located on the same TDC value. Indeed the fit values show that the ramp heights are less than two TDC counts apart, so no apparent dependency between ADC and TDC has been observed.

Spectrums have been taken for different channels with otherwise identical setup. Two example plots are shown in fig. 21. There are no major feature differences between spectra for different channels, although the end height of the two ramps may shift. Ramp 2 is higher than ramp 1 for all measured channels. The distribution of ramp heights and differences between height for ramp 1 and ramp 2 are depicted in fig. 22. The ramp heights differ up to 40 TDC counts, but the difference between ramp heights is relatively stable around 85-87 TDC counts. It might be interesting to compare the total heights

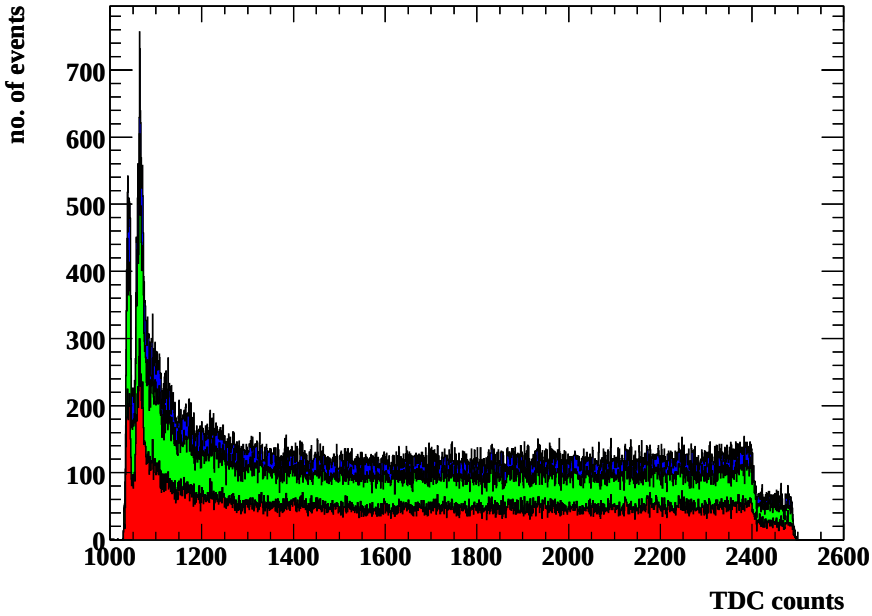
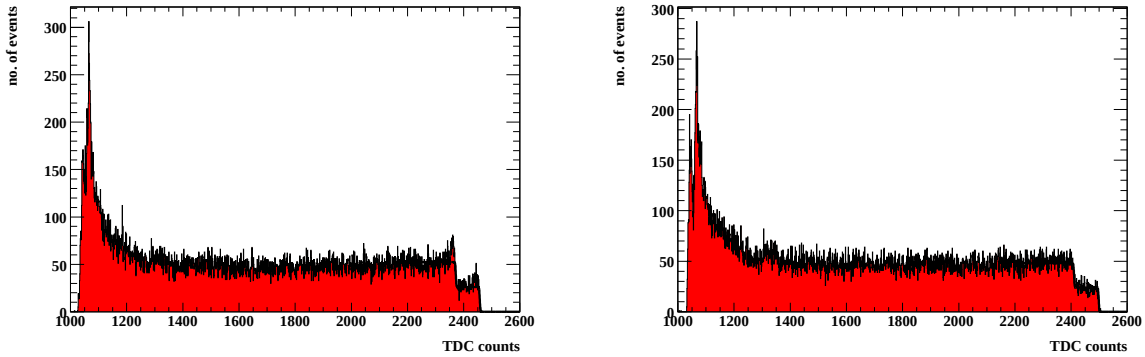


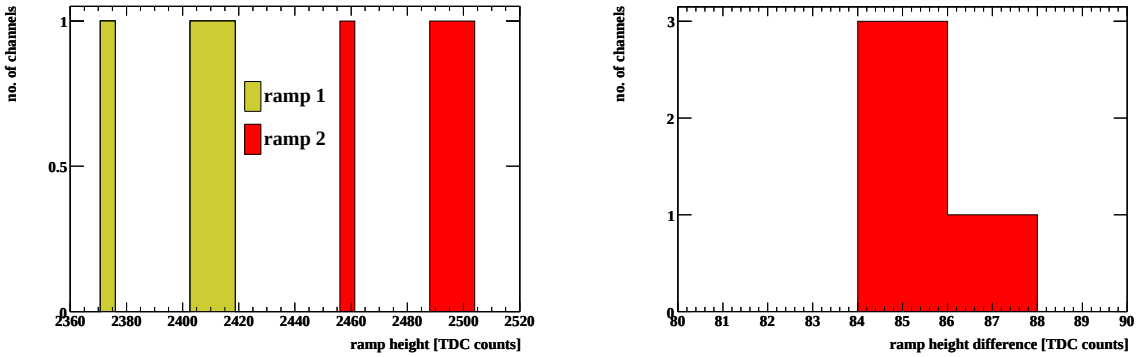
Figure 20: Stacked ILC mode TDC spectra for different injected charge.

of the ramps by subtracting the lowest TDC value for each ramp during multiplexing which can be obtained from fitting the peaks in the beginning of the spectrum. Maybe the ramps are shifting completely and such have similar total heights.



(a) Channel 5 (b) Channel 33

Figure 21: Spectra of non correlated triggers.



(a) Ramp heights (b) Difference of ramp heights

Figure 22: Histograms from spectrum step fit results.

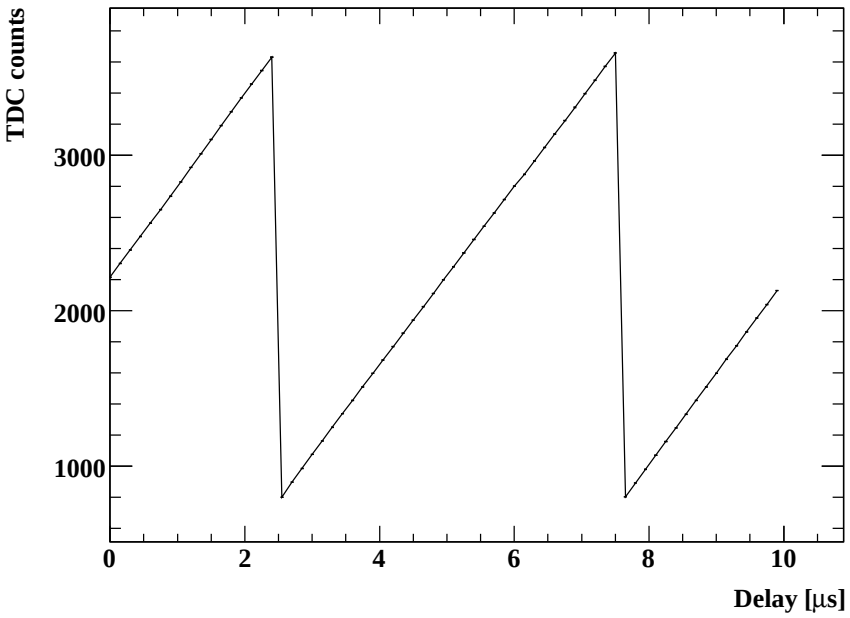


Figure 23: Testbeam mode TDC ramp, channel 5.

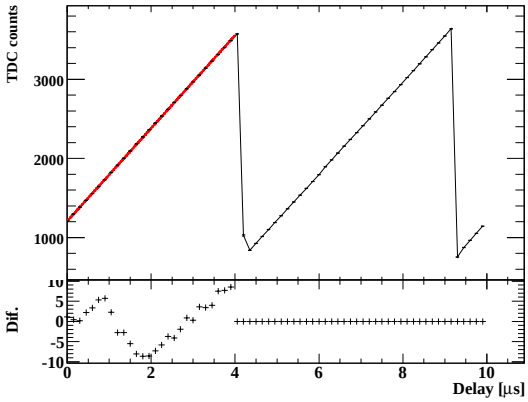
3.6 Measurement in testbeam mode

3.6.1 Testbeam ramp

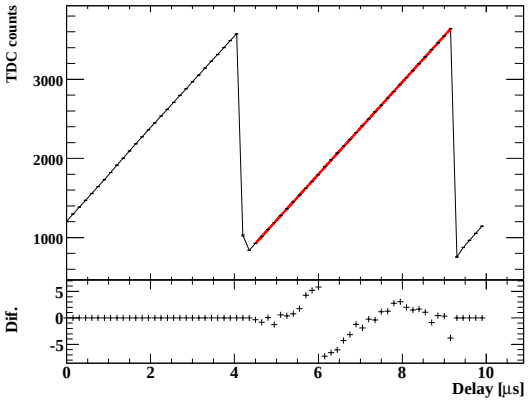
The TDC ramp has been measured for several channels in testbeam mode (fig. 23). Again first the ramps were fitted over their full range, which is shown for one example channel in fig. 24. The achieved resolution of $> 5\,\text{ns}$ is not sufficient to measure time development of hadron showers but the fit residuals once again show non random structure.

The fit residuals for the first ramp seem to segment the first ramp intro three parts around $0 - 1\,\mu\text{s}$, $1 - 2\,\mu\text{s}$ and $2 - 4\,\mu\text{s}$. Judging from the fit residuals the second ramp has an edge around the $6\,\mu\text{s}$ mark. A fit in two parts improves the resolution to better than 5 ns, in some parts down to around 2.5 ns (see fig. 25). On the upper half of ramp 2 there is still a triangular structure on the fit residuals that could justify another split into two linear functions, but as a multi-linear fit is not feasible for each TDC ramp on every ASIC channel for a testbeam calorimeter (let alone a full ILD HCAL with millions of SiPMs) this mode of fitting has to be sufficient.

However, the delays at which the observed slope changes and edges in the TDC ramp are observed happen around full integer values. Also short steep edges in the ramp as observed on ramp 2 are not a usual problem occuring in voltage ramps. This hints towards delay generated by the pulse generator as the main source of these added uncertainties. Further investigations should include verification of the results with another

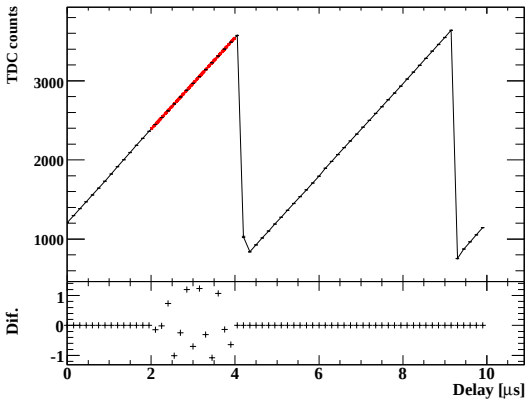


(a) channel 4, $\sigma_{tot} = 8.876\,\text{ns}$, slope: 586.81

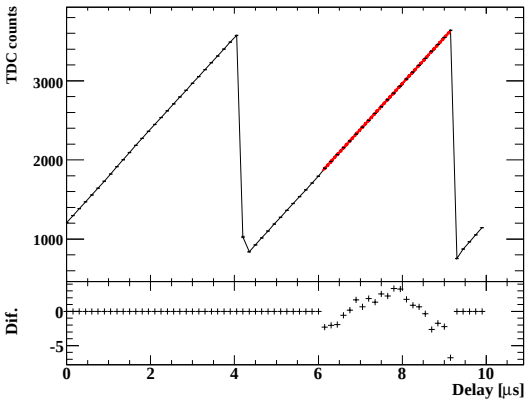


(b) channel 4, $\sigma_{tot} = 5.617\,\text{ns}$, slope: 582.50

Figure 24: Linear fits over the full ramp in testbeam mode.



(a) channel 4, $\sigma_{tot} = 2.477\,\text{ns}$, slope: 577.73



(b) channel 4, $\sigma_{tot} = 4.627\,\text{ns}$, slope: 579.87

Figure 25: Testbeam mode fits over the parts of the ramp.

type of pulse generator and an external TDC to take a closer look at the pulse generator delay.

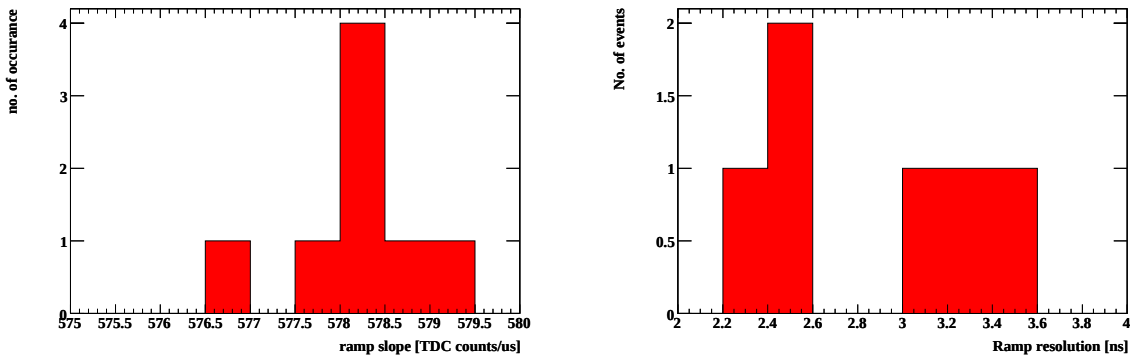
In table 3 measured resolutions for half ramp fits are shown. Some parts of some ramps have not been fitted, as the fit range would have included not enough data points for a meaningful fit. It is apparent that the fitted slopes are very similar. The average resolution increases but is still not in the 1 ns range. The distribution of fitted slopes and resolutions is shown in fig. 26.

As the fitted slopes are so close to each other the effects of ramp confusion on the TDC resolution are negligible and were therefore not investigated.

For most measurements σ_{stat} is about the same or even larger than σ_{fit}. Even when dismissing the fit resolution loss from non-linearities in the ramp, the pure statistical error gives around 2 ns resolution. This means that the only way to increase the resolution further is to increase the TDC slope m_{fit}. This should be possible without other adjustments, as the largest part of the TDC dynamic range is still unused. Even if the full

Table 3: TDC resolutions for testbeam mode from fitting half ramps.

chn	ramp	part	σ_{stat}	σ_{fit}	slope	σ_{tot} [ns]
4	1	upper	1.24	0.71	577.73	2.477
4	2	upper	1.25	2.37	579.87	4.627
30	1	upper	1.18	0.923	578.01	2.592
30	2	lower	1.21	1.40	579.06	3.233
30	2	upper	1.21	1.29	578.46	3.061
35	1	lower	1.20	0.66	578.48	2.375
35	2	lower	1.22	1.58	578.84	3.449



(a) Slope distribution

(b) Resolution distribution

Figure 26: Distributions from testbeam mode TDC ramp fits.

TDC dynamic range usage is reached it is possible to increase the bunch clock frequency, thus preventing the now steeper ramp from overflowing. The drawback of a decreased ramp length would be increased deadtime from the multiplexer effects discussed before, which is negligible for ramp lengths $< 2\,\mu$s.

In an attempt to increase the TDC slope in testbeam mode, a $10\,\mathrm{k}\Omega$ resistor was soldered to the TDC slope bias point. Also the bunch clock frequency was increased to reach a cycle length of around $1.25\,\mu$s. The resulting ramp measurement is shown in fig. 27. The measured ramp saturates very quickly for unknown reasons, but in the small linear part a slope of 2.3 times the previous slopes can be fitted. If it is possible to resolve the saturation issue, an increase in resolution of factor 2.3 is possible. For most ramp parts that would be very near the targeted 1 ns. Possibly with the use of other bias points even steeper TDC slopes can be achieved, resulting in even better resolutions.

The testbeam mode was specifically designed for best possible perfomance in a test-beam setup where there are no fixed spill timings. For this the TDC ramp is active all the time and each event has to be timed relative to the first triggered hit on one of the ramps. If that first hit is very close to a ramp switch the timing of that spill will be

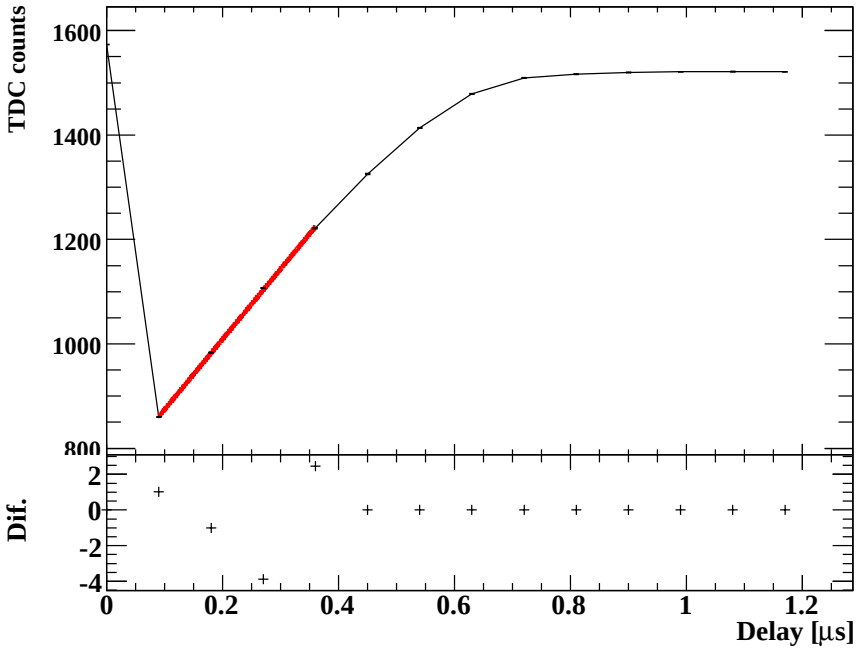


Figure 27: Testbeam mode ramp measurement for increased ramp slope and decreased ramp length. Slope: 1345

unusable. As in testbeam mode the deadtime is relatively small compared to the TDC cycle length, this should not be big a problem for testbeam operations.

3.6.2 Testbeam mode TDC spectrum

Testbeam mode TDC spectra were taken in a similar way as the ILC mode spectra. A pulse generator frequency of 951 μs clock length was used. As could already be seen from the ramp plots in testbeam mode, the ramps do not have significantly different heights or minimum values. Also the deadtime effects from the multiplexer are relatively small for testbeam mode. Therefore no significant features on the testbeam TDC spectra are expected. As depicted in fig. 28 no outstanding features are observed on such a spectrum. No shift in the spectrum has been observed for different injected charges of 5.7 pC and 8.55 pC, so there is no effect from loading the ADC on the TDC as in ILC mode.

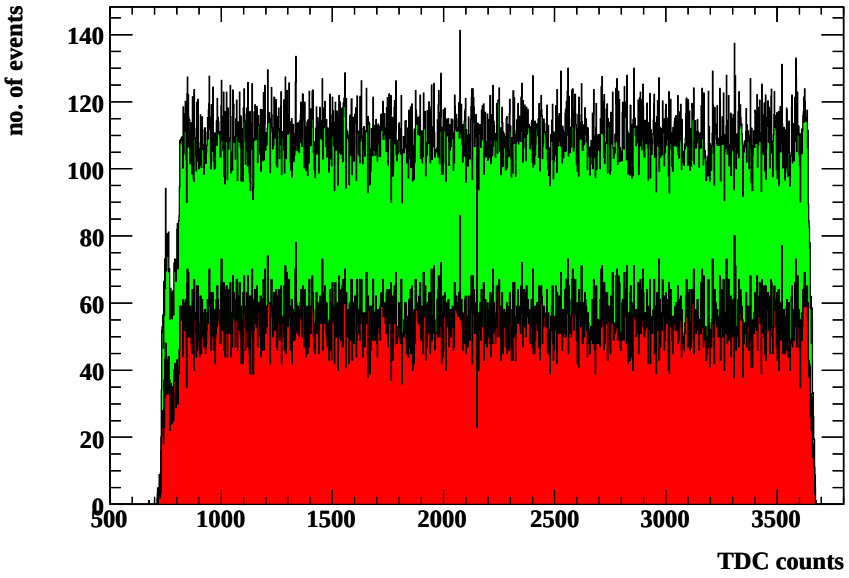


Figure 28: Stacked testbeam mode TDC spectra for different injected charges, channel 4.

4 Summary

In this report my work as a summer student in 2011 at DESY Hamburg is presented. Measurements have been performed on linearity and resolution of the ADC and TDC of the SPIROC2b ASIC. All measurements were taken via charge injection.

In the measurements on the ADC a linear response was confirmed for different channels in both high and low gain mode. It has been shown that the low gain mode is sufficiently sensitive to cover enough of the high gain mode to have a seamless dynamic range. The selectable feedback capacity per channel has been established as a way of adjusting the gain for each readout chain. However, the fitted ADC slopes do not fall off inversely proportional to the set feedback capacity. Also not all channels respond to all feedback capacities in the same way.

In the measurements on the TDC in ILC mode an overall resolution around 300 ps has been achieved by fitting each TDC ramp in two parts with different linear functions. The ramps are not straight enough to give acceptable results with only one linear fit. From spectrum measurements different ramp heights and ramp height differences can be fitted. Possible confusion between ramps leads to a decrease in resolution as long as no safe way of knowing from which ramp a measurement originates. Ramp heights may vary between different channels but ramp height differences are quite constant. By better use of the dynamic range the resolution could be increased by at least a factor of two, resulting in a performance very near to the designed 100 ps resolution.

In testbeam TDC mode an average resolution of 3 ns has been measured. Again the fit had to be done in two separate linear functions per ramp. This is mostly due to apparent shifts in the pulse generator timing. The fitted slopes of the testbeam mode ramp are very similar, thus the problem of ramp confusion is negligible. Measured testbeam mode TDC spectra show no apparent features. The use of dynamic range can also be improved in testbeam mode. If the saturation problem for increased slopes gets solved, a performance of better than 1 ns resolution should be easily achievable.

The feasibility of using the SPIROC2b for timed testbeam measurements has been established, although minor difficulties still need to be adressed. With the arrival of the new HBUs first multi HBU tests can be performed. Once enough scintillator tiles are available it will be possible to setup a small calorimeter stack for use in the DESY testbeam and have a look at timing behaviour for a full readout chain including tiles and SiPMs.

5 Acknowledgements

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I hope to return to DESY as soon as possible.

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