



Source and beam tests of CMS pixel detectors

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Abstract

The DESY contribution to the CMS pixel detector upgrade requires the capability of testing the new detectors with X-rays, β rays from a source and with a test beam. This report describes the work on preparation of source and beam tests. For both tests the PSI46 test board was used and the existing software for control and readout was adapted to new conditions. The setup for the source test using a ^{106}Ru electron source and the internal trigger mode was built in the laboratory. The beam test was set up at the DESY II testbeam 21 using a beam of 2 GeV positrons and external triggering. The capabilities and characteristics of both test environments were analyzed and compared. Two present pixel chips were tested in order to check for the test procedures proper operation and a need for synchronization of test board with the beam was discovered. The set working points of the present chips were also confirmed in the tests.

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1 Introduction

The Compact Muon Solenoid (CMS) is a general-purpose particle detector used in the Large Hadron Collider experiment in CERN. Its aim is to record secondary particles created in p-p collisions at 7 and 14 GeV center of mass energy. To allow for multipurpose capability the CMS consists of various types of detectors, i.e. the silicon tracker, electromagnetic and hadronic calorimeters and muon chambers. The barrel of the silicon tracker is formed by three layers of pixel detectors and ten layers of silicon strip detectors. Since the pixel detectors offer the highest particle momentum resolution in three dimensions, they play a crucial role in the reconstruction of particle tracks and secondary reaction vertices. In the planned upgrade of the CMS new design of pixel chips will be used with extended data buffers to avoid inefficiency of the detector with at high luminosity. The prototype chips of new design will need extensive testing to discover their properties. Moreover, current 3 pixel layers will be replaced with 4 layers of pixel detectors to achieve higher resolution. The fourth layer will be built at DESY, therefore a setup for testing the new pixel modules is being prepared. All modules have to undergo an X-ray test for calibration and β radiation source for bump-bonding quality check. Sample modules will be also tested with the test beam of DESY II. This report describes the development of a the setup for source and beam tests for single chip pixel detectors.

1.1 CMS silicon tracker

Since the silicon detectors offer a high momentum resolution and small contribution to the radiation length, they are placed directly around the beam pipe of the LHC and are used for precise reconstruction of particle tracks and vertices. Geometry of the tracker is divided into the barrel consisting of 11 concentric layers and two double-layer front detectors. Three innermost barrel layers consist of silicon pixel detector modules forming the pixel detector described in detail in the following section. The 10 outer layers are built of silicon strip detectors which can cover larger areas and retain high transverse resolution at a cost of low longitudinal resolution.

1.2 The pixel detector

Pixel modules (fig. 1(b)) are the main building blocks of the CMS pixel detector (fig. 1(a)). The three barrel layers consist of 672 such modules and 96 half-modules at the edges of half cylinders. The modules are mounted on a structure of aluminum cooling tubes and carbon fiber blades which ensure low material budget. The radii of subsequent layers are 4.4, 7.3 and 10.2 cm. This allows for a high precision in track reconstruction but also causes large radiation exposure.

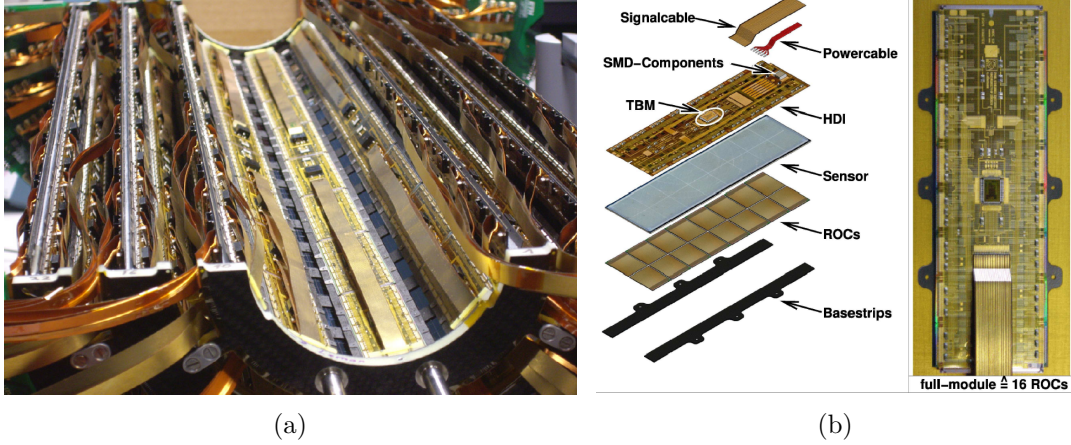


Figure 1: (a) CMS pixel barrel, (b) pixel module

1.3 Pixel chip module

Since the pixel detector silicon sensors are two dimensional arrays of independent pixels, the signal readout is more complicated than in strip detectors and performed by readout chips (ROCs) mounted below the sensor as shown in fig. 1(b). The layer of readout chips is $175\mu\text{m}$ thick and contains 16 readout chips organized in two rows. Each ROC contains the front-end electronics for every pixel of the sensor manufactured with the $0.25\mu\text{m}$ CMOS process. A single ROC reads out 4160 pixels of the $100\mu\text{m} \times 150\mu\text{m}$ size connected to their front-ends with bump bonds (fig. 2). The bump bonding process developed at PSI allows connection between sensor and ROC pixels with $25\mu\text{m}$ indium bumps placed with high precision of $3\mu\text{m}$. The High Density Interconnect (HDI) layer is glued on top of the sensor and provides the communication between all 16 ROCs. On top of the HDI a TBM is placed which is an ASIC module controller to coordinate the readout of the ROCs.

1.4 Single chip

The 4160 pixels of a single chip are organized in 52 columns and 80 rows and logically grouped in 26 double columns of 80 pixels each. The double column layout results from optimal buffer selection as all pixels of a double column share one common data buffer located in the periphery at one edge of the chip. The dimensions of the pixel are $100\mu\text{m}$ in the φ direction and $150\mu\text{m}$ in the z direction. This size and shape yields a high resolution for transverse momentum but is large enough to enclose the pixel front-end electronics on the ROC.

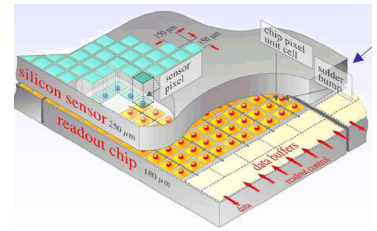
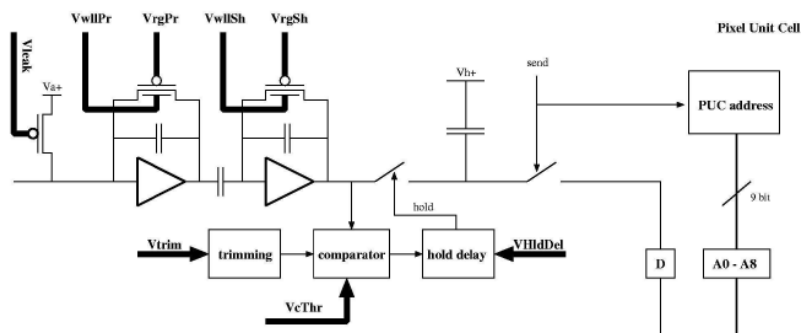


Figure 2: Connection of sensor and ROC

A single front-end cell scheme is shown in fig. 3. When an ionizing particle passes through the silicon sensor, electrons and holes are created and start a current pulse



which is directed into a preamplifier and shaper and further into a comparator. The charge deposit sharing between neighboring pixels can be analyzed to increase resolution however it requires that the pulse is read out in the analog form. As a result, the whole ROC communication and control is analog. The working point of the ROC electronics can be adjusted by 26 internal 8-bit registers whose values also need to be transferred into the ROC through a DAC and therefore are called DAC parameters.

A shaped signal is compared to the threshold (adjustable by DAC parameter **VthrComp**) in the comparator and further stored into a sample-and-hold capacitor. The hold delay is also adjustable by a DAC parameter **VhldDel**. The pulse is then read out by the periphery where it is stored and a time stamp is added.

1.5 Pixel chip readout and timing

Since the LHC design bunch crossing frequency is 40 MHz, the interval between bunch crossings (BC) is 25 ns which becomes a natural unit for data acquisition timing. The CMS tracker readout clock is also 40 MHz and the time stamp stored along with the pixel pulse height in the ROC periphery buffer is counted in units of clock cycles. The hit data can only be read out from the buffer if it is validated by the appropriate 1st level trigger signal which comes from other CMS detectors. For this the time stamp of an incoming trigger signal has to vary from the hit time stamp by a fixed number of bunch crossings called WBC. The WBC is one of the adjustable DAC parameters. In CMS the first level trigger latency is fixed at about $3.4\,\mu\text{s}$ which leads to well defined WBC=135 but in test conditions when the trigger is generated otherwise and with setup-specific signal delays, determining the proper WBC value is a crucial step for obtaining data readout from the chip.

2 General single chip test setup

2.1 Psi46 test board

For testing of chips and modules in laboratory conditions a PSI46 test board is used which emulates the real pixel detector readout of CMS tracker (fig. 4). The board has

its own 40 MHz clock and an FPGA controller for communication and readout of data which are then stored into a 64 MB memory. The readout and communication with a PC computer is done via USB 1.1 interface. Both a single chip and a whole module can be connected to the board using special adapters, however for the setup preparation only single chips were used. High bias voltage of up to -100 V is also supplied to the chips sensor through the test board.

The FPGA can operate in two trigger modes. In the internal trigger mode an artificial trigger signal is generated by the FPGA in regular time intervals based on the board clock. The external trigger mode allows the use of an external particle detector to generate a trigger signal corresponding to a real particle hitting the chip. The PSI46 test board has both analog and digital input for the trigger signal. In this work the digital input was used which interfaces directly one of the FPGA inputs. Therefore the trigger was always passed to the board as a 3.1 V TTL signal.

Currently there are two issues concerning the data taking with the PSI46 test board. One of them is a slow USB 1.1 interface due to which transfer of the full memory content takes about 90 seconds. This means after every memory fill the data taking will have to be stopped for a long transfer time. Nevertheless, for the introductory tests described in this report usually short single runs of 10–100 s were taken so that the board memory was not filled. A second issue are corrupt data blocks which often occur in the taken data. They may cause a huge part of the data to be uninterpretable which strongly affects the data taking efficiency. The reason of the data corruption has not been explored yet.

2.2 Software

2.2.1 The *takeData* program

The board was controlled by a *takeData* program running on a 64-bit Linux PC. Several changes and improvements were introduced to the *takeData* code developed at PSI to adapt it to the current testing conditions. The program allows for setting the DAC and timing parameters online and for taking the data in both trigger modes either for a stated amount of time or until the tesboard memory is filled. After data taking it coordinates the readout of raw data from the memory via USB and saves it a binary file. The data downloaded with *takeData* is then not processed in any way and for its analysis separate software is used.

2.2.2 The *b2h* program

The raw data from the binary file is analyzed offline with a program called *b2h* (*binary to histograms*) created by Daniel Pitzl basing on the offline analysis code from PSI. The first task of offline analysis is to reject the corrupt data mentioned above. After checking for the proper data header structure a full rejection of corrupt data was achieved. In the remaining data the program identifies the hits recorded by pixels. Single hit data contain the pixel address and the pulse height in ADC values. The address consists of double column and row numbers transferred as analog values encoded using a 6-level

system. Therefore they are decoded using chip-specific level ADC ranges. Since the gain and signal offset of the preamplifiers may vary between pixels of the chip and between chips, the calibration of analog pulse height is applied by the *b2h* program. This yields the information on the charge deposited by the ionizing particle in the sensor pixel.

In fact, the deposited charge can be shared by several neighboring pixels, either if the sensor bias voltage is not high enough for well charge separation or if the particle incidence angle to the sensor is low. The latter is used to increase the resolution of the detector. Thus, rather than pixel hits, the information on clusters of neighboring pixels hit in one trigger, is needed. The *b2h* program performs a simple cluster analysis. For each trigger with hits (later called an event) it starts from a hit pixel and searches for hits in neighboring pixels, allowing a gap of one row or column. The hit pixels are adjoined to a cluster and their neighbors are then checked. Thus, a cluster of pixels is identified. The total charge deposited in a cluster is counted and a central pixel weighted by charge is determined.

The information on the pixel hits and identified clusters is visualized as histograms of the distributions of most interesting values. Those histograms are stored in a ROOT binary file which is created by *b2h* for each data taking run.

3 Source test

3.1 Setup

The principle of every test of a pixel silicon detector is to irradiate it with ionizing particles of known properties and analyze the response of the detector. A source test uses a small β radiation source to irradiate the chip with electrons. In this work a Ruthenium 106 source was used which emitted electrons of 3.5 MeV in the decay chain $^{106}\text{Ru} \rightarrow ^{106}\text{Rh} \rightarrow ^{106}\text{Pd}$. The activity of the source measured with a scintillator was about 15 kHz.

The setup for the source tests is shown in fig. 4. The source was mounted above the detector as close as possible to its surface but still high enough to irradiate the whole sensor. An attempt was made to use an scintillator with a PMT placed below the chip as a source of external trigger but the energy of electrons was not high enough to pass the chip and the adapter board and reach the scintillator. Therefore the internal trigger mode was used for the source tests. A similar procedure is used for X-ray tests since measurement of X-rays is destructive and external triggering is not possible. Since the internal trigger does not correspond to a passage of a certain particle, a hit can only be recorded by random coincidence. To increase the probability, the FPGA on the test board allows for clock stretching. The clock cycle corresponding to the trigger diminished by WBC can be stretched by a factor of up to 2^{16} from the standard 25 ns value. Thus the time window duration for hits which will be validated by internal trigger can be even $2^{16} \cdot 25 \text{ ns} = 1.6384 \text{ ms}$. In the measurements described below time stretches of 1 ms and 0.5 ms were used which results in multiple clusters recorded per event. With a time window of 1 ms the internal trigger rate should be 1 kHz and the rate of 890 Hz was

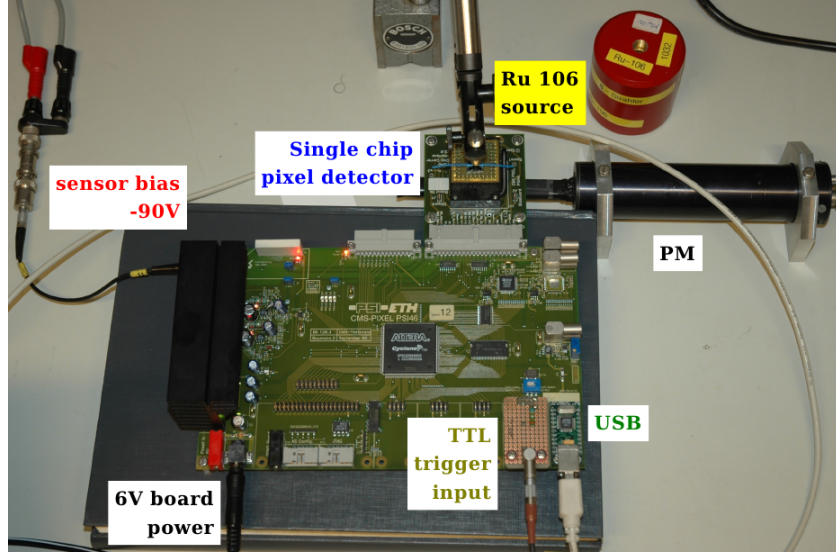


Figure 4: PSI46 testboard and the setup used for source tests.

measured which indicates a very good 89% duty cycle of the FPGA with the internal trigger.

3.2 Bias voltage scan

A scan of bias voltage scan applied to the sensor was performed for three chips labeled 6,7 and 8. The bias voltage was varied from 0 to -100 V in steps of 10 V. For every voltage the hits were recorded for 10 s with the source. The binary files with raw data for every run were analyzed with the *b2h* program and ROOT files were created. Since the corrupt data blocks sometimes cause a huge loss in taken data, the amount of well identified hits was controlled and bad runs were repeated.

For analysis of this and future scans a ROOT script was created which opens the ROOT files for every bias voltage value and creates graph of mean values of pixel pulse height, cluster charge, cluster size and numbers of hit pixels and clusters per event vs. bias voltage. Some of the results are shown in fig. 5. The cluster efficiency reaches a wide plateau already at -50 V. This is because the low energetic source electrons deposit a large amount of charge in the silicon so that even relatively small bias voltages are enough to collect some charge and record a cluster. The average cluster charge decreases with the absolute bias voltage because charge collection is less effective, but it is stable for voltages below -80 V. A difference of plateau levels between various chips for both cluster efficiency and charge can be seen, which is caused by different threshold setting used for the chips. The alignment of chip and source could also have influenced the differences since it was set manually for each chip and was not perfectly reproduced. The calibrated cluster charge for chip 7 is not presented because it requires gain and offset calibration data which was not taken due to chip 7 malfunction. This is also why later only chips 6 and 8 were tested with the beam.

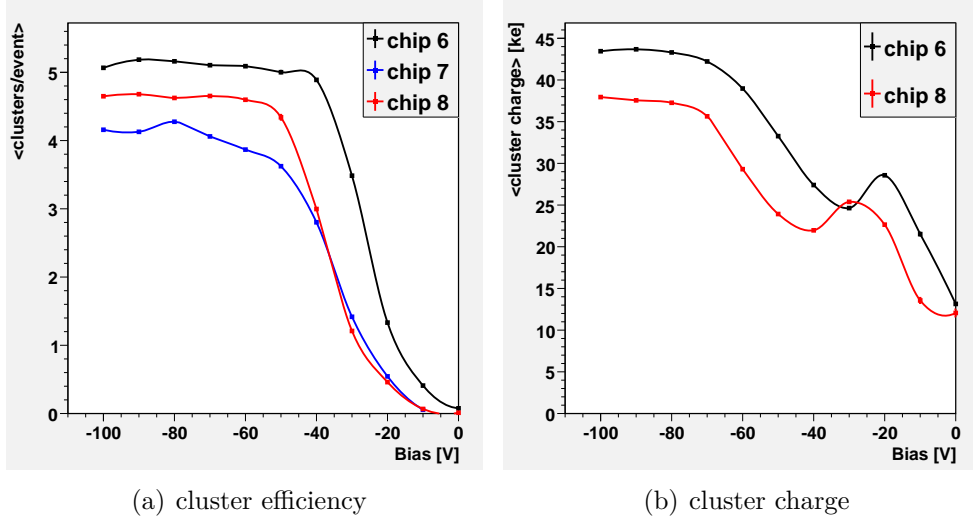


Figure 5: Results of bias voltage scan with source.

3.3 Threshold scan

Similarly to the sensor bias voltage, the strength of the threshold applied to the pixel analog pulse was scanned for chip 8. The V_{thrComp} DAC parameter states the level of threshold applied to the negative pulse, thus its higher value corresponds to a softer threshold. It was found out that the available threshold range is between 30 and 130 DAC. For thresholds stronger than 30 no hits were recorded with the source used and thresholds softer than 130 yielded empty readouts. This results from threshold being at the level of preamplifier baseline signal and continuously recorded hits overflowing the buffers which causes the buffer to reset. The available range was scanned with steps of 10 DAC and runs of 10 for each step with the bias voltage fixed at -90 V. For analysis of the scan a ROOT script was created similar to the bias scan script plotting the same set of quantities vs. threshold level.

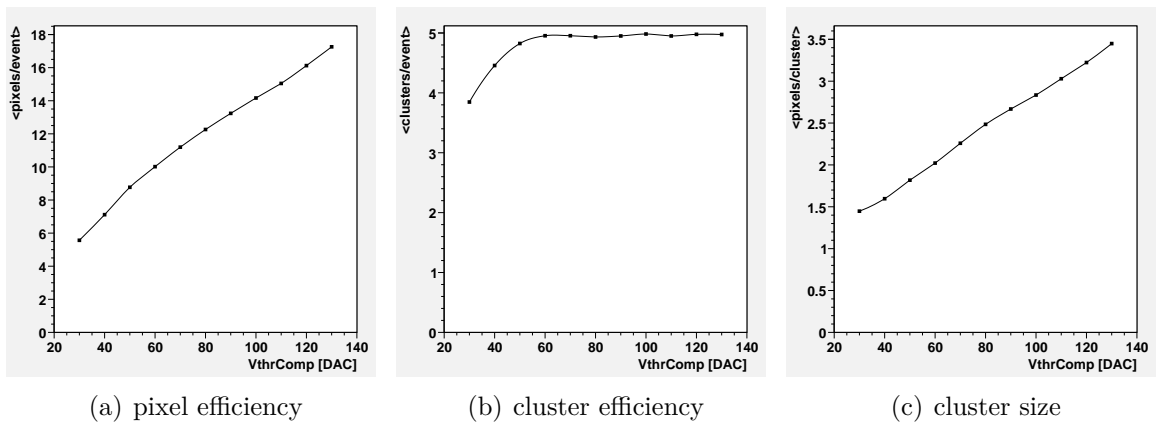


Figure 6: Results of threshold scan with source.

Figure 6 shows several results of the scan for chip 8. The linear pixel efficiency growth with softer thresholds is obvious since the threshold is applied to single pixels. The cluster efficiency, however, exhibits a plateau extending for most thresholds but the strongest ones, for which a drop in efficiency is visible. This is because most clusters contain pixels with high charge deposited, which are above threshold and are only cut off by the strong threshold. Nevertheless the clusters also have a halo of pixels with all charges which are subsequently rejected by the harder thresholds, causing a linear decrease in cluster size. All these results appear as expected for the source test conditions.

3.4 Cluster charge distribution

The source test is easy to perform in laboratory conditions and will be applied to all pixel chip modules used for the CMS upgrade to test for correct bump bonding and overall quality. However, more sophisticated tests such as the hold delay and trigger level scan need particles with a narrow and well defined energy spectrum which cannot be achieved with a low-energetic source. For this reason the beam tests are necessary.

Figure 7 shows the cluster charge distributions for measurements of source and testbeam radiation with the same chip and the same working parameters. Since the number events recorded in a run depends on the appearance of corrupt data in the readout, the vertical scale of the plot is not normalized. Nevertheless, the width difference of both energy spectra is clearly visible. Because of the small energy, the source electrons deposit larger charge amounts in the silicon sensor while relativistic beam positrons most often deposit about 26 ke thus being close to the Minimum Ionizing Particle charge deposit of about 24 ke for a $285\text{ }\mu\text{m}$ thick sensor. It is essential for precise scans of parameters like threshold and analysis of the analog output to use particles about the MIP because the preamplifier already saturates at about twice the MIP charge deposit.

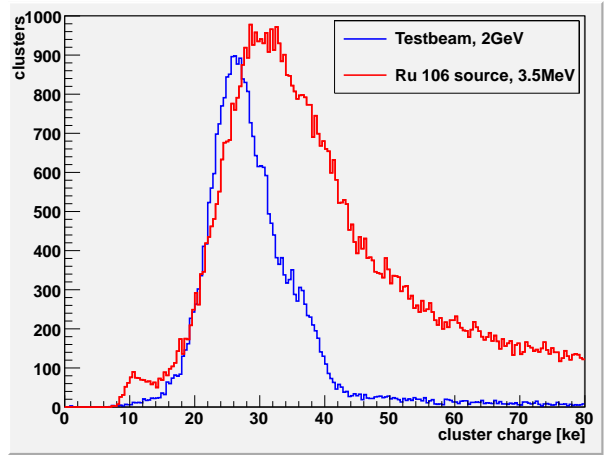


Figure 7: Cluster charge distributions for source and testbeam. Vertical scale is not conserved. $V_{\text{bias}}=-90\text{ V}$, $V_{\text{thrComp}}=100\text{ DAC}$.

4 Beam test

4.1 Setup

For the beam test a positron test beam from DESY II synchrotron was used. The principle of test beam generation is shown in fig. 8(a). A carbon fiber target is put

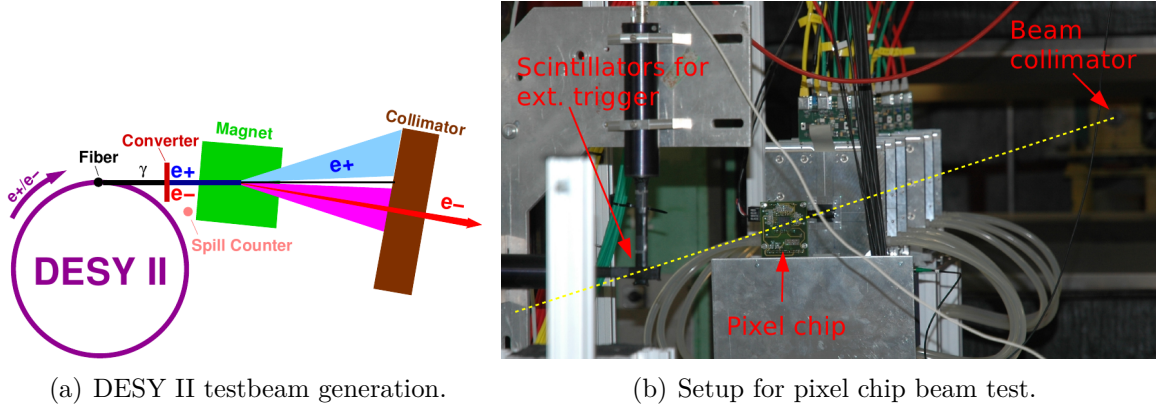


Figure 8: Testbeam details

in the way of DESY II positron beam to generate bremsstrahlung photons which hit a copper target and create e^+e^- pairs. The positrons of the desired energy are then chosen from the secondary beam with magnetic field. Finally the beam is distributed to the experimental area through a controllable shutter and a collimator.

Figure 8(b) shows the setup used for beam tests. The detector subject to the test is placed in the beam behind the EUDET telescope. Below the test board is mounted on a metal holder. 72 cm behind the detector two crossed finger scintillators are also in the beam. Coincidence signal of both of them is used as a source of external trigger. The trigger signal is delayed by an adjustable amount of time Δt and converted to a 3.1 TTL pulse before being passed to the test board. The finger scintillators are mounted on a mobile platform which allows the position adjustment with 0.2 mm precision. The horizontal and vertical position of the scintillators was varied with beam present and for each position the rate measured by both scintillators was noted. Thus, the beam profile was determined as shown in figures 9(a) and 9(b). The scintillator perpendicular to the scan direction showed a significant change in the rate while the parallel scintillator rate was stable during the scan. However, in the vertical scan, the edge of the vertical scintillator was reached, which resulted in a drop in vertical rate (fig. 9(a)).

For proper triggering, the detector and the scintillators intersection area have to be well aligned and the proper WBC value has to be found. The correct WBC depends on the trigger delay Δt_{cables} gained on cables etc., the adjustable trigger delay Δt and software trigger delay added by the FPGA $\Delta t_{software}$:

$$WBC = \Delta t_{cables} + \Delta t + \Delta t_{software}$$

The software delay was set to 85 BC. A scan was performed for both spatial dimensions and the WBC to find the proper alignment in space and time. The optimal parameters were determined as shown in table 1. Comparison with fig. 9 shows this position is still close to the maximum of the beam profile.

The detector dimensions are $0.8 \times 0.8 \text{ cm}^2$ and the triggering scintillator intersection area is about $1 \times 1 \text{ cm}^2$ therefore the geometrical acceptance should be at most 64%. In fact, the total measured acceptance was about 45%.

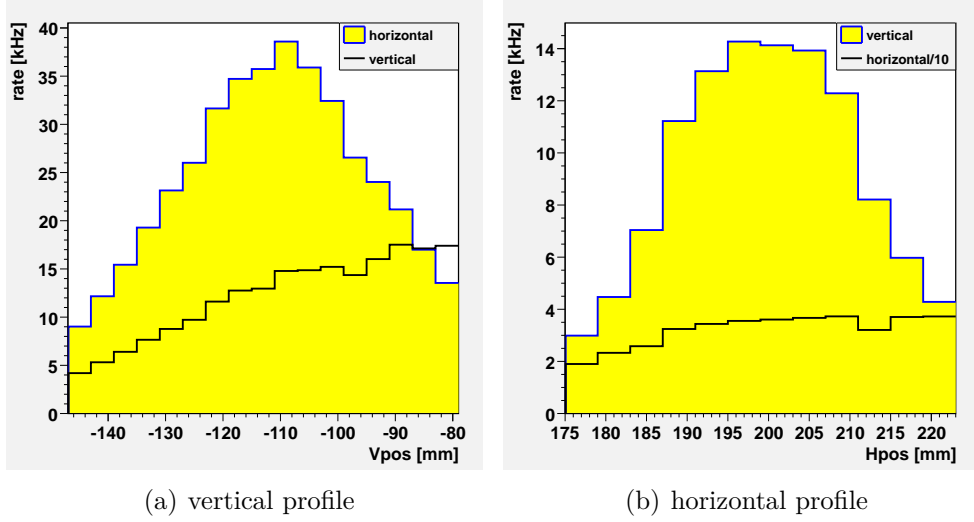


Figure 9: Beam profile of DESY Testbeam 21 measured at the mobile scintillator platform. The profiles were sampled with the perpendicular scintillator rate.

Table 1: Optimal alignment and WBC for the beam test

X position [mm]	Y position [mm]	WBC [BC]
193	-111	119

4.2 Bias voltage scan

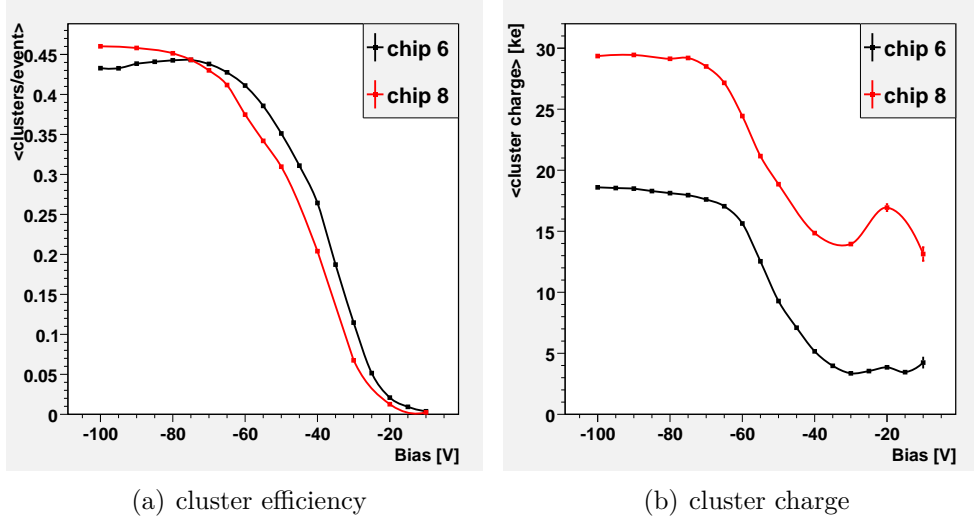


Figure 10: Results of bias voltage scan with the test beam.

The impact of the sensor bias voltage on several qualities of the detector operation was

scanned with the test beam similarly as with the source (sect. 3.2). 2 GeV positrons were selected from the secondary beam. This energy yields a maximal possible scintillators coincidence rate of 7 kHz. As this is twice smaller than in the source test and due to the 45% acceptance data taking runs were now extended to 50 s.

It was discovered that the PSI46 test board can only work with external trigger with the `TBMEulator` option switched on. In this mode the analog values passed from the ROC to the test board are larger by a form factor of 4 which was included in the `b2h` program. The ROOT scripts created for final analysis of the source data can also be used with beam data without modification.

Results of the bias voltage scan with the test beam (fig. 10) are generally similar to the source scan. The cluster efficiency, however, now only reaches the plateau at -80 V because the relativistic positrons deposit less charge in the sensor. The conformity of these results for both chips is now much better because of fixed alignment of the setup and the fact that chip thresholds had been optimized before the scan.

The average cluster charge dependence on the bias voltage is also similar to the previous result. The significant offset between two chips is caused by the imperfect calibration of preamplifier gain and offset.

4.3 Threshold scan

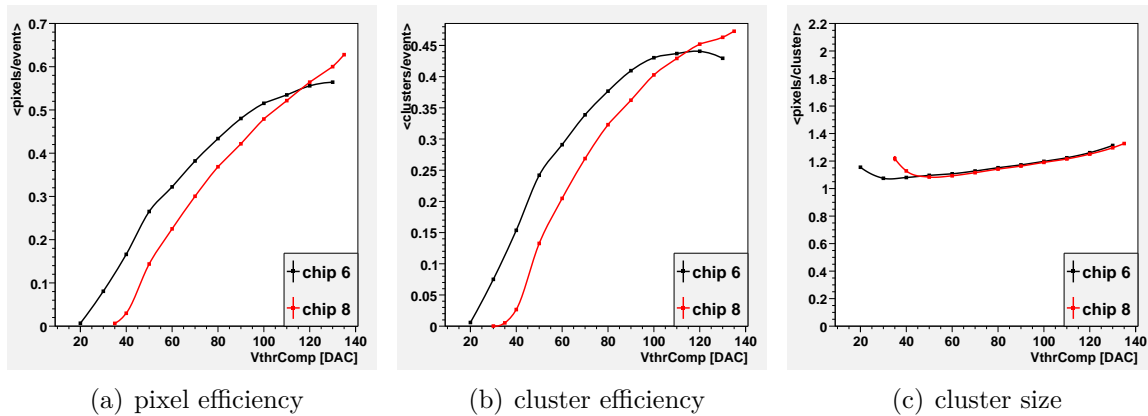


Figure 11: Results of threshold scan with the test beam.

The threshold scan was performed in the same conditions as for the bias voltage. Again the universal analysis procedures created for the source tests were used. Some results are shown in fig. 11. Since the beam positrons usually give one pixel clusters, the cluster size is stable around 1 with a very slight rise for softer thresholds. Therefore the pixel and cluster efficiencies are coupled and their similar behavior is not a surprise. Nonetheless, both decrease with harder thresholds while an abrupt drop was expected due to the narrow deposited charge distribution. This indicates that the charge spectrum is affected by unexpected small pulses. This observation confirmed the hypothesis that

the lack of synchronization between the test board clock and the beam causes timing issues. This effect is described in section 4.6.

4.4 Hold delay scan

The hold delay parameter states the time delay before the analog pulse is sampled and stored into a capacitor (see fig. 3). To obtain high analog output the pulses should be sampled at the maximum. The proper hold delay can be found by analyzing the analog output dependence on the varying `VhldDel` parameter. The result varies for different pulse heights as small pulses trigger the discriminator later than high ones, but a compromise has to be found. Such a measurement had previously been conducted using calibrate pulses generated by the ROC. The height of calibrate pulses can be adjusted by the `Vcal` 8-bit DAC parameter. Several pulse height had been used for the scan. With the test beam setup the scan was repeated using real pulses from the sensor hits. The beam results show a good conformity with calibrate pulse data for `Vcal`=200 DAC as shown in fig. 12. Basing on the measurements, a `VhldDel` value of 135 DAC was chosen as optimal for sampling pulses from MIP-close positrons at the maximum.

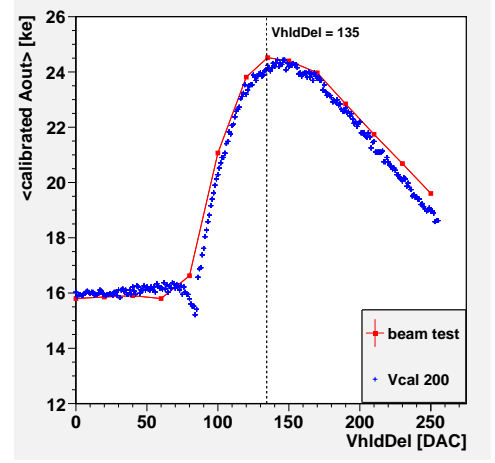


Figure 12: Hold delay impact on the calibrated analog pulse height for calibrate pulse (`Vcal` 200) and beam test.

4.5 Trigger delay scan

The external trigger delay could be adjusted with a nanosecond precision which should allow for the control of the pulses which are validated by a trigger. The time interval between high and small pulses reaching the threshold level can exceed one bunch crossing. For this reason, some valid highest pulses can be lost or small pulses from another event can be validated by the wrong trigger depending on the trigger delay value in a sub-bunchcrossing scale. For the WBC of 119 a trigger delay range of two bunch crossings around 71.2 ns was scanned to find the cluster efficiency maximum. Figure 13 shows the result which implies $\Delta t=70.0$ ns yields the best efficiency.

However, the cluster charge behavior observed in this scan is surprising. In the comparison in fig. 14

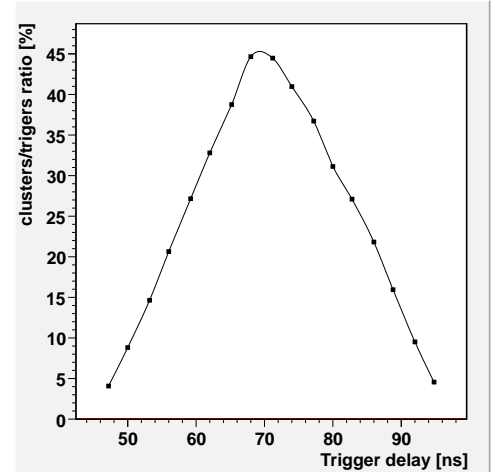


Figure 13: Cluster efficiency dependence on the trigger delay in a sub-bunchcrossing scale.

a rising peak of low charge clusters is visible for increasing trigger delays.

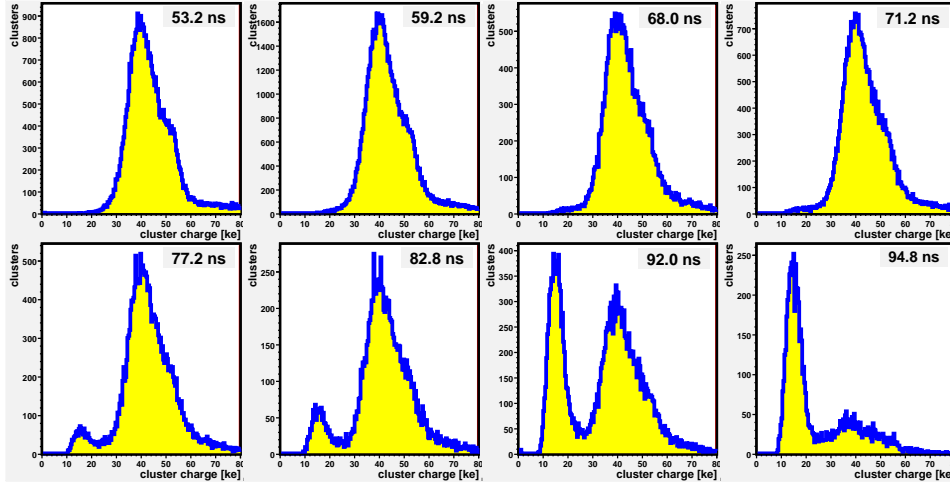


Figure 14: Cluster charge distributions for trigger delay varying in a sub-bunchcrossing scale.

4.6 DAQ and test beam timing

The DESY II synchrotron has a circumference of 292.8 m and accelerates a single bunch of positrons, thus a relativistic bunch rate is 1.024 MHz. The test board FPGA generates clock signal of 40 MHz, which means the secondary beam positrons can reach the detector every 39.068 clock cycles, which is visible on histogram of trigger time stamp differences in fig. 15. Since the data acquisition frequency is not an integer multiple of the beam frequency, the hits appear in various phases of the triggered clock cycle. Along with the trigger spread between high and low pulses this leads to migration of large pulses to the previous clock cycle and small pulses to the next one.

This issue can be fixed by synchronizing the test board clock with the beam frequency. This is possible as the FPGA provides the functionality of operating with an external clock frequency.

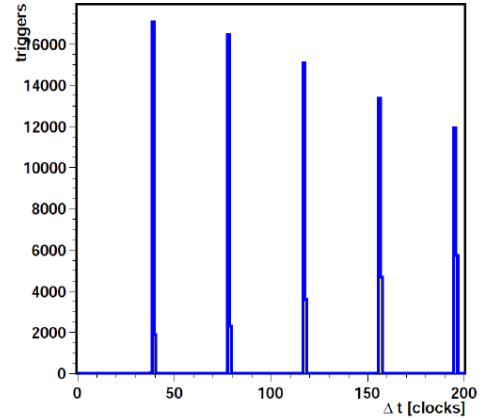


Figure 15: Intervals between triggers with the test beam.

5 Future perspectives

The basic procedures for testing of CMS pixel detectors with both β radiation source and the test beam have been established and necessary tools have been created. Two issues need to be fixed before further tests can be performed. First of them is the corrupt

data readout for which the reason has not been discovered yet and the second one is the lack of clock synchronization.

Future tests can involve a rotatable support for the test board and detector so that the beam incidence angle can be varied to observe and study charge sharing. Another desirable step is to conduct common measurements of the pixel detectors with the EU-DET telescope which is essential for resolution studies. Finally, an absolute preamplifier gain and offset calibration can be performed with the use of X-ray lines.

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