SILC: Silicon tracking for the International Linear Collider

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on behalf of the SILC R&D Collaboration

With many thanks for all the valuable contributions

Status Report for the PRC-DESY,

May 26-27, 2005

http://silc.in2p3.fr

Outline

- The Collaboration
- Goals
- The R&D activities
  - R&D on sensors
  - R&D on electronics
  - R&D on Mechanics
- The tools
  - Lab test benches
  - Test beams
  - Simulations
  - Alignement & calibrations
- Conclusions

The SILC R&D Collaboration

U.S.A

Michigan U.
SCIPP-UCSC

Close connections:

- **FNAL** (DOE prop 05) UCSC, FNAL, LPNHE
- **SLAC** (DOE prop 03: funded): UCSC, SLAC Michigan U, LPNHE and meetings

Europe

IMB-CSIC, Barcelone (SP)
Geneva U, Geneve (CH)
Helsinki U. (Fi)
IEKP, Karlsuhe U. (D)
Moscow St. U. , Moscou(Ru)
Obninsk St. U., Obninsk (Ru)
LPNHE, Paris (Fr)
INFN-Pisa, Pisa (It)
Charles U. , Prague (CZ)
Roma 1, La Sapienza (It)
IFCA, Santander(Sp)
Torino U., Torino (It)
IHEP, Academy Sci., Vienna (Au)

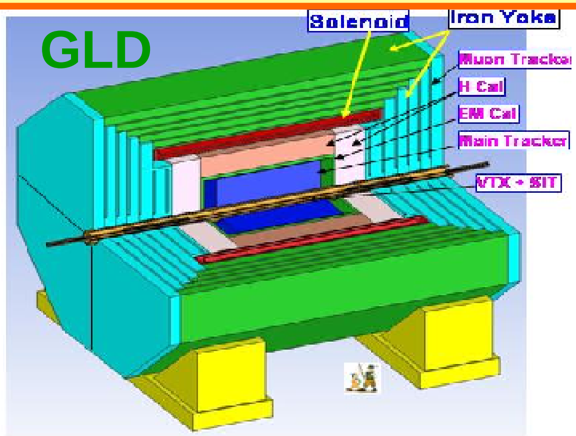
Asia

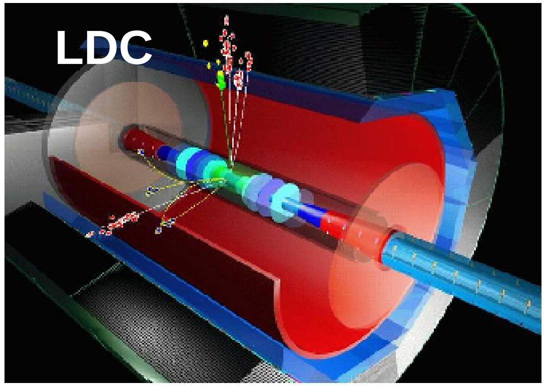
Kyungpook U. Taegu, Ko
Yonsei U., Seoul, Ko
Korea U. Seoul, Ko
Seoul Nat. U., Seoul, Ko
SungKyunKwan U. Seoul
Tokyo U. (Japan)
HAMAMATSU (Japan)

Launched January 2002, Proposal to the PRC May 2003
Several contracts of collaborations between Institutes, ex:
HPRN-CT-2002-00292, CICYT-IN2P3, IN2P3-Hamamatsu, DOE proposals, EUDET(?)
New teams in the 3 regions interested in joining.

R&D Goals

SiLC is a generic R&D collaboration to develop the next generation of large area Silicon Detectors for the ILC; It applies to all the detector concepts and indeed gathers teams from all 3 detector concepts:





- **Very high precision on momentum and spatial measurements**
- **Low material budget**
- **Robustness**
- **Easy to build and to work with**
- **Low cost**

❖ ***SILC R&D offers a unique framework to compare tracking performances between the various detector concepts.***

❖ ***Main difference between the detector concepts = tracking system***

R&D on Sensors

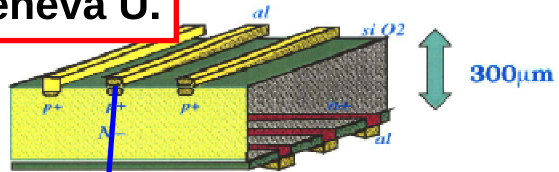
- **Silicon strips are the baseline with:**
  - **Larger size wafers**
  - **Thinner/Thinning**
  - **Smaller pitch**
  - **High yield**
  - **Eventually different shapes**
- **Possibility to use new technos in some regions:**
  Pixels, DEPFET, MAPS/FAPS, SOI …

1)Tests & results on Si strips

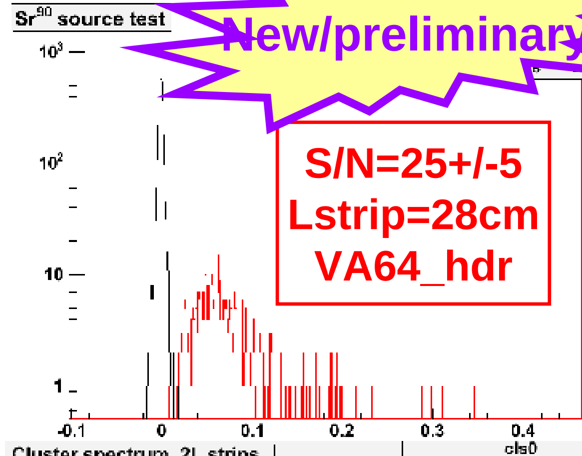
28cm x N=1,4

Built by Geneva U.

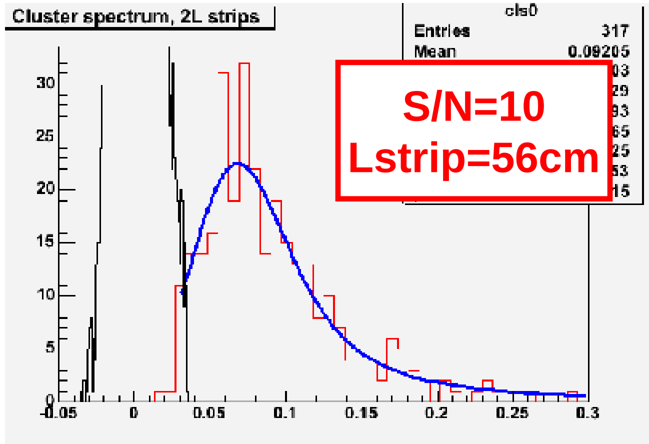
VA64_hdr
Tsh=3.7μs



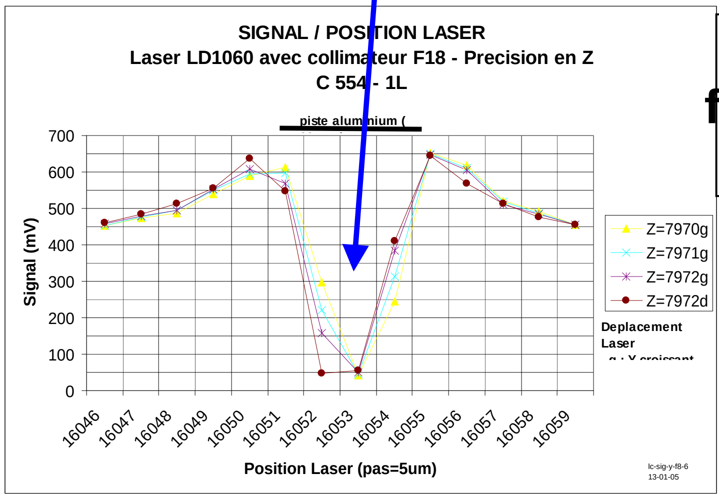
New/preliminary



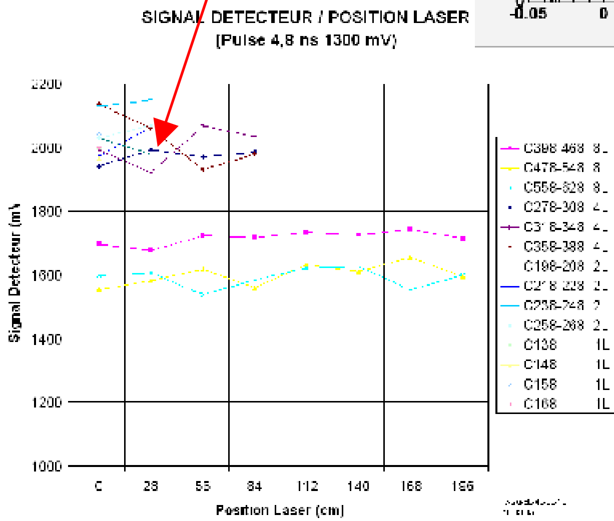
S/N=25+/-5
Lstrip=28cm
VA64_hdr



S/N=10
Lstrip=56cm



Same amplitude
for L=28 up to 112 cm
with Tsh=3.7μs

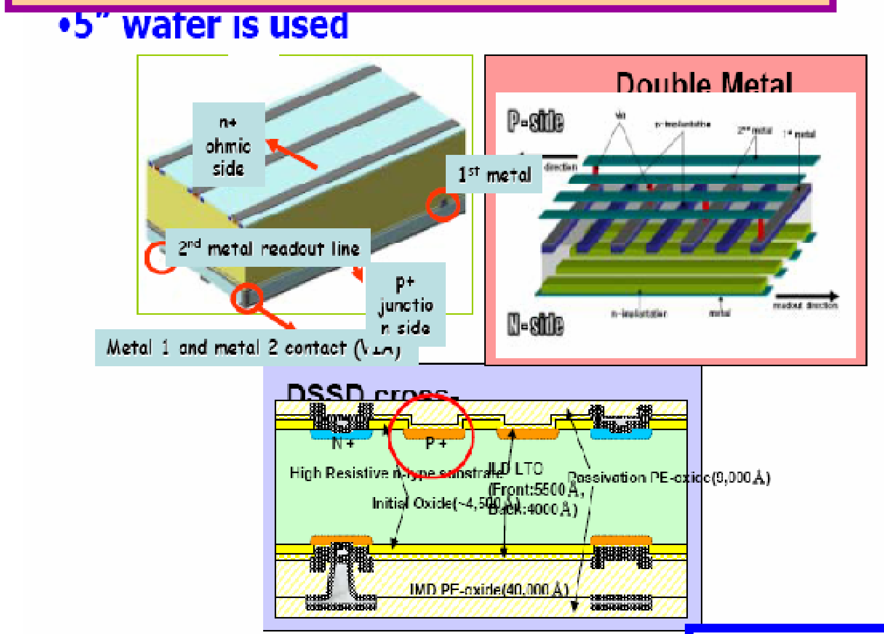


Paris test bench

Collaboration Paris-Prague

2) Development of fabrication line for new sensors

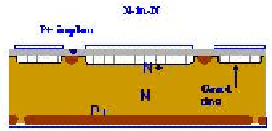
Ex1: 5’’ DSSD fab. line in Korean U.

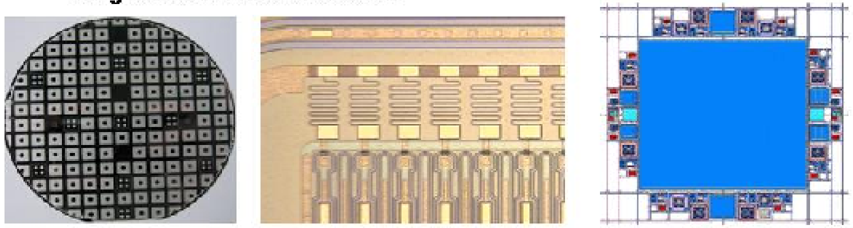


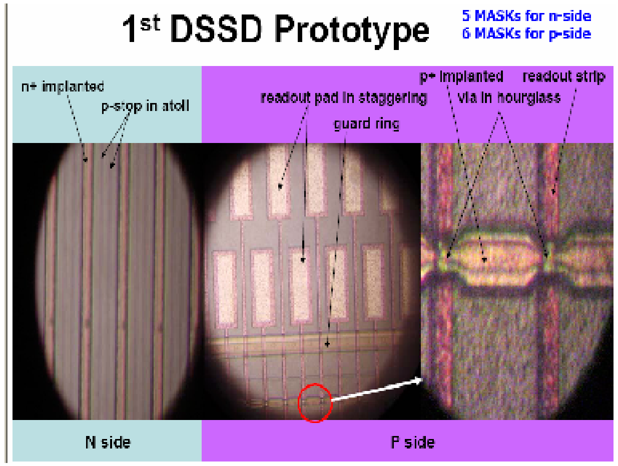
Ex2: rad hard sensor techno at IMB-CNM

Detector design and fabrication

- Technologies:
  - P-on-N, N-on-P, N-on-N
  - Pad, strip and pixels detectors
  - High resistivity poly, capacitive coupling, two metal layers, two side processing
  - Limited to 4 inches wafers
  - Radiation hard devices: Oxygenated FZ and magnetic Czochralski silicon.

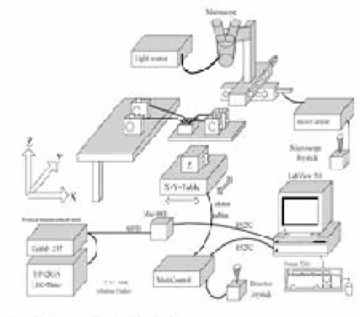






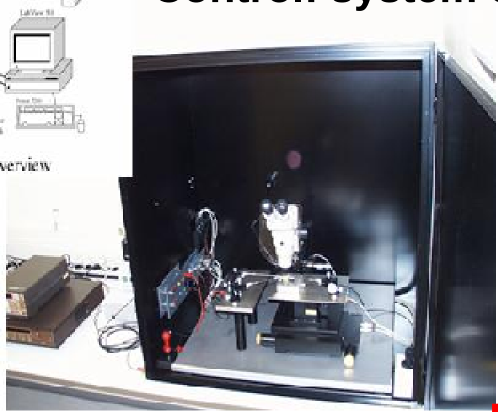
Several Institutions in SILC (also Helsinki U.) are developing new sensor research lines
Such facilities are very usefull for developing & testing new ideas and transfer to Industry.
For large production, high quality and reliability: HAMAMATSU Monopoly

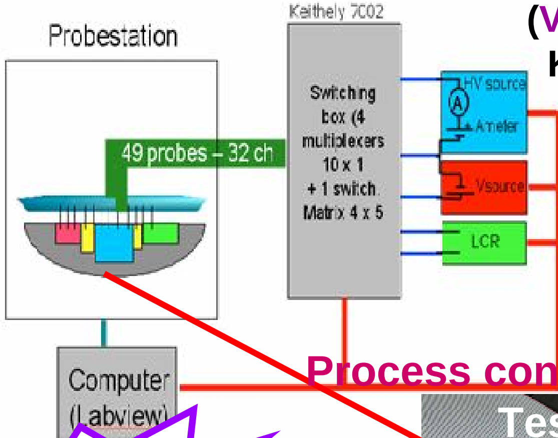
3) Process Quality Control and sensor characterization



Semi-automatic probe station - System overview

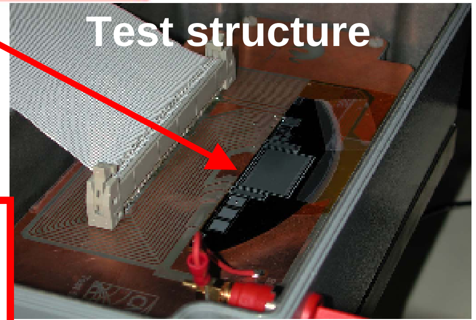
Semi-automatic sensor probe station for quality Control: system overview





(Vienna, Karlsruhe, Korea, Helsinki, Pisa ….)

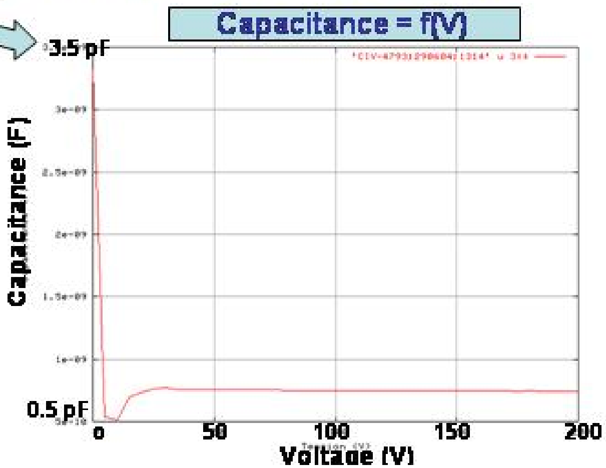
Process control scheme:



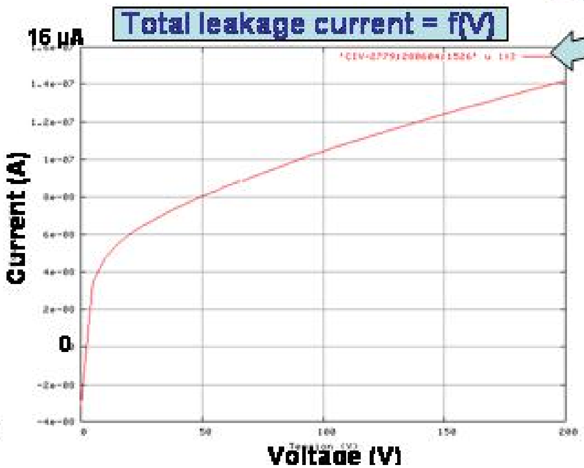
Essential for

- ➢Developing new sensors
- ➢Test of production

Total C_{sensor} as f (reverse bias), measured between backplane and bias line allows to extract the $V_{depletion}$ of the sensor & to check its thickness



Total leakage current as f (reverse bias), measured between backplane and bias line

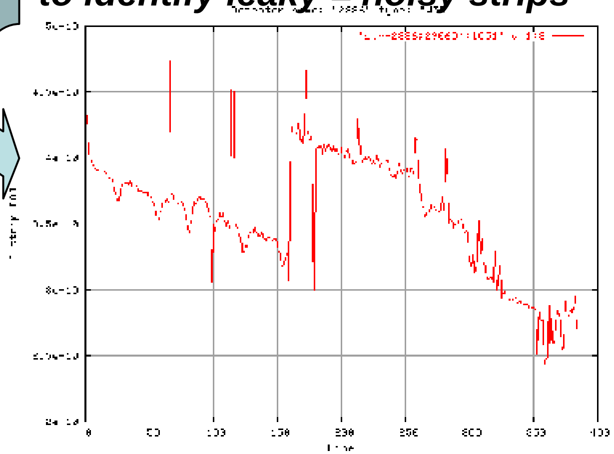


Test of 10 Hamamatsu det.
S8743 (GLAST)
8.9500+/-20 x idem µm
Strip pitch: 228µm
Nb of strips: 384
(done @Vienna PQC set up)

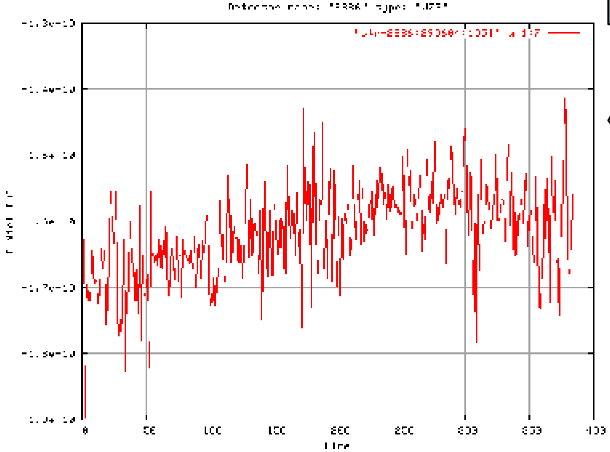
Test Quality on sensors (cont'd)

Strip-by-strip tests are performed at a constant bias voltage, and are aimed to identify defective strips (< 1%). All four tests are performed in the same scan, by contacting DC & AC pads simultaneously and by switching between different measurements.

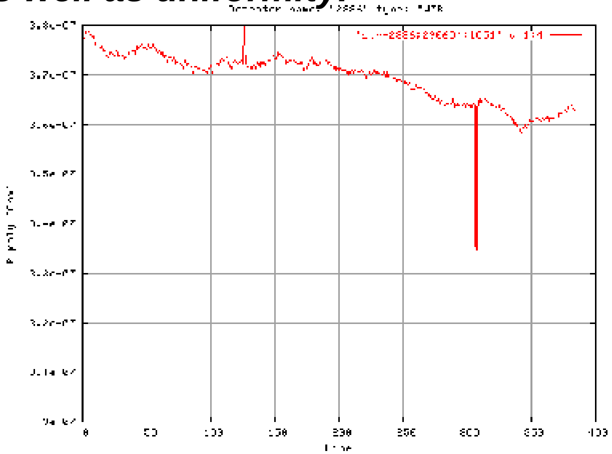
Leakage current of each strip ? to identify leaky = noisy strips



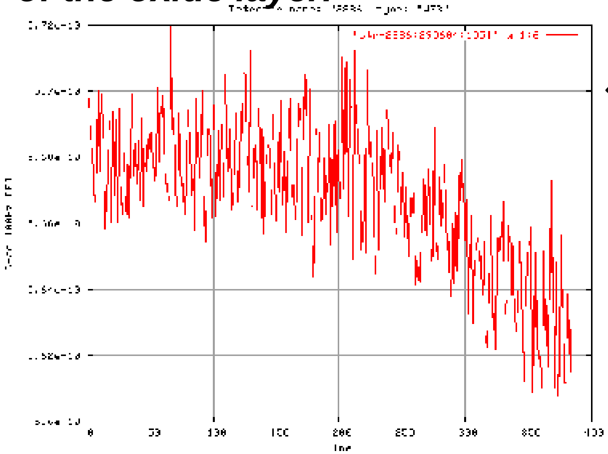
I_diel measurement identify pinholes.



Polysilicon resistor connecting strips to the bias line. The nominal value is required as well as uniformity.



Coupling capacitor for each strip is measured to check pinholes and monitor the uniformity of the oxide layer.



Tests at TQC in HEPHY-Vienna gives the 10 sensors are OK

R&D on Electronics

The Si tracking system: a few $100 m^2$, a few 10^6 strips
Events tagged every bunch (300ns) during the overall train (1 ms)
Data taking/pre-processing ~ 200 ms
Occupancy: < a few %

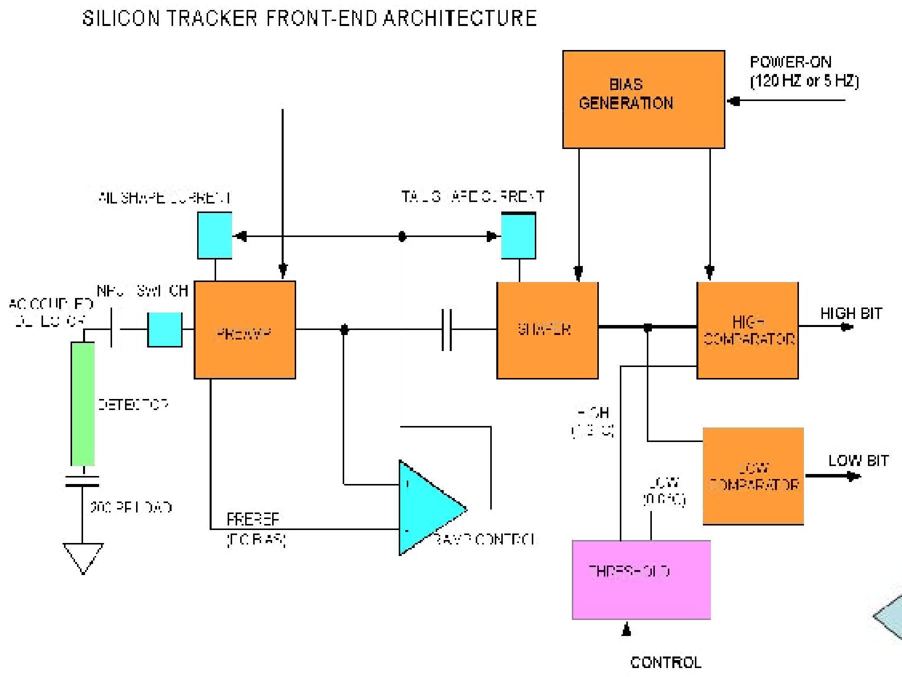
Goals:

Low noise preamplifiers
Shaping time (from 0.5 to 5 μs, depending the strip length)
Analogue sampling
Highly shared ADC
Digitization @ sparsification
Very low power dissipation
Power cycling
Compact and transparent
Choice of DSμE

NEW!!

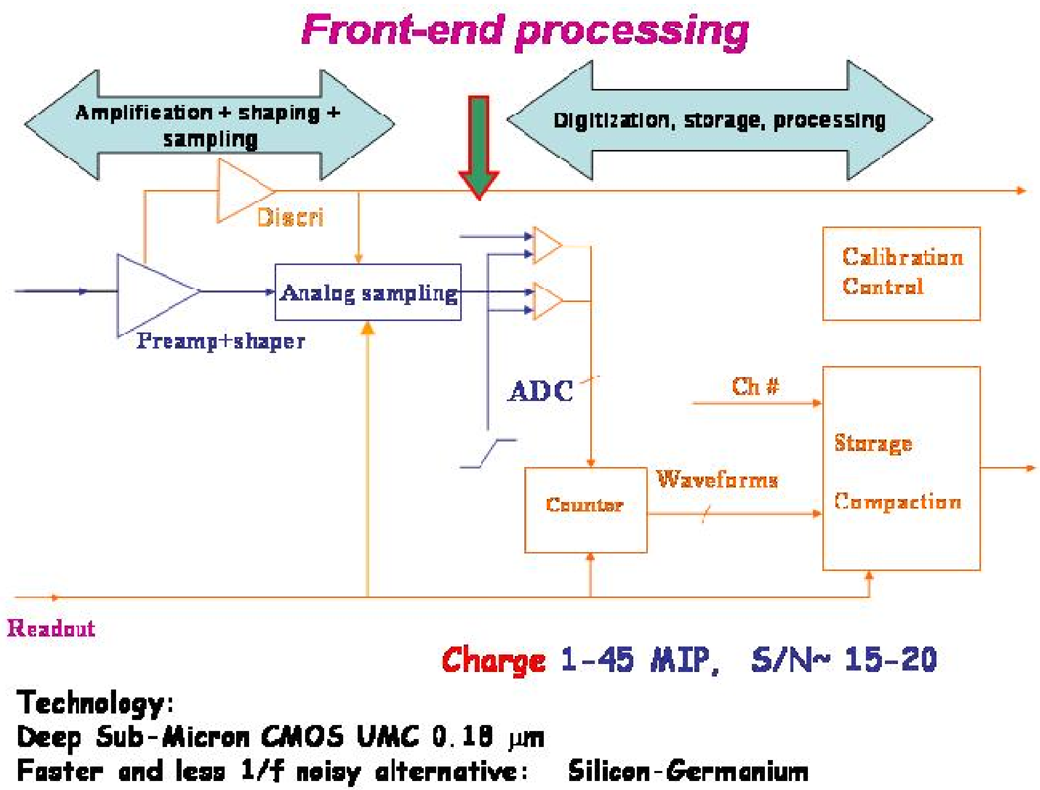
First LPNHE prototype fulfills most of these goals

Two designs



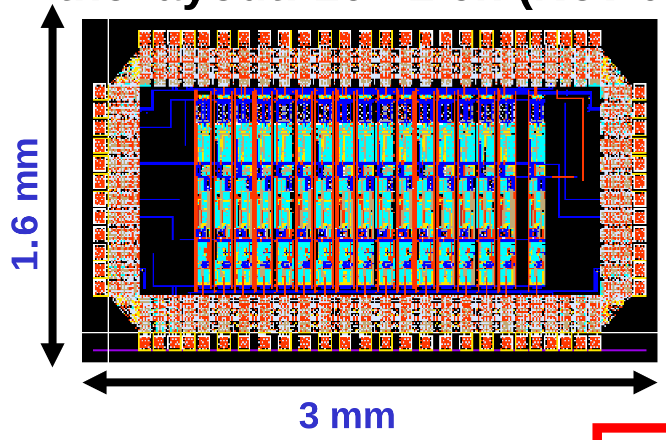
SCIPP-UCSC:
Double-comparator discrimination system
➢Charge by TOT
➢Improve spatial resolution (25%)
Next foundry: May 9.

LPNHE-Paris:
Analogue sampling+A/D, including sparsification on sums of 3 adjacent strips.
Deep sub micron CMOS techno.
First chip successfully submitted and now under test
Next version: in progress

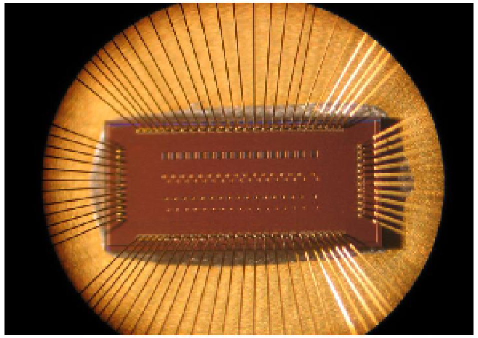


LPNHE chip: layout results & tests

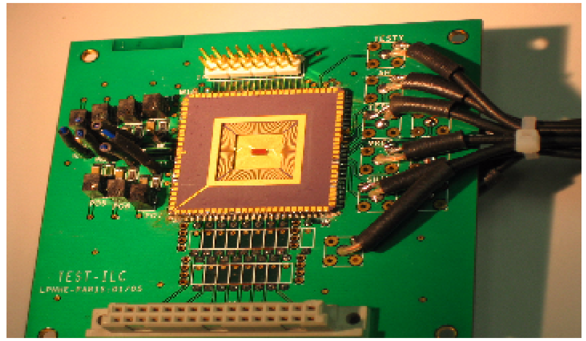
the layout: 16 +1 ch.(Nov 04)

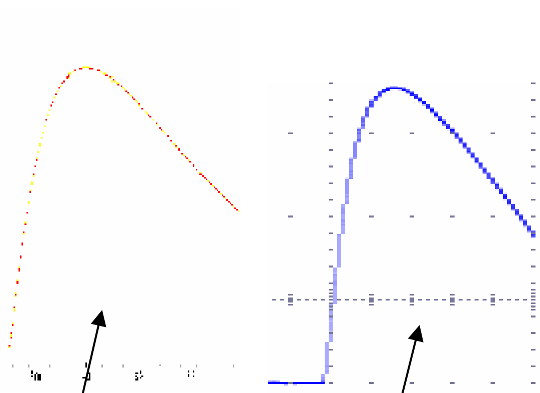


the chip (Feb 05)



the test board



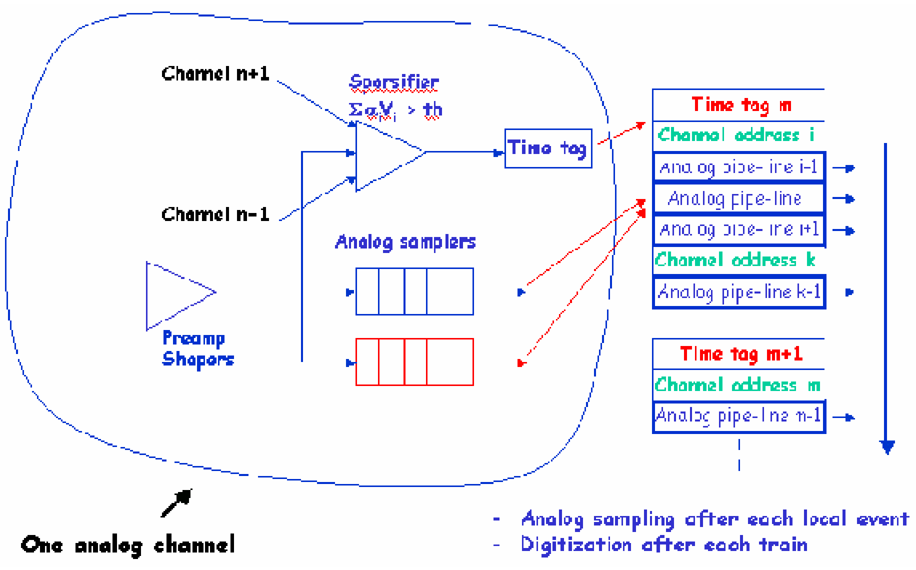


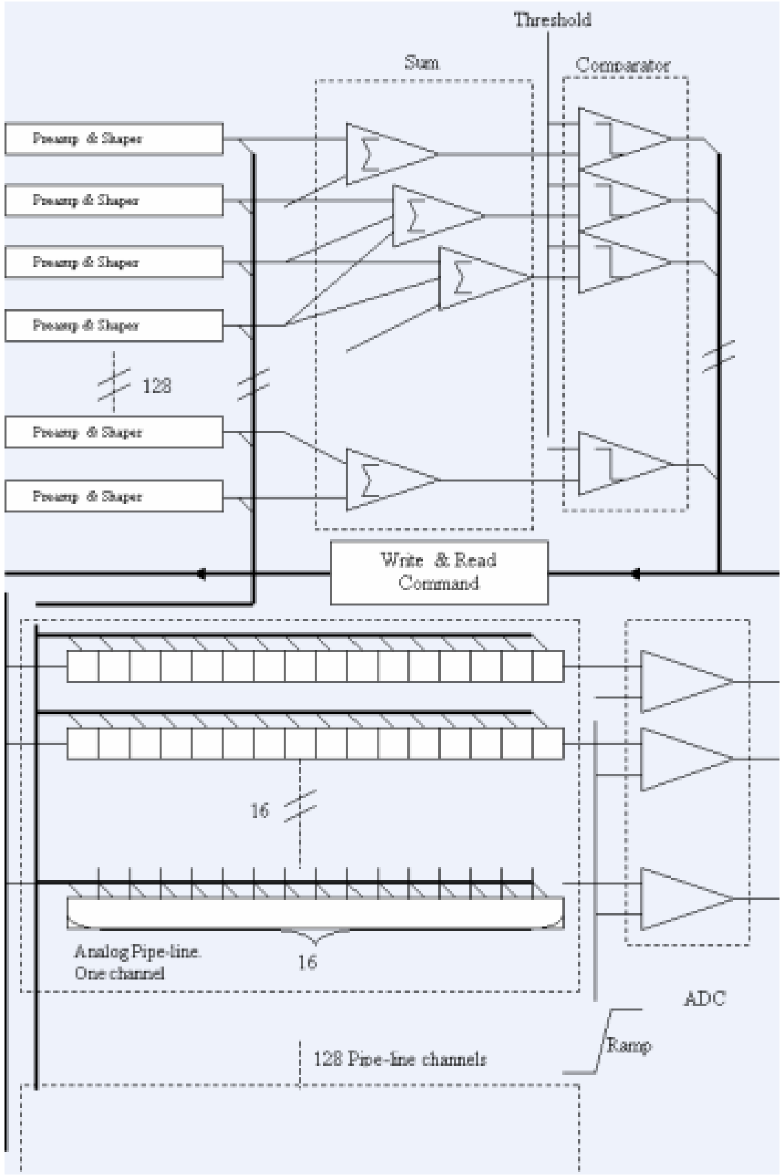
Shaper:
simu vs measurement

VERY ENCOURAGING FIRST RESULTS

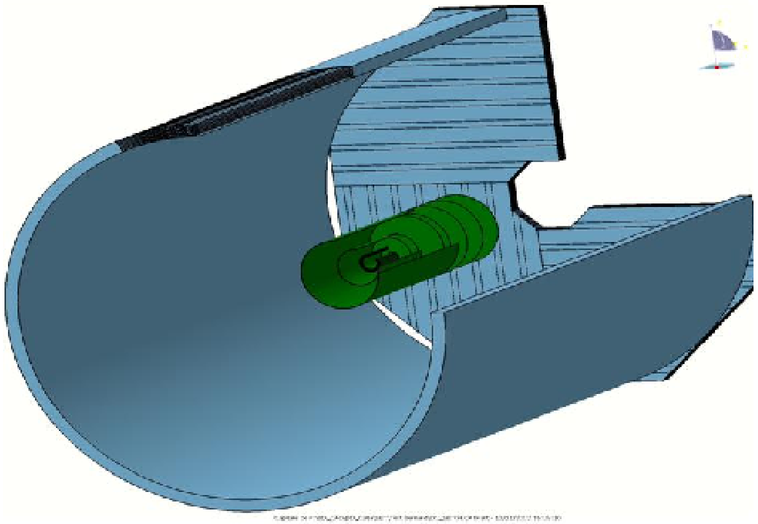
Preamp + Shaper			
	Preamp: Gain	8mV/MIP	OK
	Linearity	+/-1.5%	
	Dynamic range:	75 MIP	OK
	Noise @ 3.3pF input cap, 3 µs shaping time:		
		205 e-	140 e- expected
Shaper:	2 - 10 µs tunable peaking time		OK
Power:	Preamp	90 µW	70 µW expected
	Shaper	110 µW	OK

Second LPNHE prototype: underway





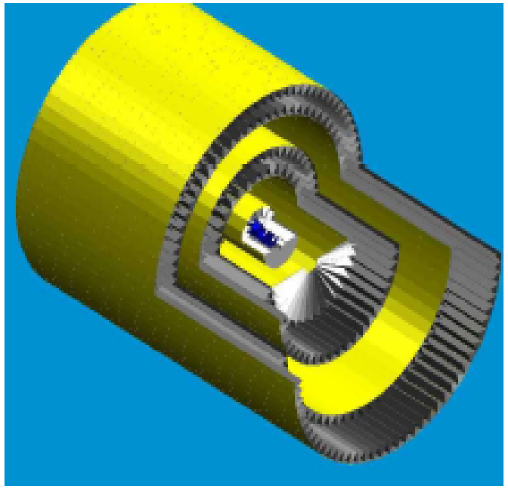
Next step: going to 128 channels with analogue sampling included; second chip prototype currently under design, foreseen submission Fall 05. Will equip the test beam prototypes



R&D on Mechanics

The aims of the R&D on Mechanics are:

- Low material budget
- Easiness of construction (simple modular structure, transfer to Industry)
- Robustness
- Low cost
- Integration issues



CAD design of the various components

- **The detailed CAD design of the various components of the Silicon Tracking system is studied for all detector concepts by SILC.**
  So unique place to compare detector performances

- **It allows to get a deep understanding of their feasibility, what are the problems and eventually how to solve them.**

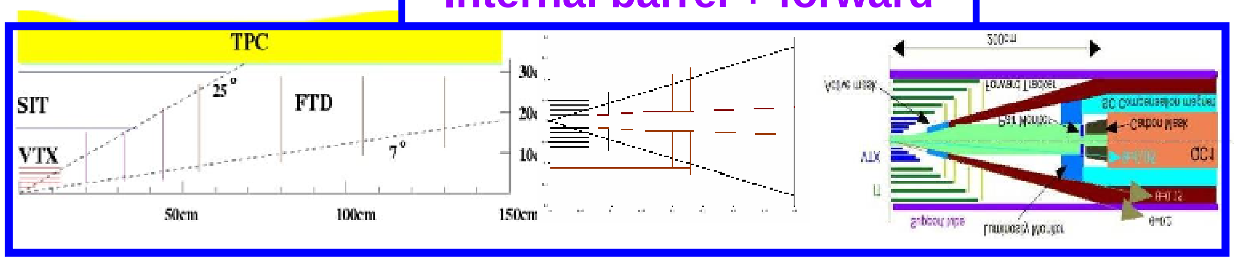
- **Ongoing brain storming on possible modifications of the baselines of the various detector concepts:**
  CAD tool essential for the quick follow up and response.

- **It allows to define DB geometry for GEANT4 simulations.**

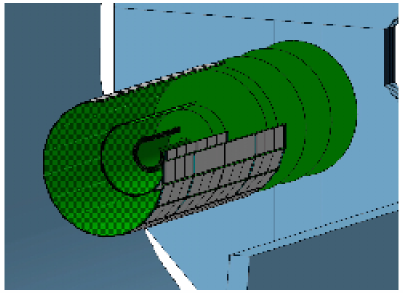
- **Although the main difference between detector concepts is the tracking system (TPC: Si or No?),** ***the design of the various components are very similar:***
  Barrel and Forward components for the Barrel and Large angle (Forward) regions

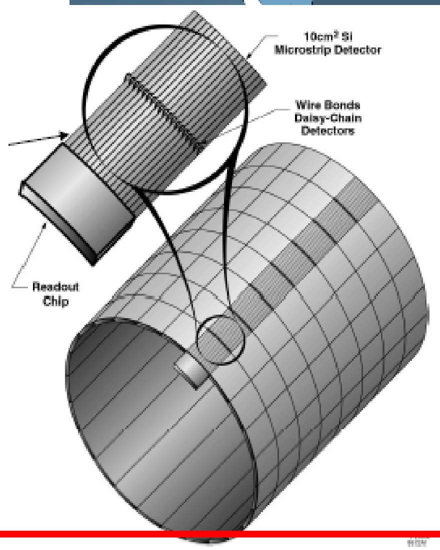
CAD of various components

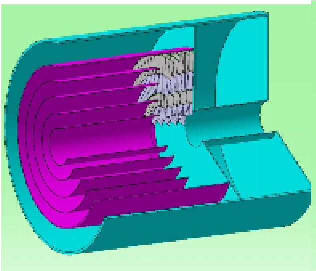
Internal barrel + forward

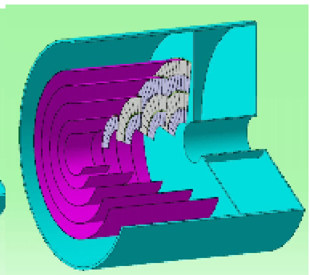


Barrel

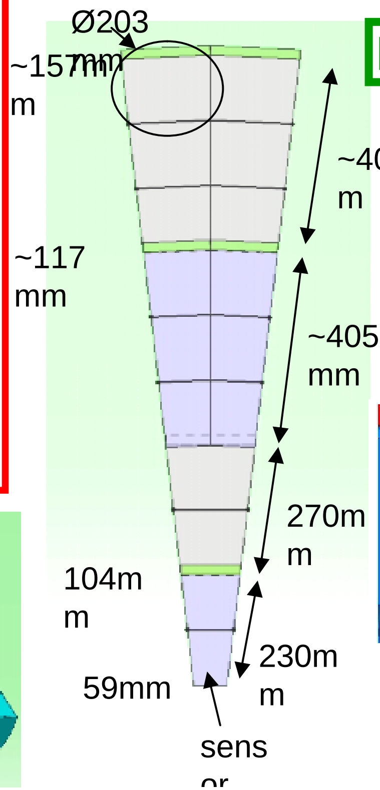




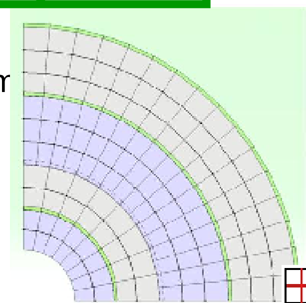


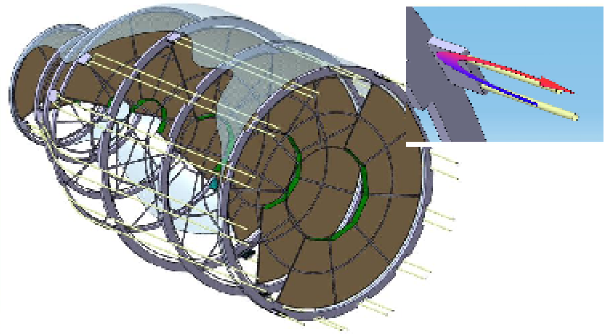


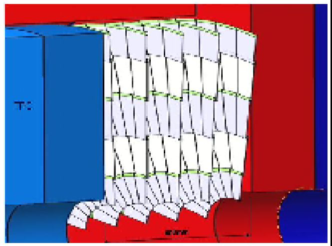
Forward components both internal and external are essential: Physics at Ecm=1 TeV is demanding highly performing tracking at large angles.
Lot of work going on

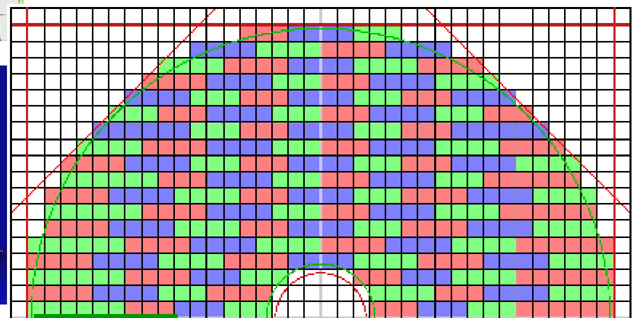


Projective

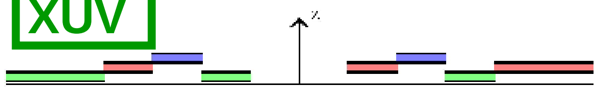






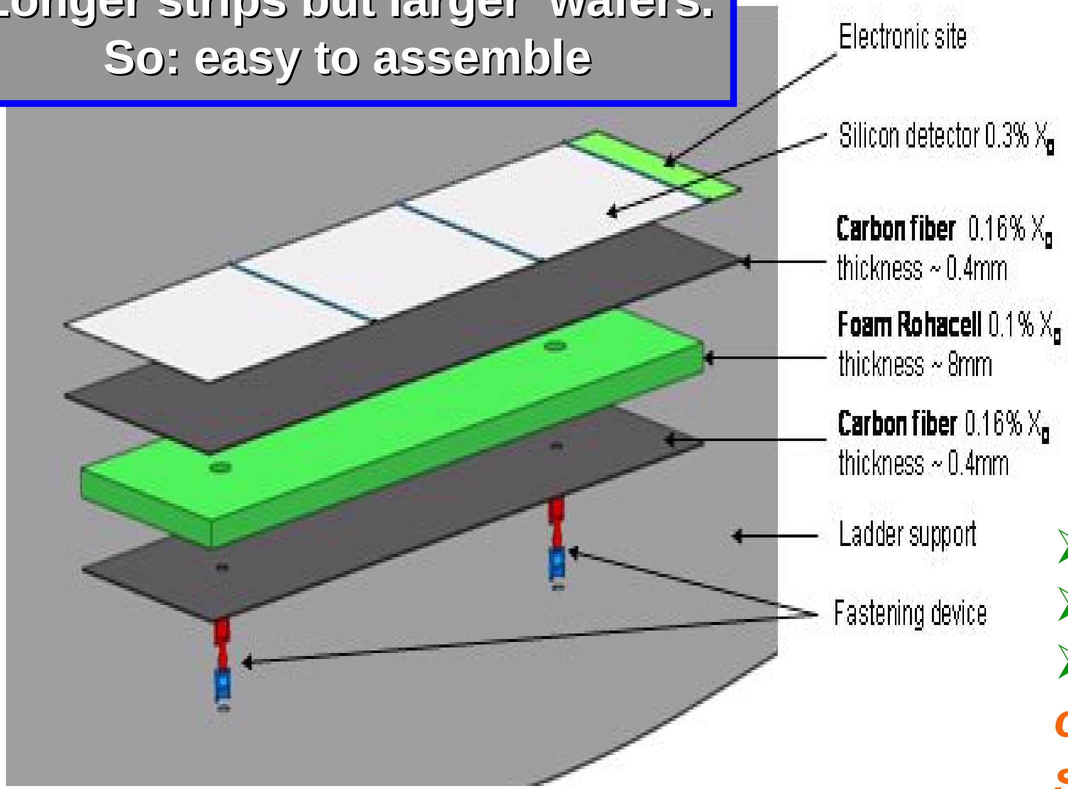


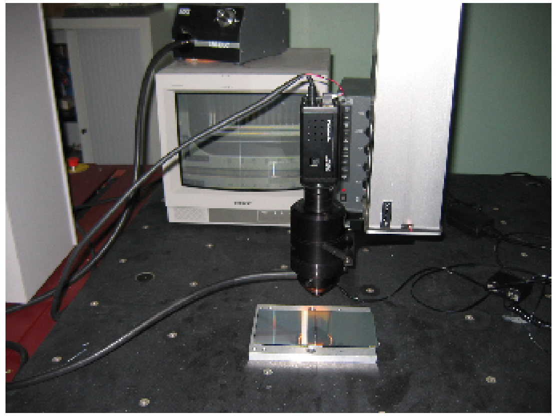
XUV



Elementary modules (revisiting existing techniques)

Longer strips but larger wafers.
So: easy to assemble





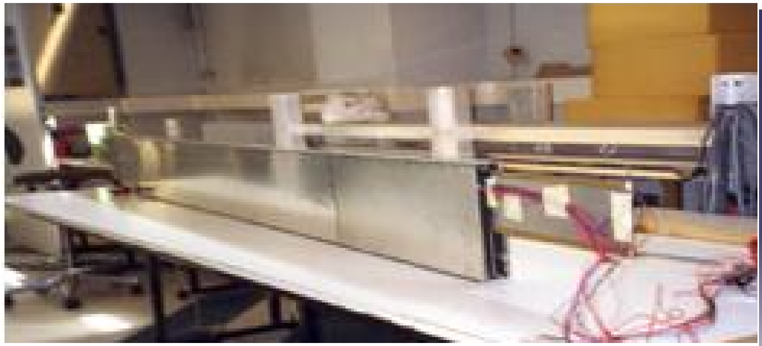
Occupancy studies tend to confirm that strips of 30 up to 60 cm length are adequate for most of the detector components

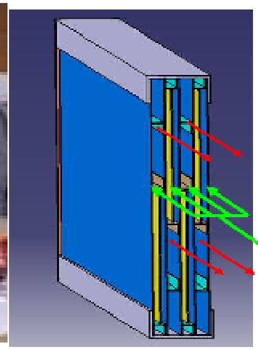
Key issues:

- ***Minimum material Budget***
- ***Best strips alignment***
- ***Most accurate positioning of the module on the support structure (large size!)***
- ***FE electronics connectics, packaging and cabling***
- ***Cooling***
- ***Easy to build***
- ***Transfer to Industry(large nb)***

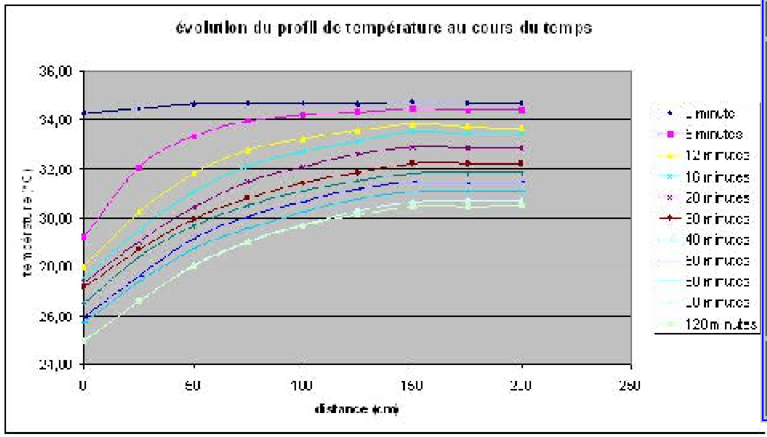
Be innovative!

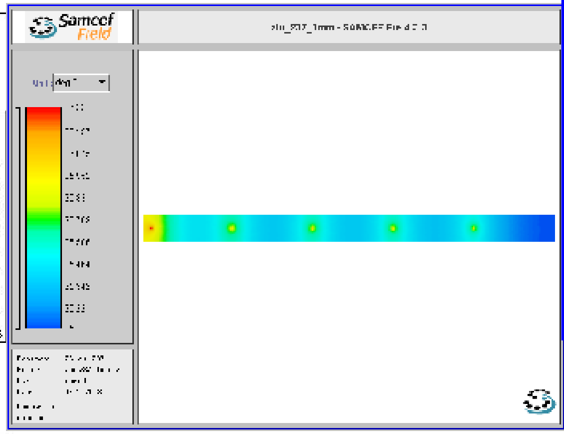
Thermo mechanical studies

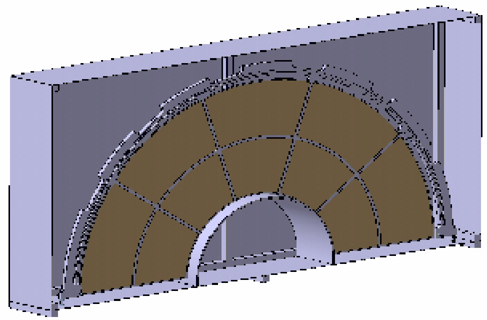




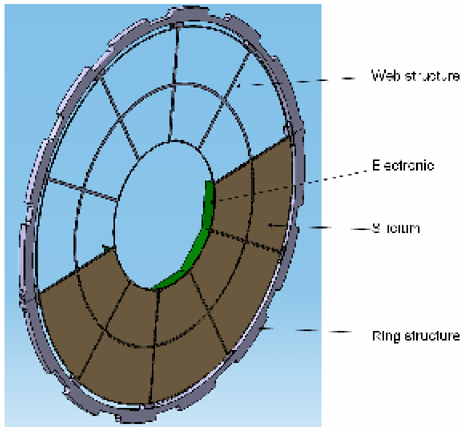
Extensive studies
on realistic external
central & forward
prototypes gives: air
conduction + convexion
Is sufficient;
What really matters
Is the environtmental
temperature







preliminary design of the mechanical
prototype to test the cooling system
for a disk of the inner forward



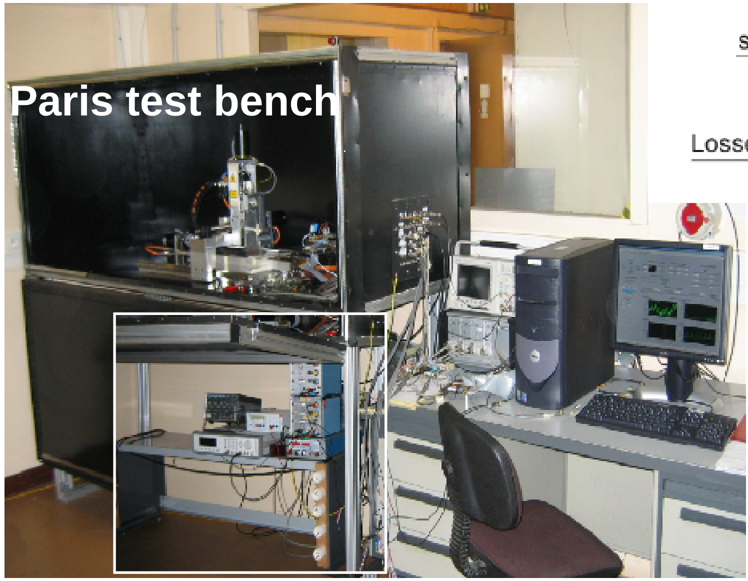
Now starting,
cooling studies
of the inner parts:
a bit more tricky…

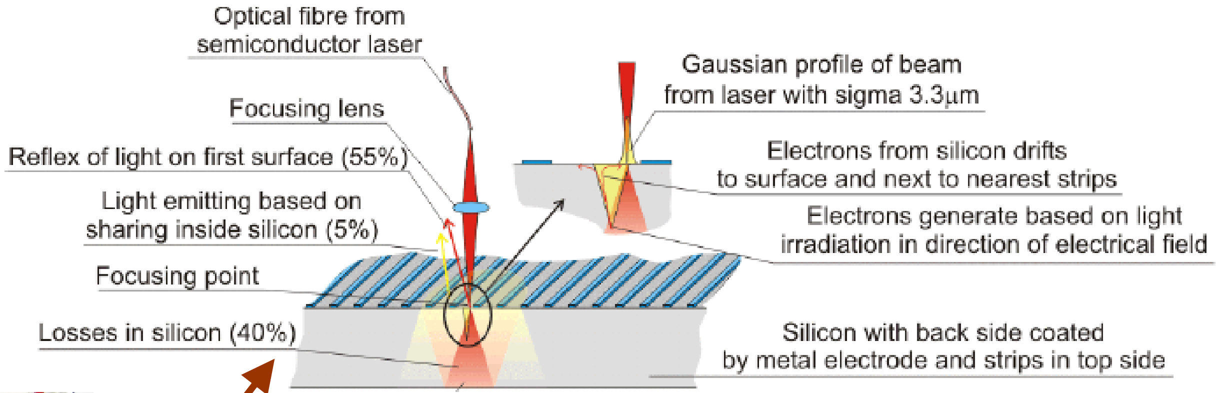
The tools:

- Lab test benches
- Test beams
- Simulations
- Alignment

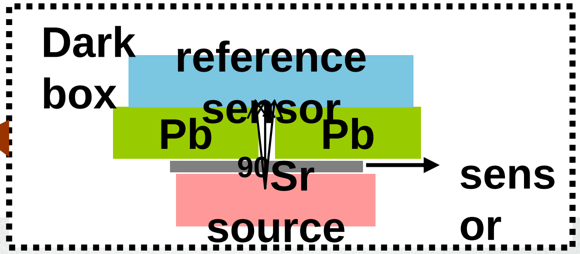
  (Michigan U. , IFCA-Santander)

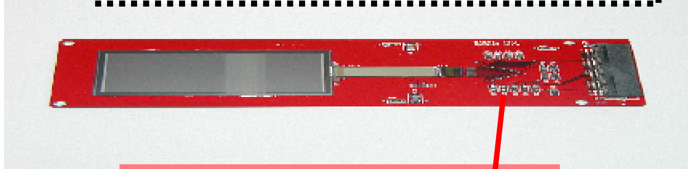
Lab test benches

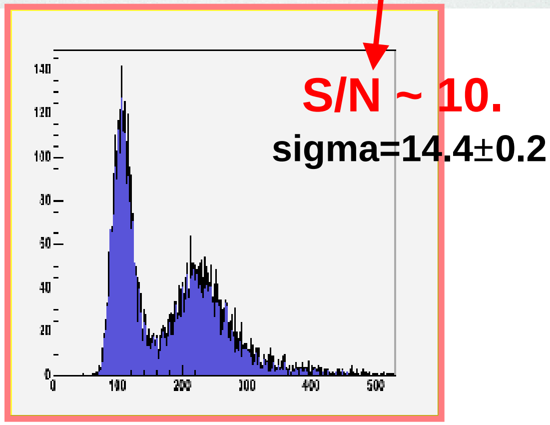


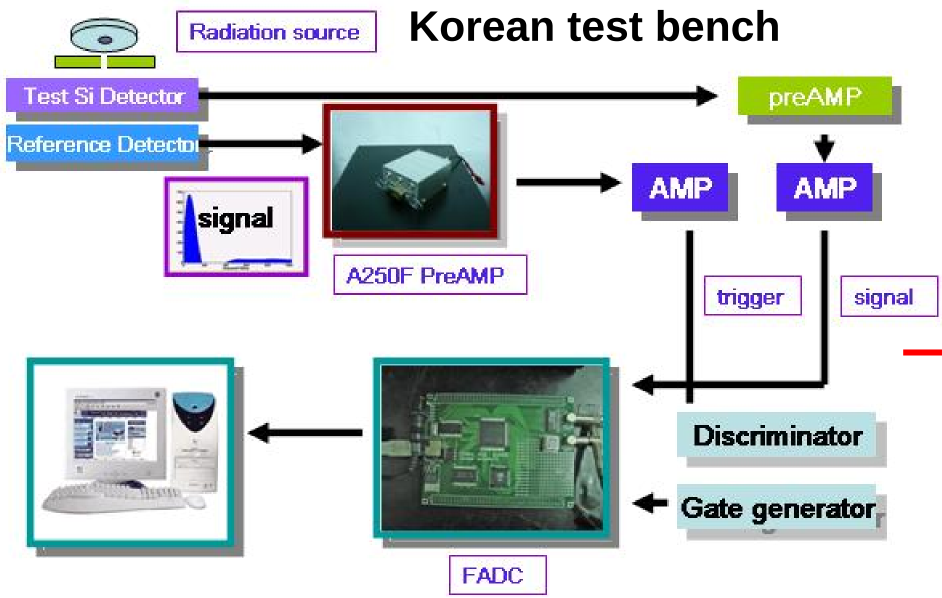


In most Labs:
LD & radioactiveSource (ex: Paris & Korea)





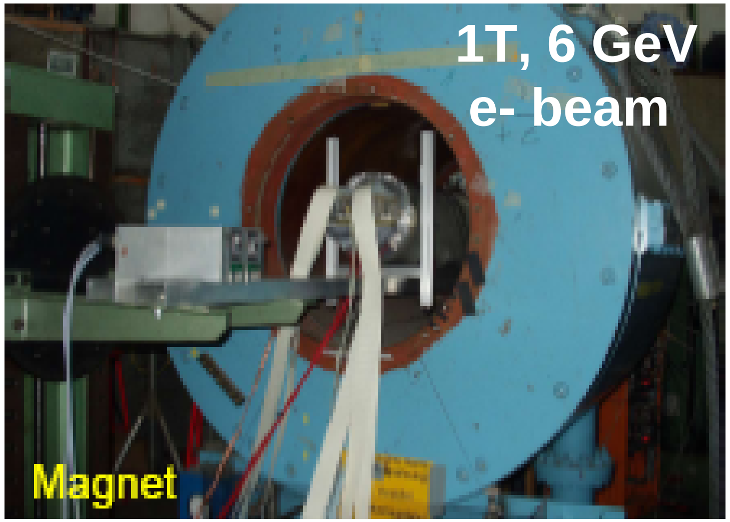




Test beams: Goals

- To qualify in conditions **closest to the real life**: prototypes of detectors (including New Si technologies) and of the associated FE and readout electronics.
- Detection efficiency vs operational parameters
- Spatial resolution, cluster size
- Signal/Bruit
- Effect of magnetic field (Lorenz angle determination)
- Angular scans, bias scans
- Integration with other sub-detectors
- Alignment
- Cooling (including power cycling)
- In the specific & new ILC conditions.

Foreseen beams



Others:

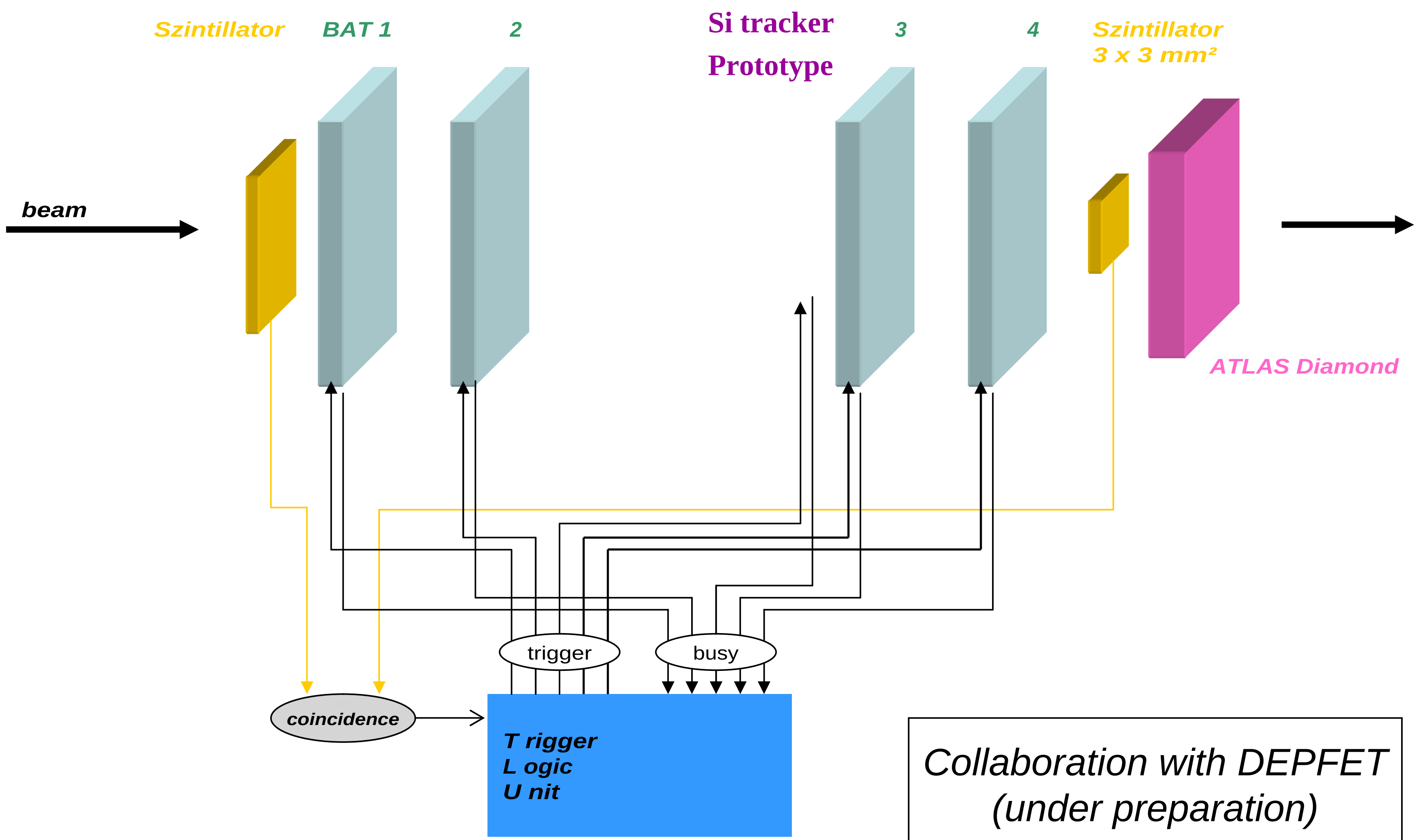
CERN, FNAL, KEK (Korean colleagues)

Bonn electron 3.5 GeV

Elektronen-Stretcher-Anlage (ELSA)

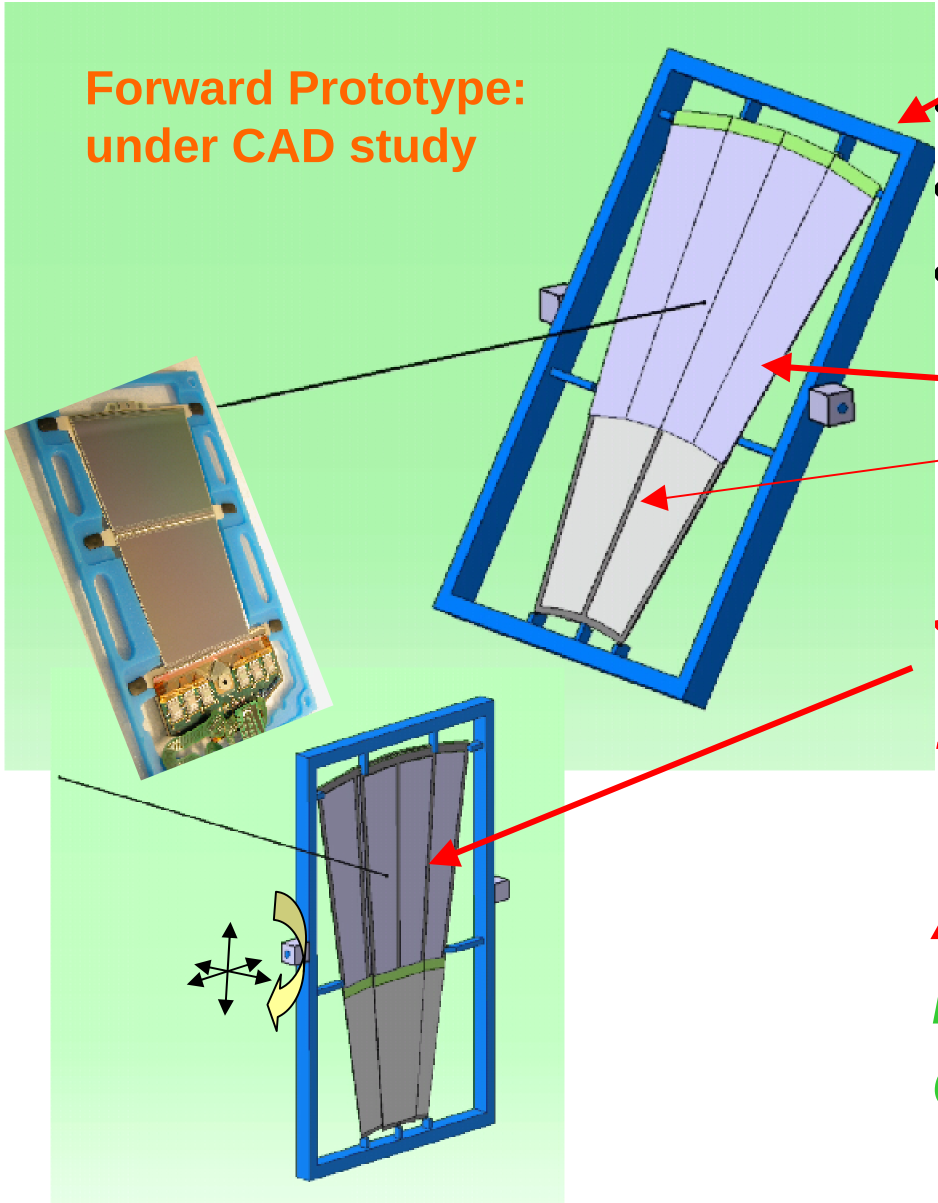
Participants: All + FNAL

Using the test beam setup in Bonn



Collaboration with DEPFET
(under preparation)

Detector Prototypes:



Support mobile

- Design (just started)
- Fabrication
- Assembling & Mounting

Module with 3 sensors

Module with 2 sensors

Second layer partly covering the first one.

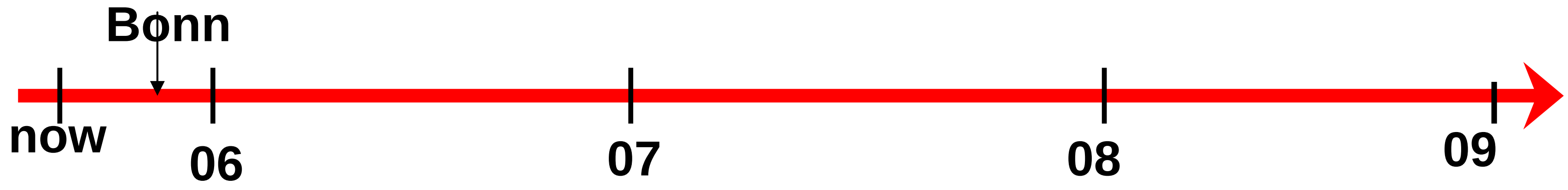
Total of 60 trapezoidal sensors,

About 10 K readout channels

Ready by end 2006/beg. 2007

Other prototypes: Ladders of different sizes and sensors

Calendrier et financement



Préparations tests Proto1

Tests échelles construction proto Forward
Chips 128 voies

Construction proto barrel
Tests (suite) aussi combinés avec autres sous-détecteurs
Autre fonderie (>=512 voies + techno)

EUDET prévoit pour Si-tracking dans JRA2, support financier pour

- *Partie des chips (deux fonderies) et un large nombre de voies*
- *Protos large dimension partie de détecteur Si central et bouchons*
- *Protos alignement*
- *Protos refroidissement*

Charge au niveau physiciens dans tests faisceau/analyse: semble OK dans SiLC.

Simulations

The SILC collaboration (V. Saveliev) is installing the Si components of the various detector concepts in the simulation packages, GEANT 3 and 4 based.

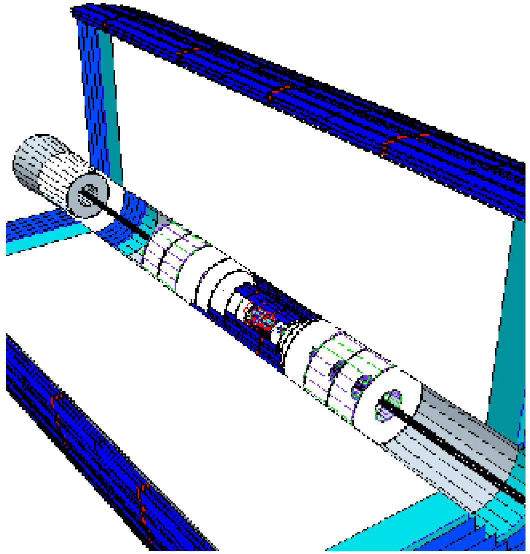
The main issues are:

- To have the reconstruction package in GEANT 4 framework
- To get a common/compatible simulation package (presently: MOKKA, JUPITER, SLIC ..)

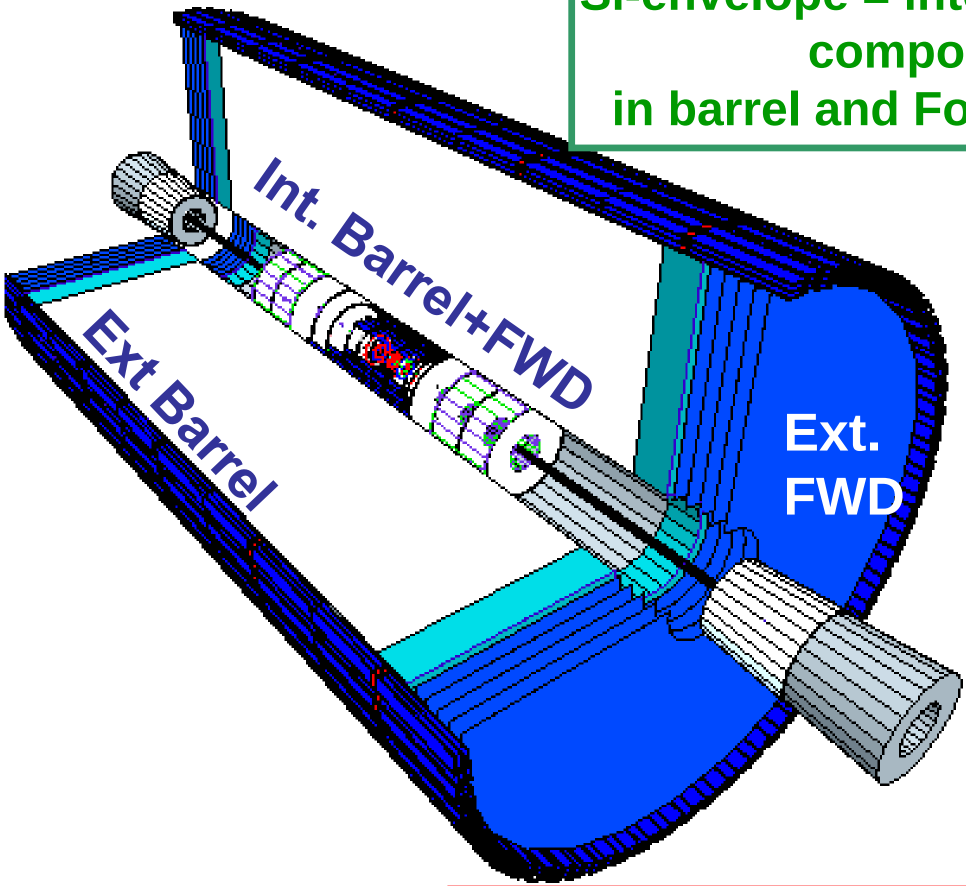
Anyway: SILC has started to work on the comparison of performances between the various tracking concepts and aims to have results by Snowmass.

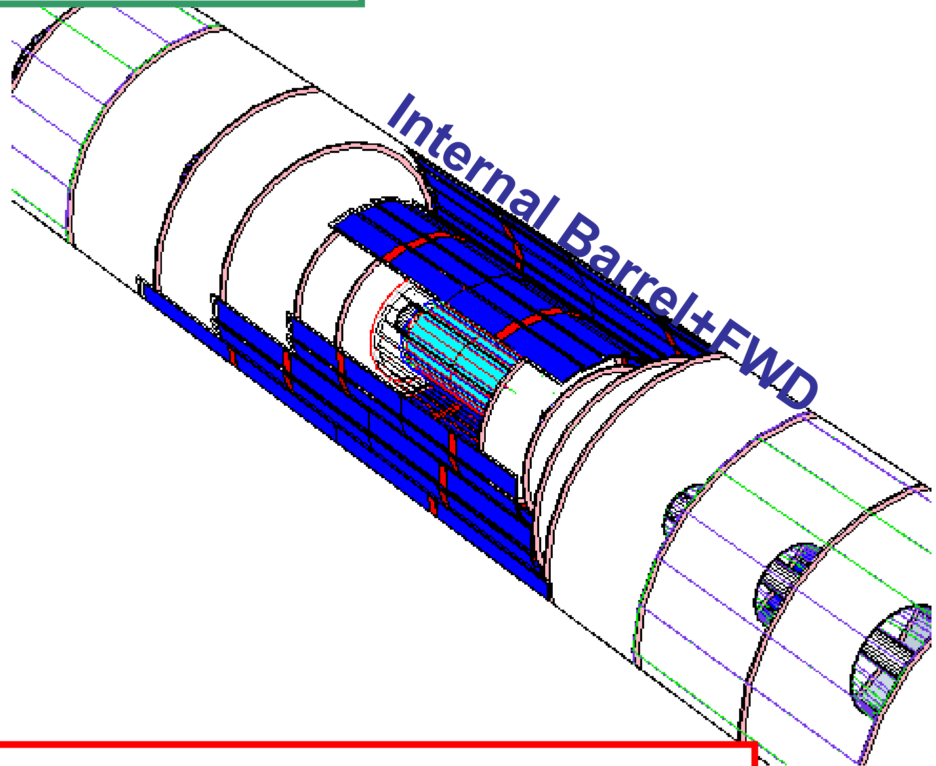
Geometry DB for Si tracking systems in G4 *(V. Saveliev, DESY-Obninsk)*

Ex: the Si Envelope



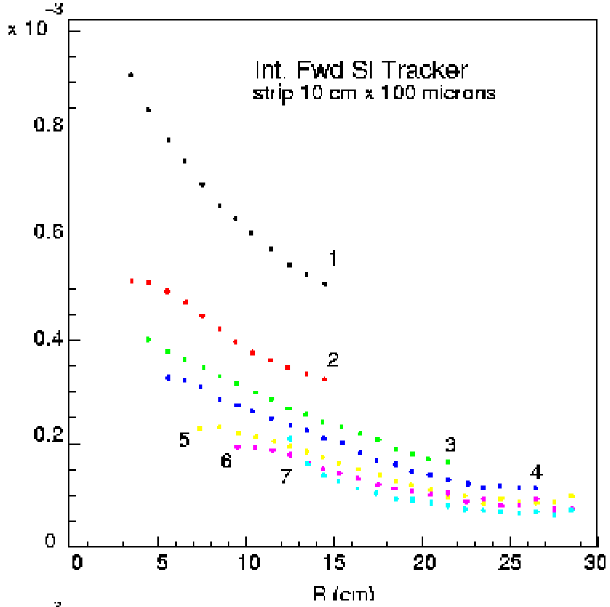
Si-envelope = internal & external components
in barrel and Forward regions

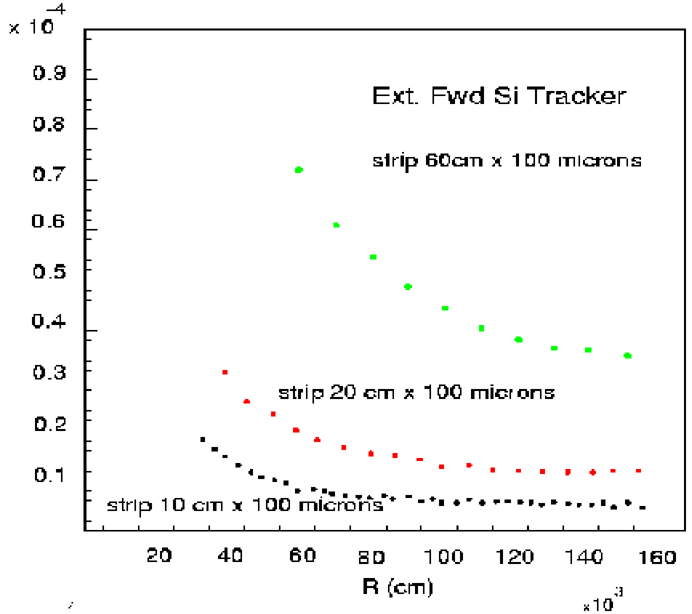




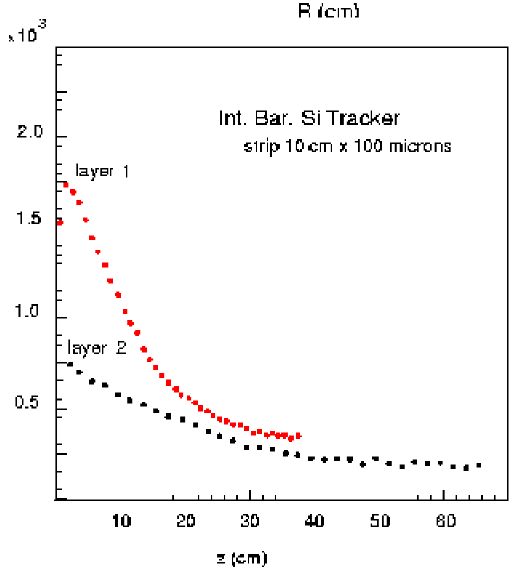
The DB definiton has been sent to the official DB:

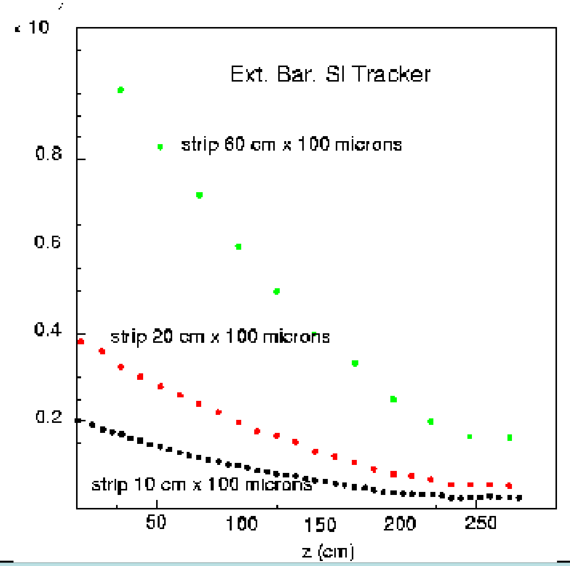
DETECTOR OCCUPANCIES

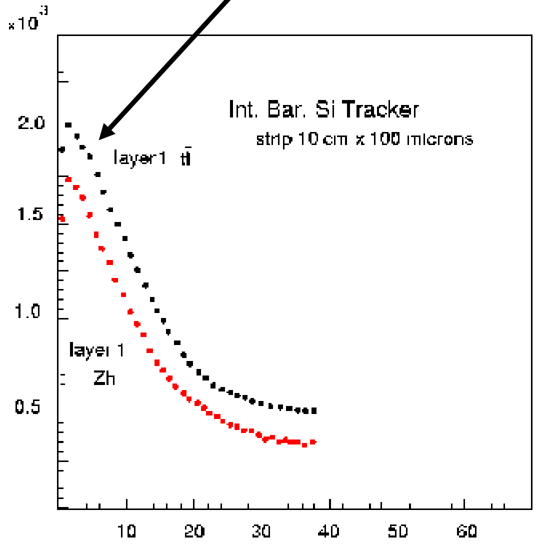




ttbar/ HZ gives ~20% higher occupancy



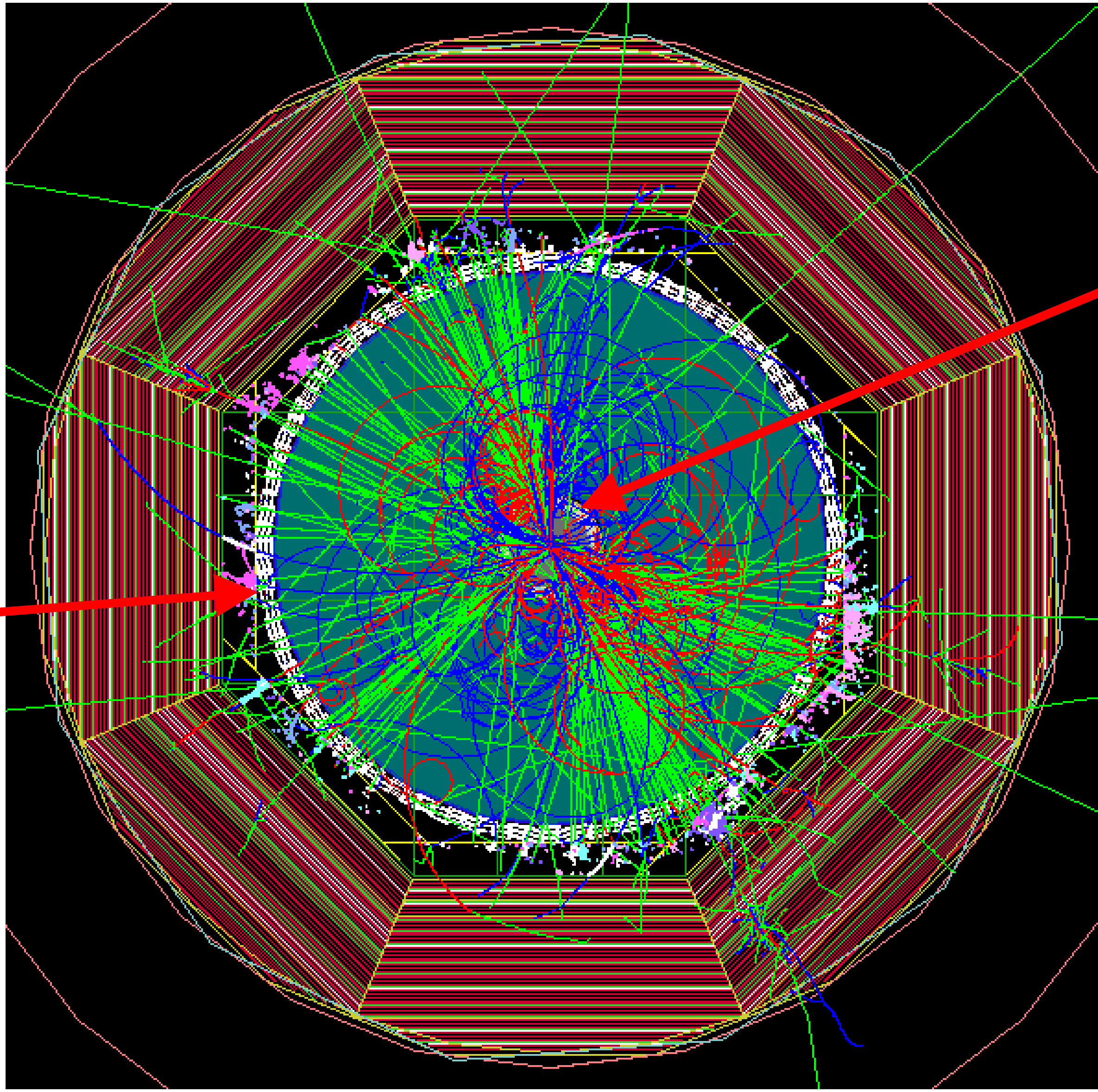




Occupancies are calculated with BRAHMS full simulation (Si-Envelope+TPC), Higgstrahlung HZ with bbbar and q qbar at Ecm=500 GeV
Values at most of order 1% to 2% for the hotest places in the detector!

Strips of length from 30cm to 60cm are appropriate.

LDC

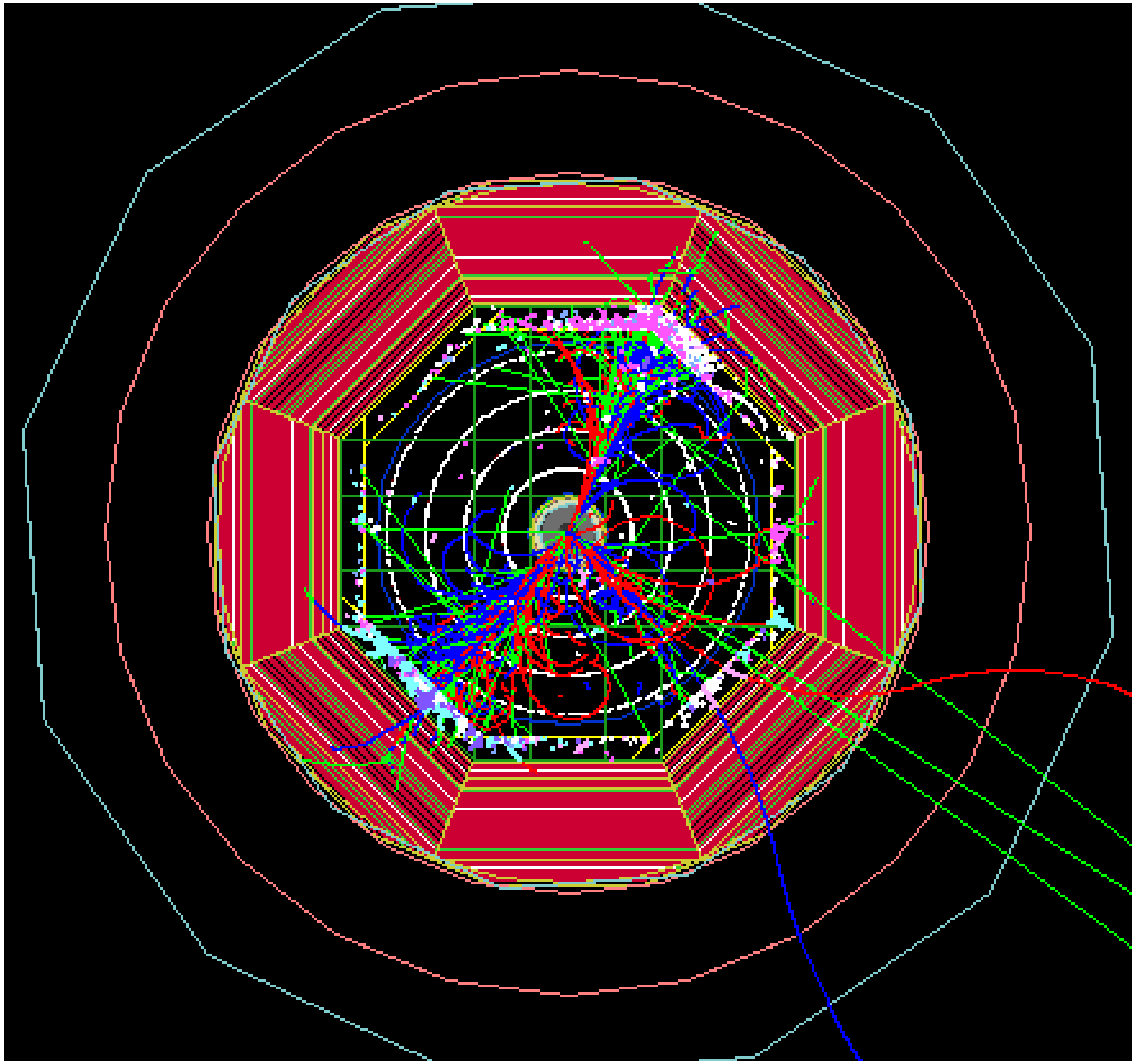


Silicon
Internal
barrel
component

Silicon
external
barrel
component

e+e- → H° → ttbar → 4q-jets + 2 b-jets, Ecm=750 GeV
Pythia +ISR+FSR+beamstrahlung+ full simulation (MOKKA:
μvertex+SIT+TPC+SET +FTD+Si-FCH +em calo+hadron calo)

SiD



Geant4 simulation of Higgs event in SiD detector, using MOKKA framework including geometry DB for SiD concept

SiLC R&D proposal was presented to the PRC on May 2003

Goal: to develop the next generation of large area Si trackers suited for performing very high precision measurements in spatial position and momentum at the ILC,

All R&D aspects, on sensors, electronics and mechanics are addressed.
All needed tools: simulations, Lab test benches, test beams, alignement and calibration are developed

Highlights/important progress these last 2 years:

- **Work on sensors: characterization of long strips, development of fab lines**
- **FE electronics in deep submicron CMOS techno**
- **Developing Lab test bench for the precise requested measurments**
- **CAD of all tracking components both for LDC (Si Envelope) & SiD**
- **Thermo mechanical studies**

NOW:

Preparing for test beams and getting even closer to the real life conditions.
Collaboration getting speed and established close contacts with all 3 detector concepts
Keeping synergy with LHC (SuperLHC).

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