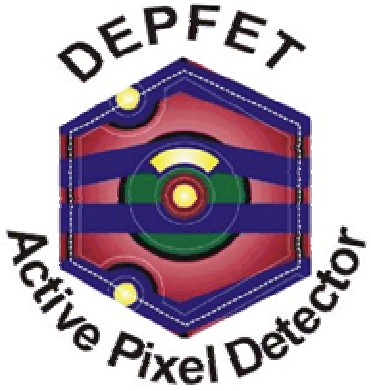
Status of DEPFET pixel detectors for ILC



Peter Fischer for the DEPFET collaboration

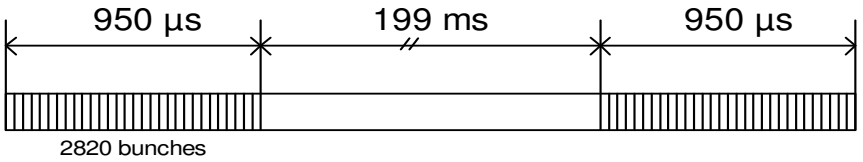
Bonn University:	R. Kohrs, M. Karagounis, H. Krüger, L. Reuen, C. Sandow, M. Trimpl, N. Wermes
MPI Munich, HLL, ILC:	L. Andricek, G. Lutz, H. G. Moser, R. H. Richter, M. Schnecke
Mannheim University:	P. Fischer, F. Giesen, I. Peric
MPI Munich, HLL, XEUS:	K. Heinzinger, P. Lechner, L. Strüder, J. Treis

Talk Outline

- Summary of ILC requirements
- Possible geometry of ILC DEPFET layer
- The DEPFET working principle
- Sensor design & technology
- Thinning technology
- ILC prototype system
- Measurements on ILC structures:
  - -Irradiations
  - -Noise, clear efficiency
  - -Matrix: Lab results
  - -Matrix: Test beam results
- Power consumption of ILC system
- Summary and outlook

Requirements for ILC innermost Tracker Layer

- Time structure: one train of **2820 crossings** in **~1 ms** every **~200ms**

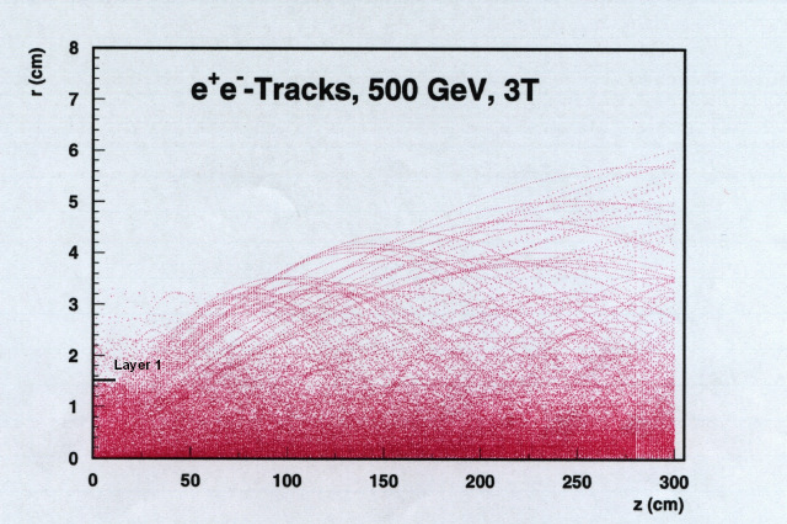


- Hit density: For a 10 cm long cylinder at **r=15 mm** (A=10500 mm²):
  ~ 370 tracks / crossing
  ~ 0.035 tracks / mm² / crossing
  ~ **100 tracks / mm² / train**

  much less if r > 15 mm (~ 1/7 for r=27 mm)

- Row readout rate: some 10 MHz

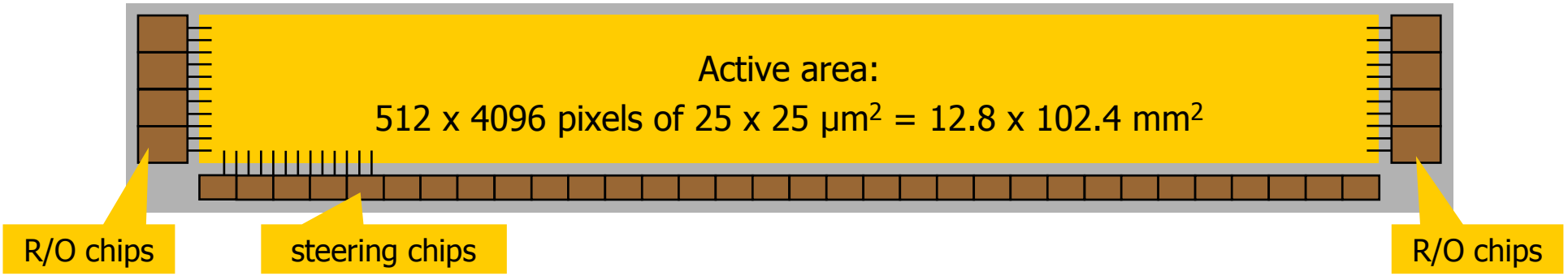
- Resolution: **few µm** (⇒ pixel size ≤ 25 x 25 µm²)
- Radiation tolerance ≥ **200 krad** (for 5 years operation)
- Radiation length very small: **~0.1% X_0** per layer



(simulation from C. Büsser, DESY)

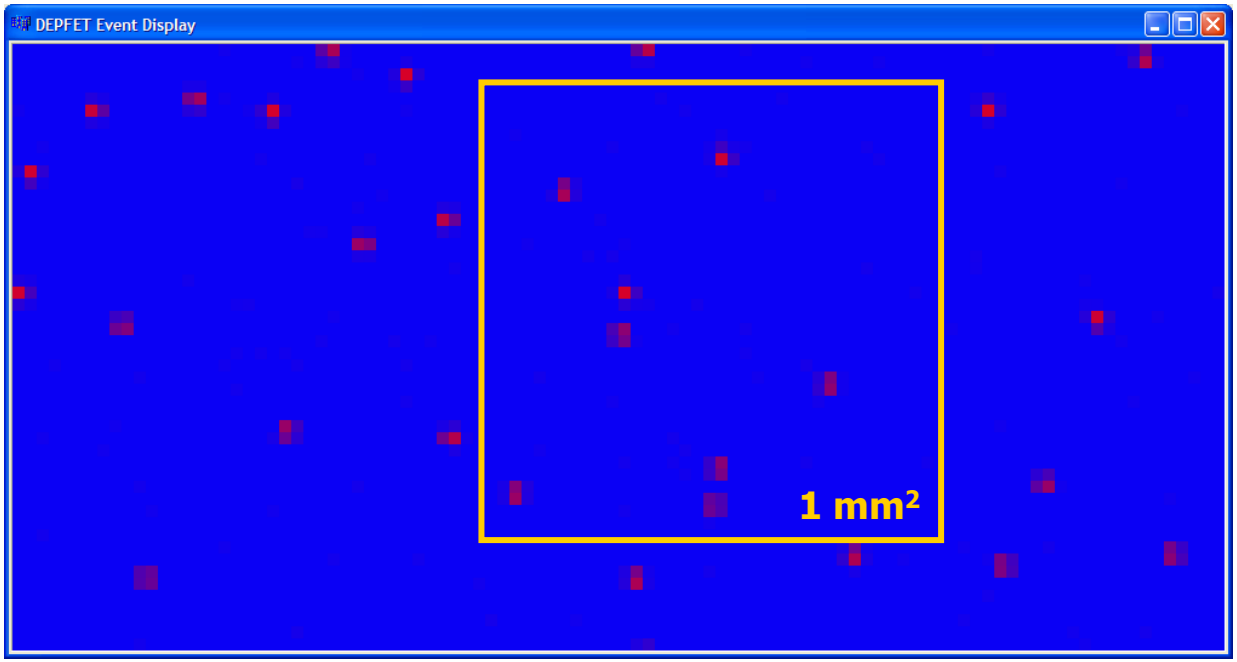
ILC DEPFET Module (Layer 1)

- Modules have active area ~**13 x 100 mm²**
- They are read out on **both sides**.

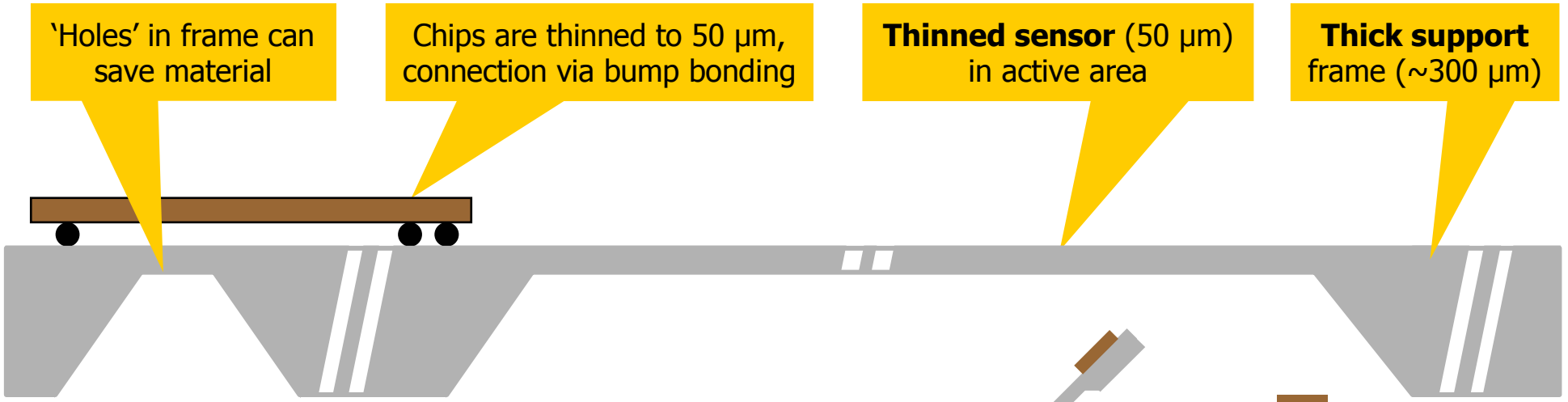


- Occupancy simulation:
  - Assume signal width of 10µm
  - Read **10 frames** per train
    i.e. 10 x 2048 rows in 1ms
    or one row in 50ns (**20MHz**)
  - Expect ~10 tracks / mm² / event

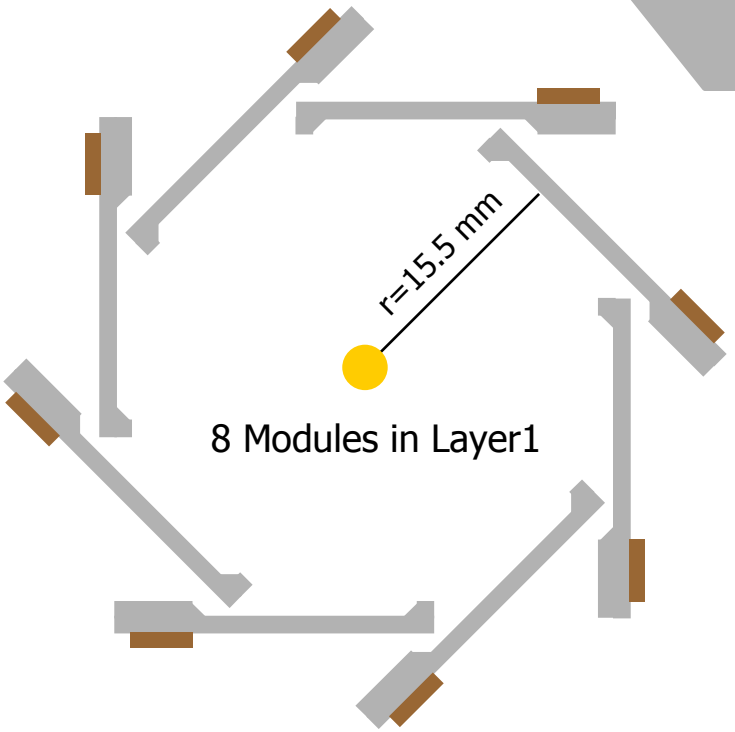
- Pattern recognition should not be a problem!



Possible Geometry of Layer 1



Cross section of a module



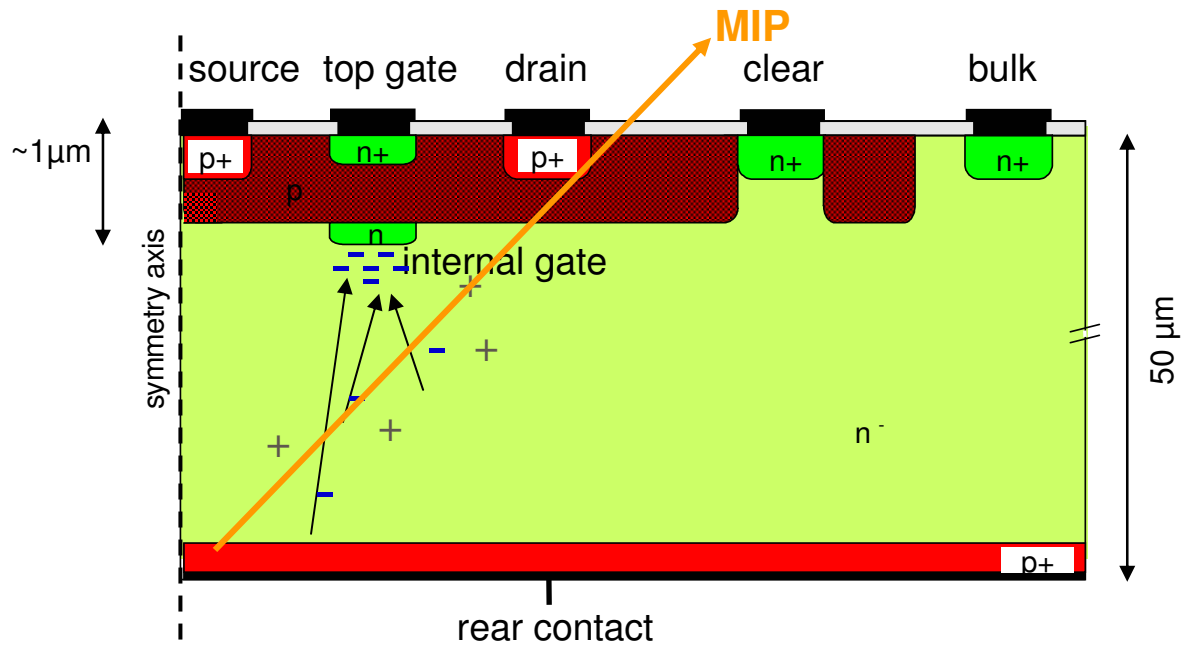
8 Modules in Layer1

Estimation of material budget:

- pixel area: 13x100 mm^2, 50µm: 0.05% X_0
- steering chips: 2x100 mm^2, 50µm: 0.01% X_0
- frame w. holes: 4x100 mm^2, 50% of 300µm: 0.05% X_0
- total: **0.11% X_0**

DEPFET Principle of Operation

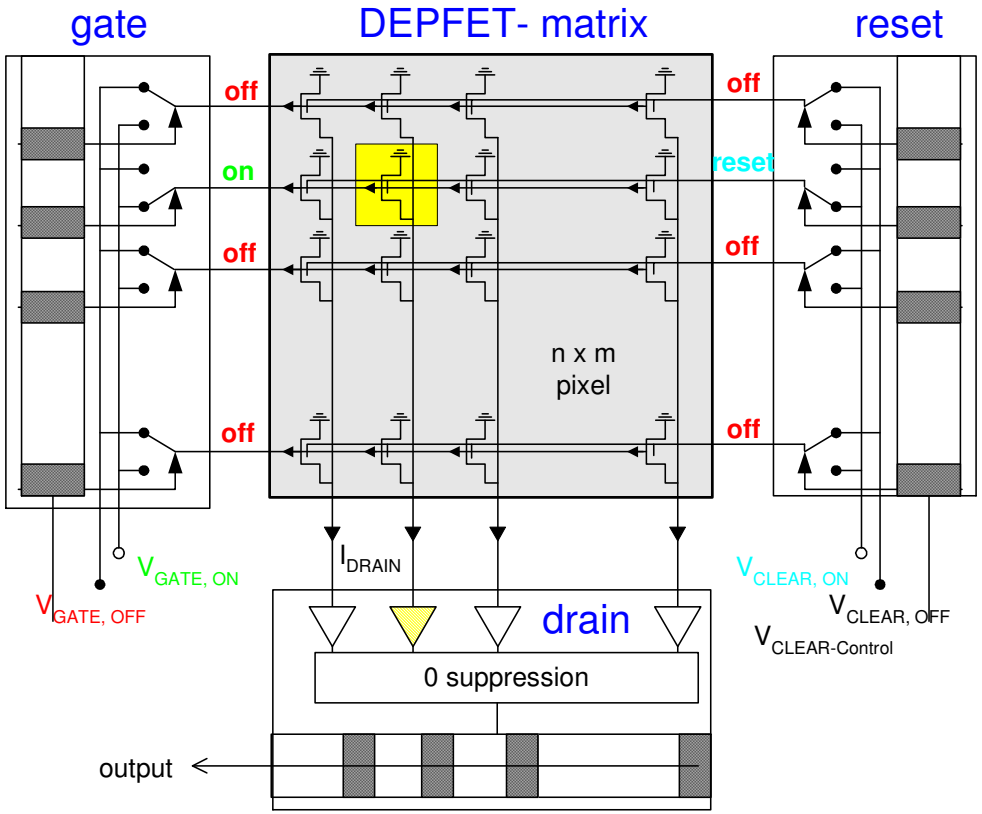
- A **p-FET** transistor is integrated in every pixel
- A **potential minimum for electrons** is created under the channel by **sideward depletion**
- Electrons are collected in the „internal gate" and **modulate the transistor current**
- Signal charge is removed via a clear contact

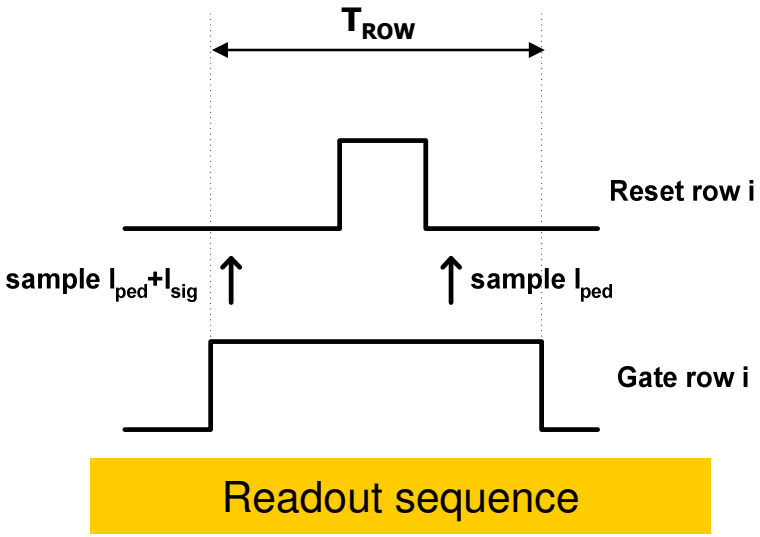


- **Fast** signal collection in **fully depleted** bulk
- **Low noise** due to small capacitance and first amplification
- Transistor can be **switched off** by external gate – charge collection is then still active !
- Readout can be at the source ('voltage signal') or at the drain ('current signal') – **ILC uses drain readout**

Matrix Operation

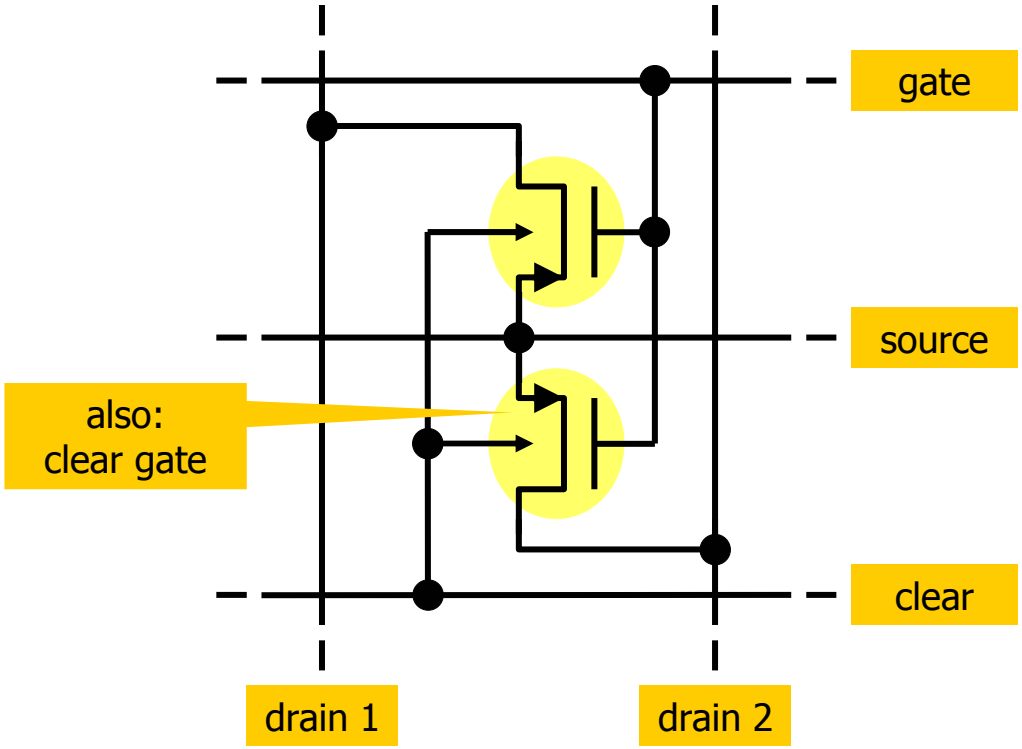
- Connect **gates and clears horizontally** to select / clear single rows. Apply voltages with SWITCHER chips.
- Connect **drains (or sources) vertically** and amplify current (or voltage): CURO chip
- Charge is not shifted!
- Readout sequence: Enable row – read current (I_{sig} + I_{ped}) – clear – subtract current (I_{ped}) – move to next row

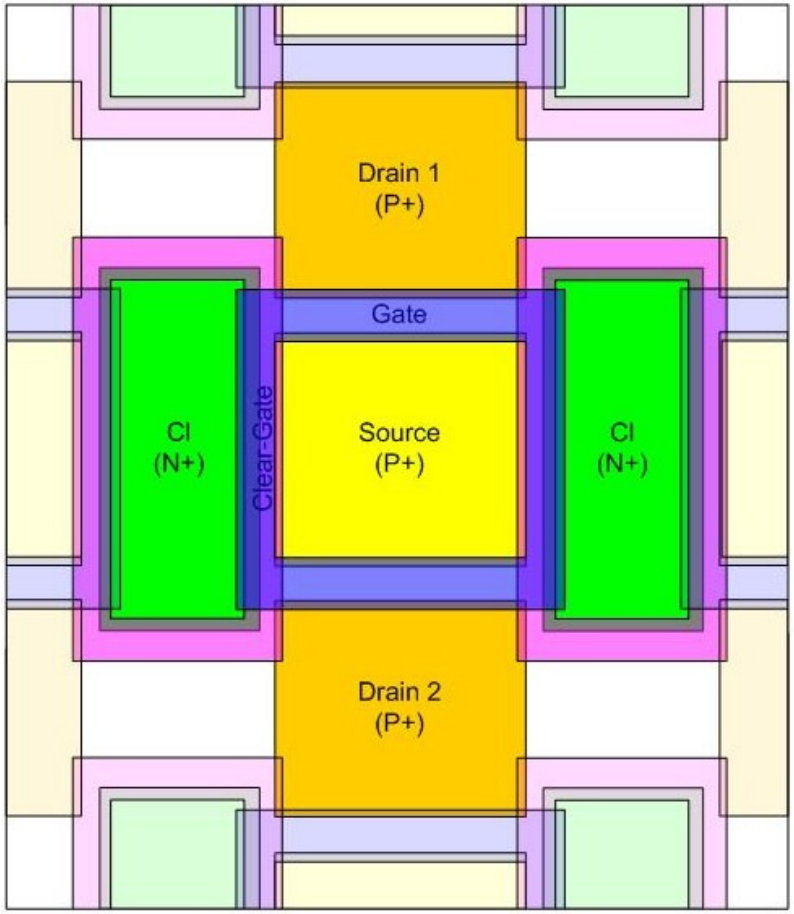




Sensor Design: MOS Devices

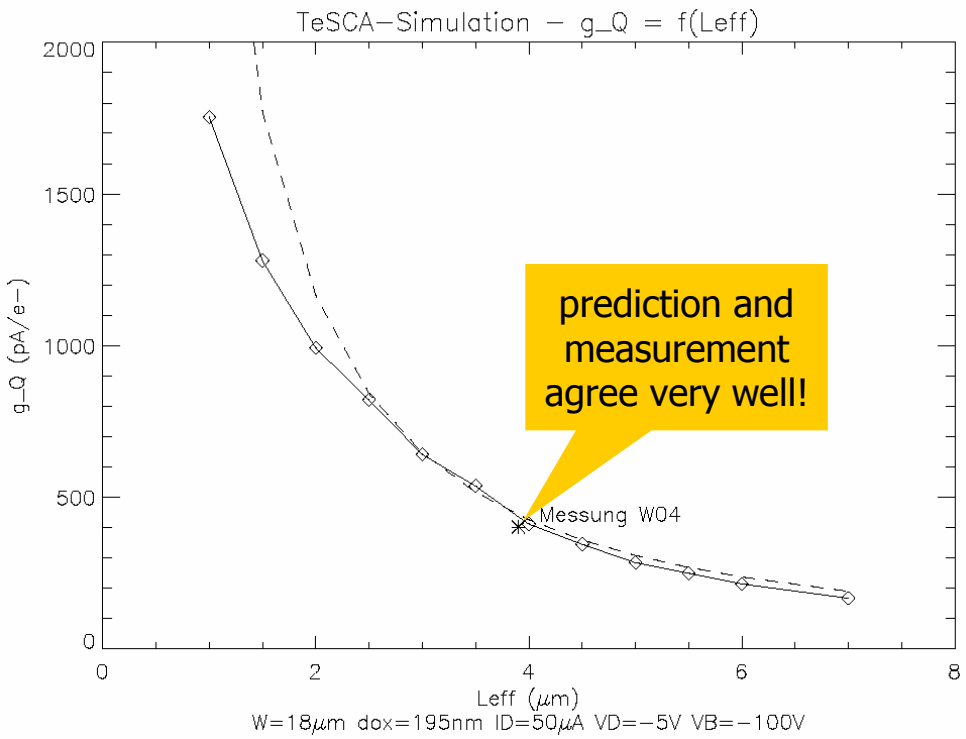
- Moved from JFETs to MOSFETs (top gate):
  - smaller device variations (required for large sensors)
  - smaller pixels (linear transistors possible)
  - radiation tolerance of gate oxide ?
- Increased amplification (now ~1nA / e^-)
- Fast and complete clear (using clear gate)
- Compact double pixel cell



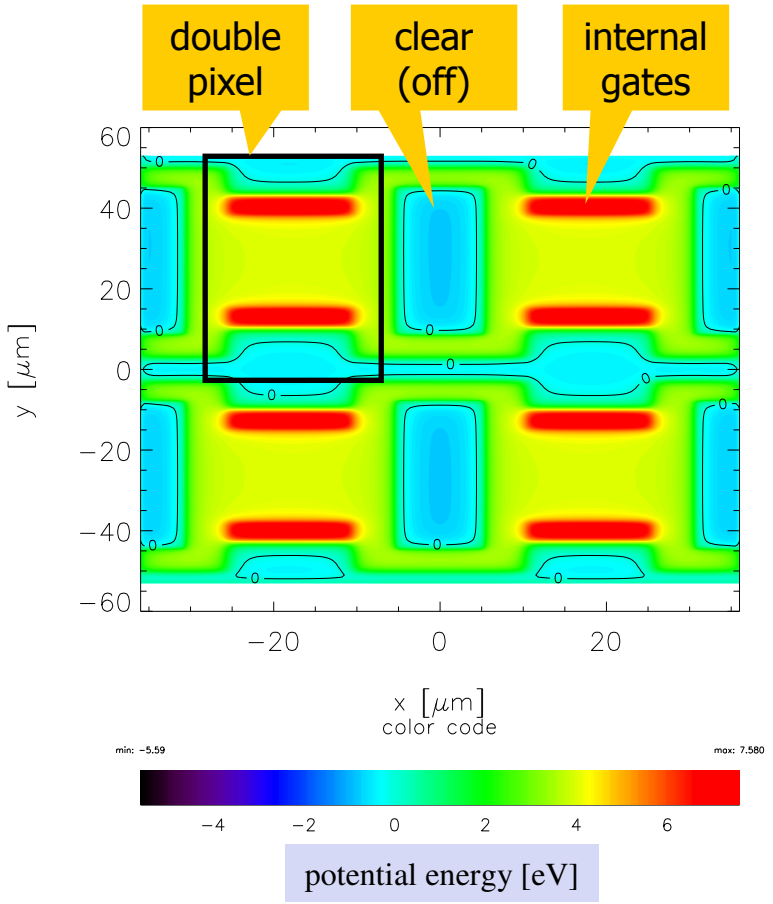


Sensor Simulations

- Use 3D-Simulator (Poseidon) for complicated structures
- Device behavior can be predicted accurately.
  Important for successful new designs!



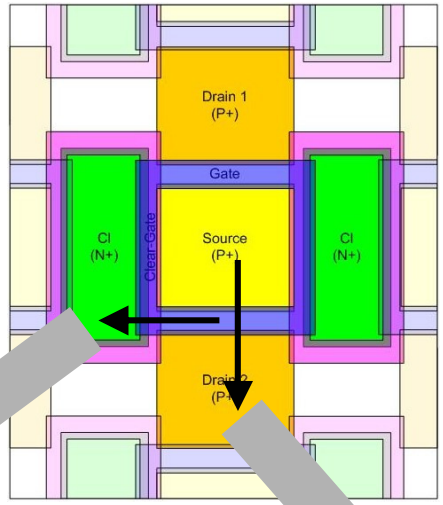
charge gain g_q for varying gate length

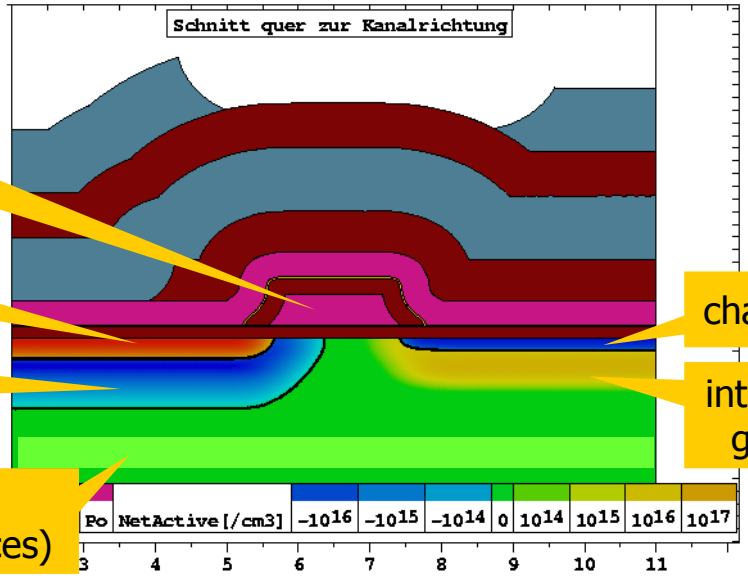


Potential distribution in 1µm depth in charge collection mode

Device Cross Sections

- Added **'clear gate'** to lower the clear barrier. Clocked and **static** operation possible
- Added a deep **high-E** n-implantation in some devices to lower clear voltages (clear channel is moved into bulk)





clear gate (Poly)

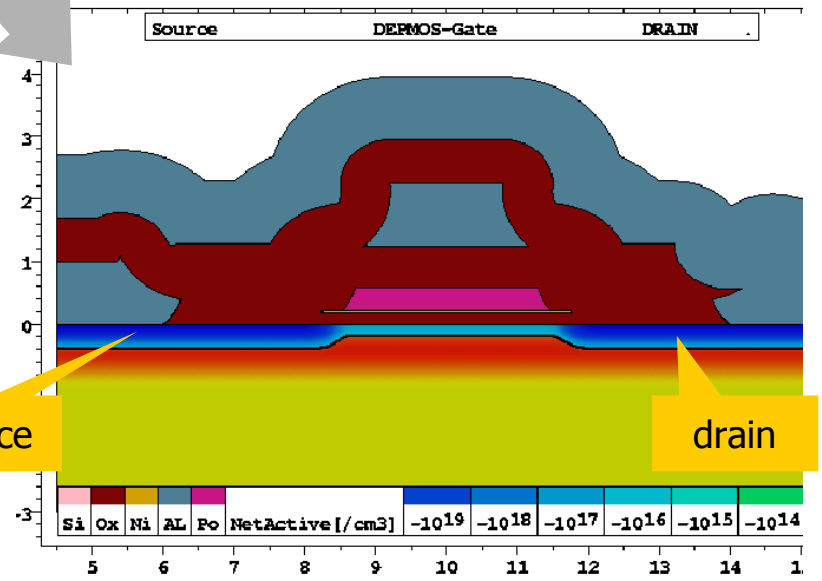
clear (n^+)

p-well

high-E (some devices)

channel

internal gate

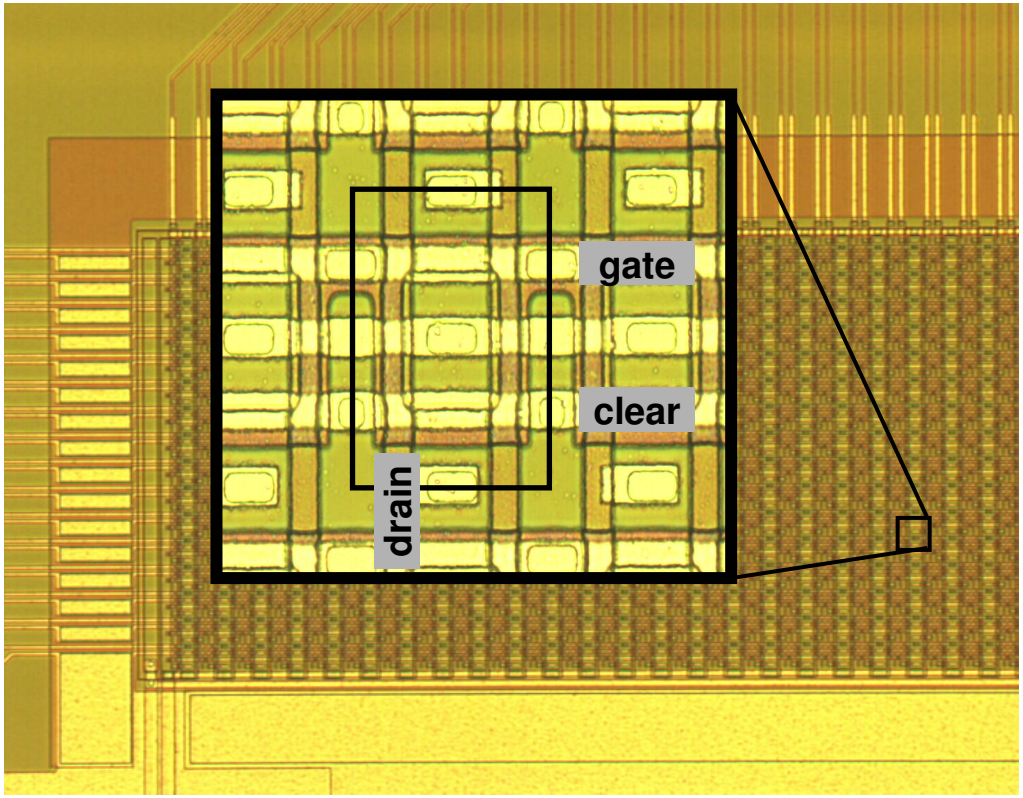


source

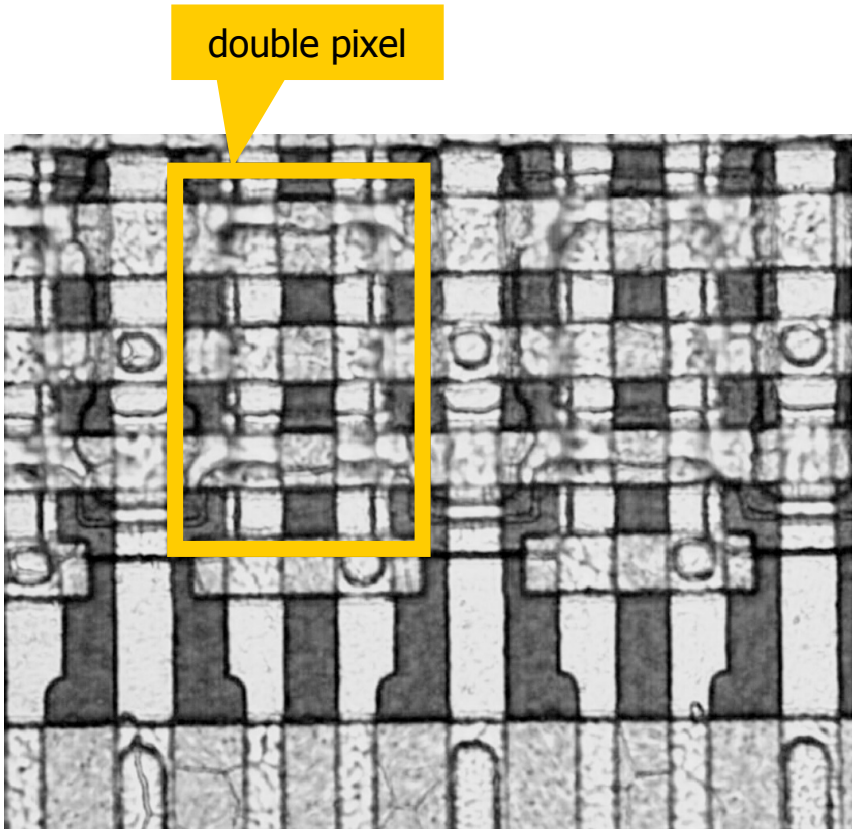
drain

Sensor Fabrication Technology

- A sensor-compatible technology with **2 poly and 2 metal layers** has been developed at HLL
- These are required for large matrix designs



16x128 test matrix, double pixel cell 33 x 47 μm^2

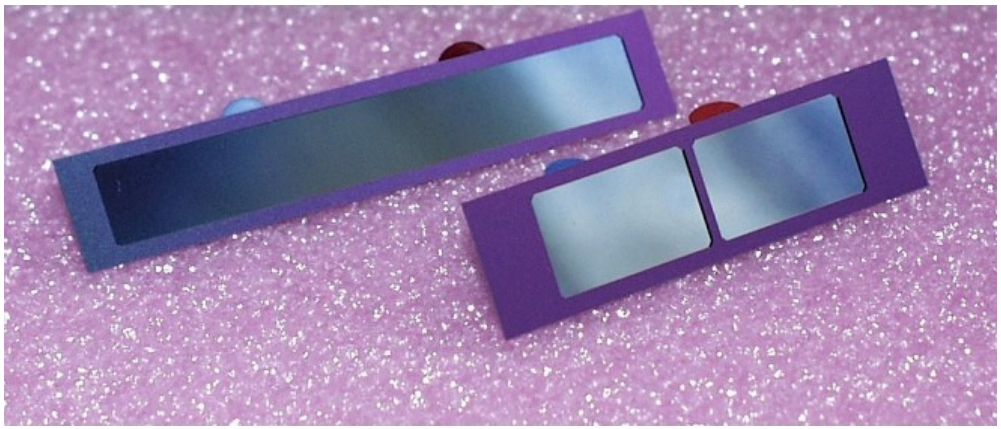


double metal matrix

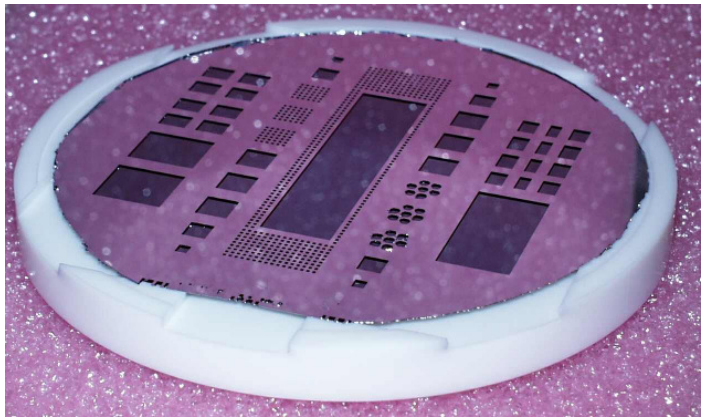
Making thin Sensors

- A novel technology to produce detectors with thin active area has been developed and prototyped (L. Andricek)

1. implant backside on sensor wafer
2. bond wafers with SiO_2 in between
3. thin sensor side to desired thick.
4. process DEPFETs on top side
5. etch backside up to oxide/implant

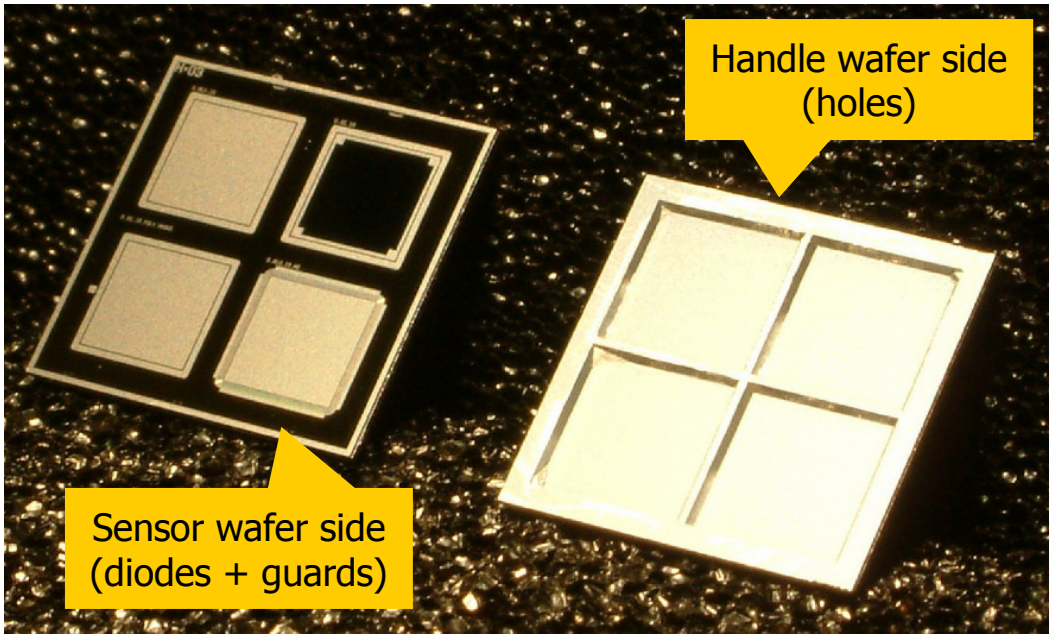


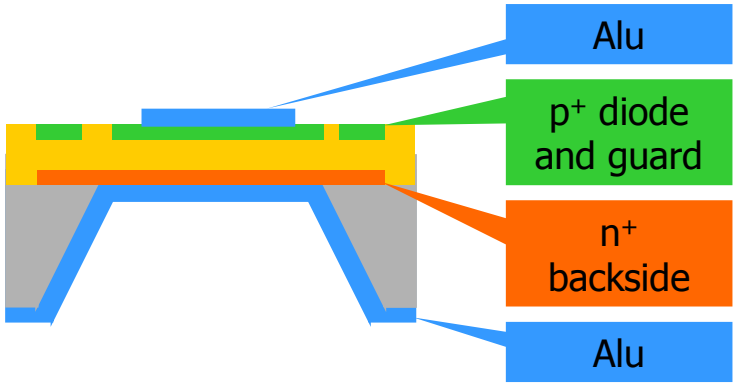
first 'dummy' samples:
50µm silicon with 350µm frame

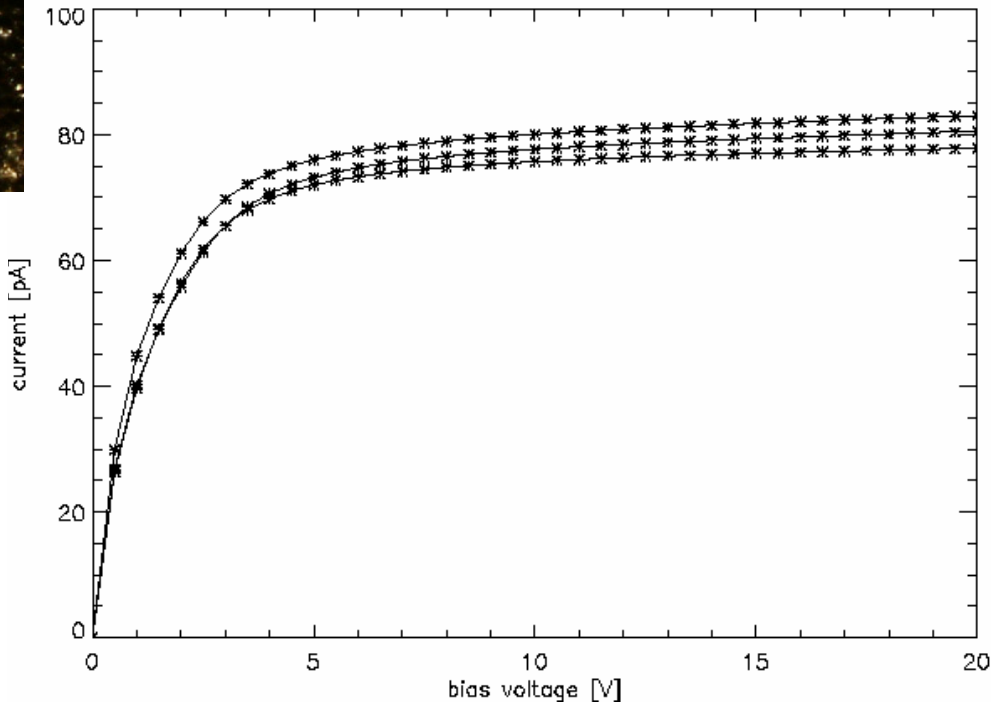


thinned diode structures:
leakage current: <1nA /cm²

Quality of Thin Diodes

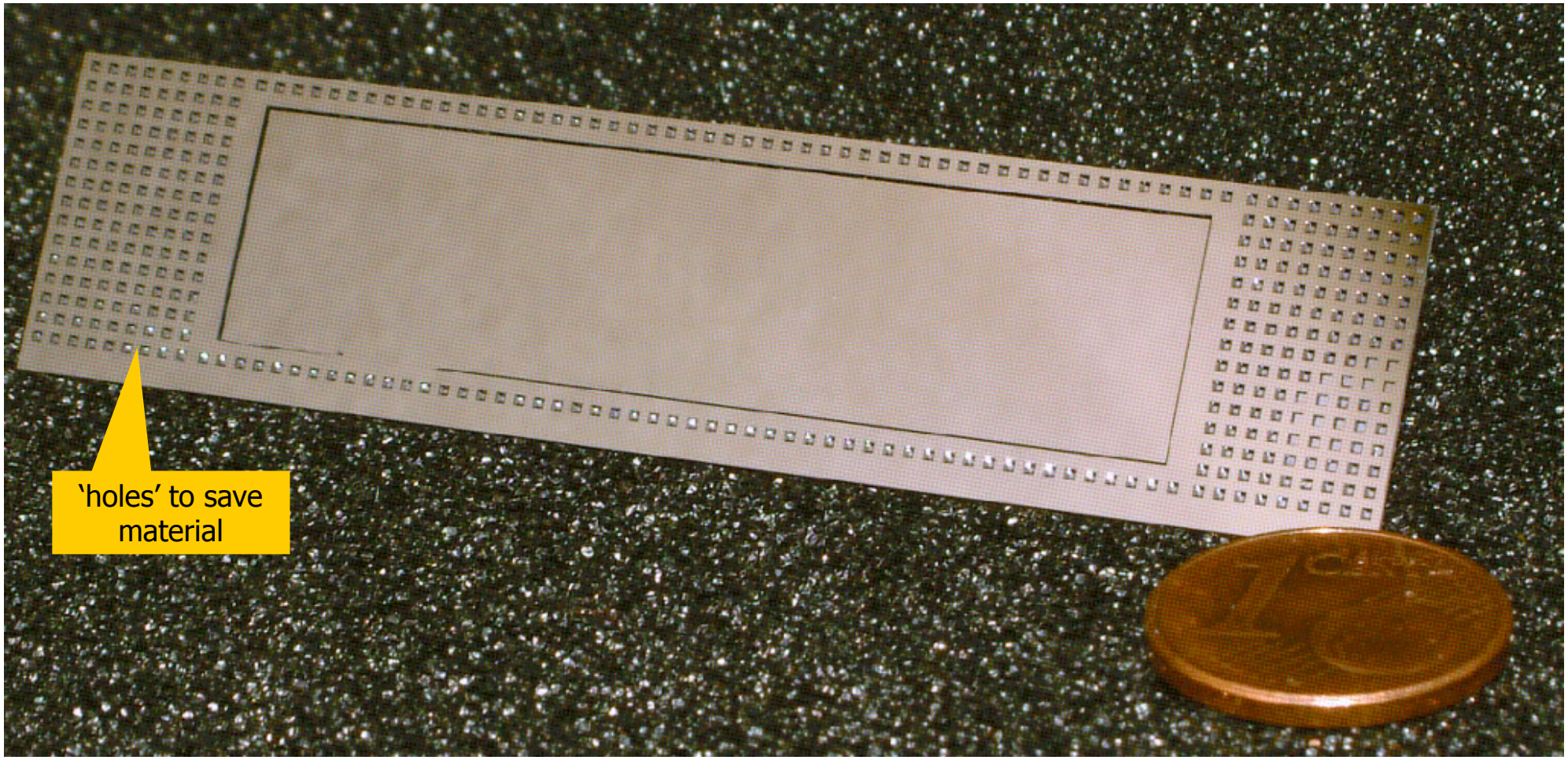




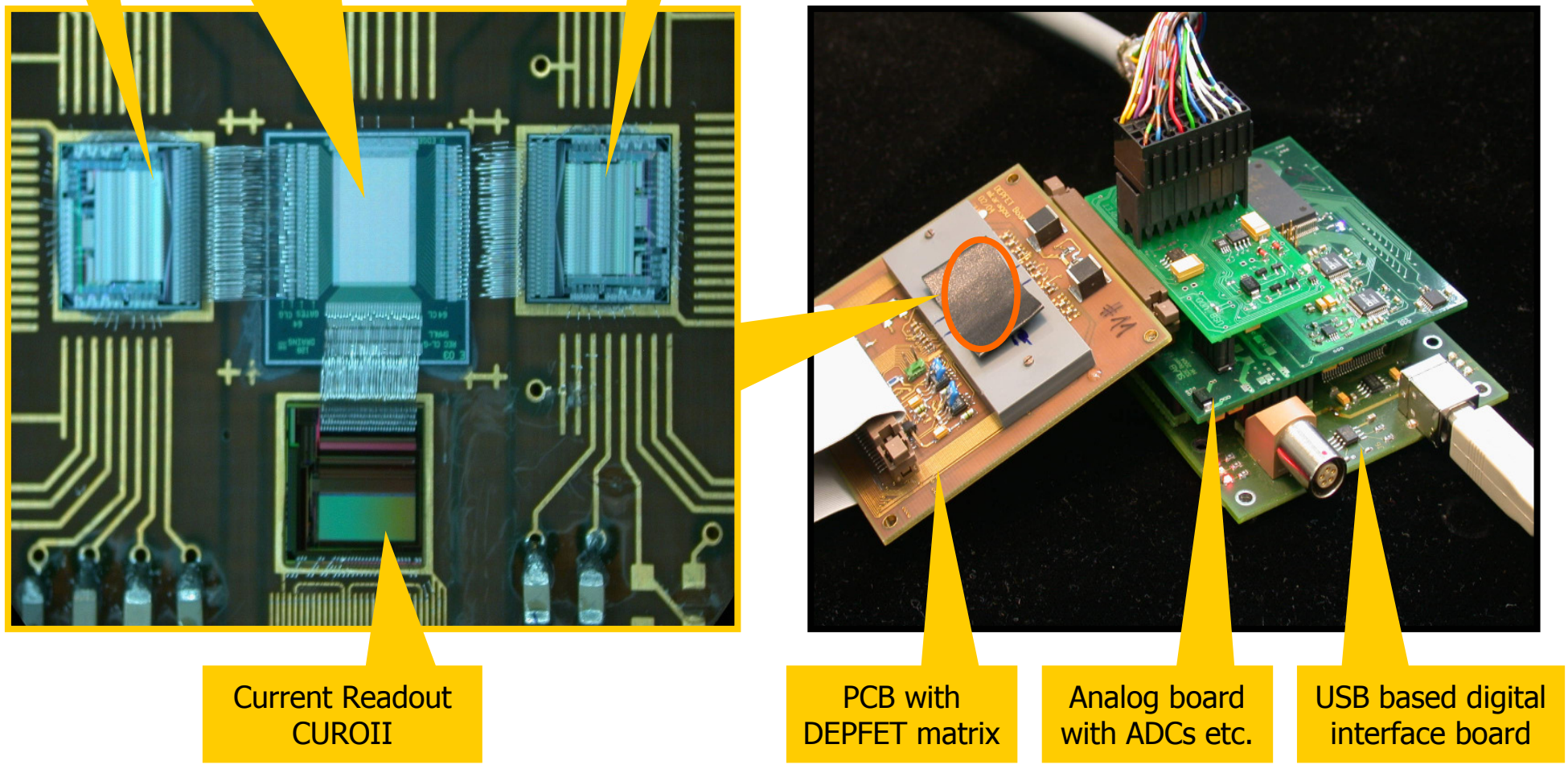


- 10mm² diodes on 50µm have been produced
  (in test lab, 'real' devices will be even better!)
- Measured leakage currents are very low: **150 nA/cm³**
  (~very good strip detector)
- No breakdown is observed even at strong over-depletion

Dummy Module with ~ ILC Geometry

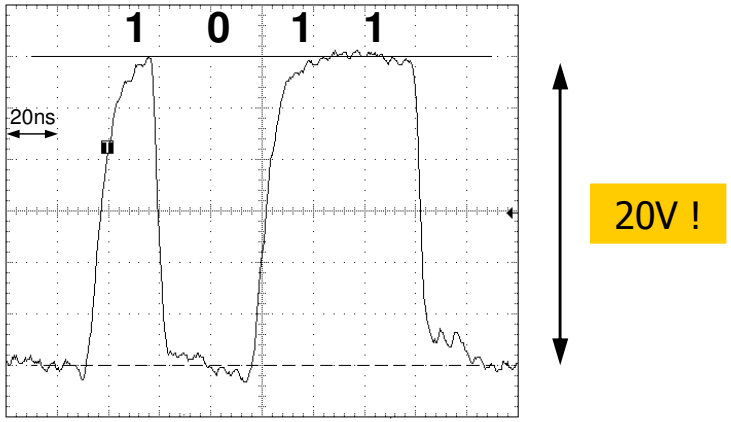


ILC Prototype System

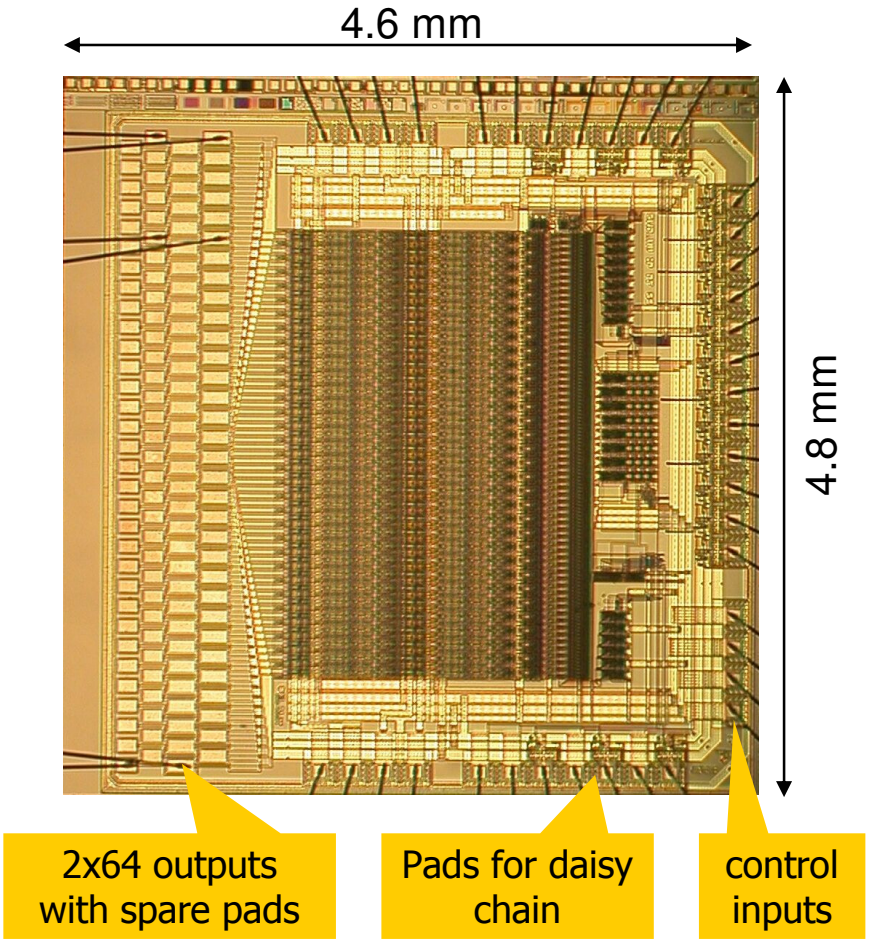


Switcher ASIC (Multiplexer)

- **64 channels** with **2 analog MUX** outputs ('A' and 'B')
- Can switch up to **25 V**
- **digital control ground + supply floating**
- **fast internal sequencer** for programmable pattern (operates up to 80MHz)
- **Daisy chaining** of several chips on a module possible
- Present dissipation: **1mW/channel @ 30MHz**
- 0.8µm AMS HV technology
- Radiation tolerance may be problematic!



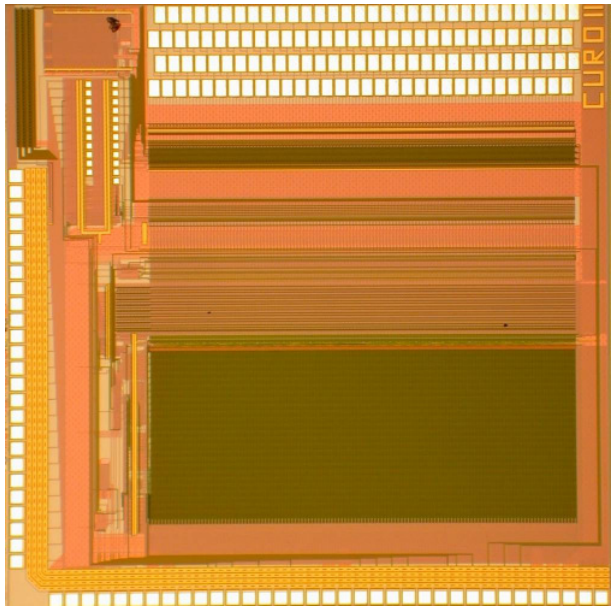
Switching 20V @ 30MHz

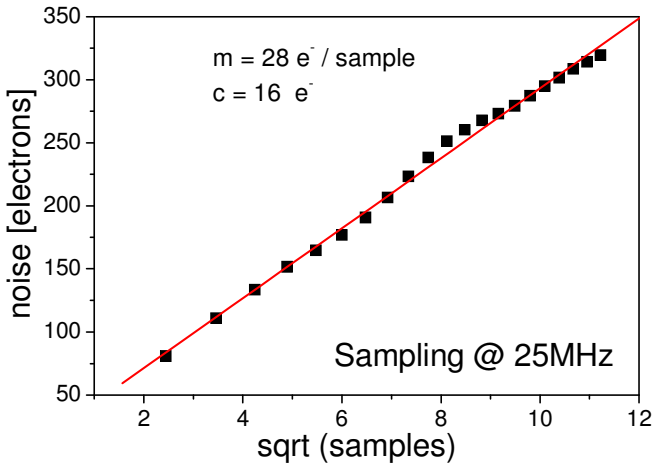


CURO ASIC (Drain Readout)

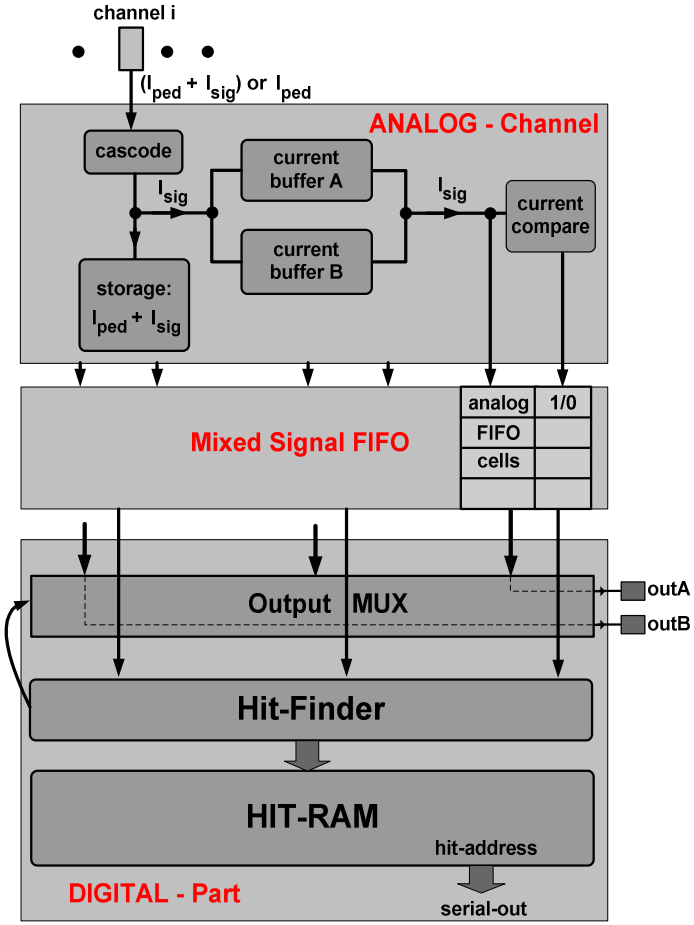
- **128 channel** drain readout chip
- Drain voltages are kept constant with regulated cascode circuits
- Direct **current subtraction** by switched current technique
- Real time **hit finding** and zero suppression
- Hit addresses store in on-chip RAM
- 0.25µm technology. Radiation tolerance should be fine.

- Noise per sampling: 30e$^-$ @ 25MHz
- **Row rate of 25 MHz has been achieved** (i. e. sampling @ 50MHz)
- Digital zero suppression works at >100 MHz



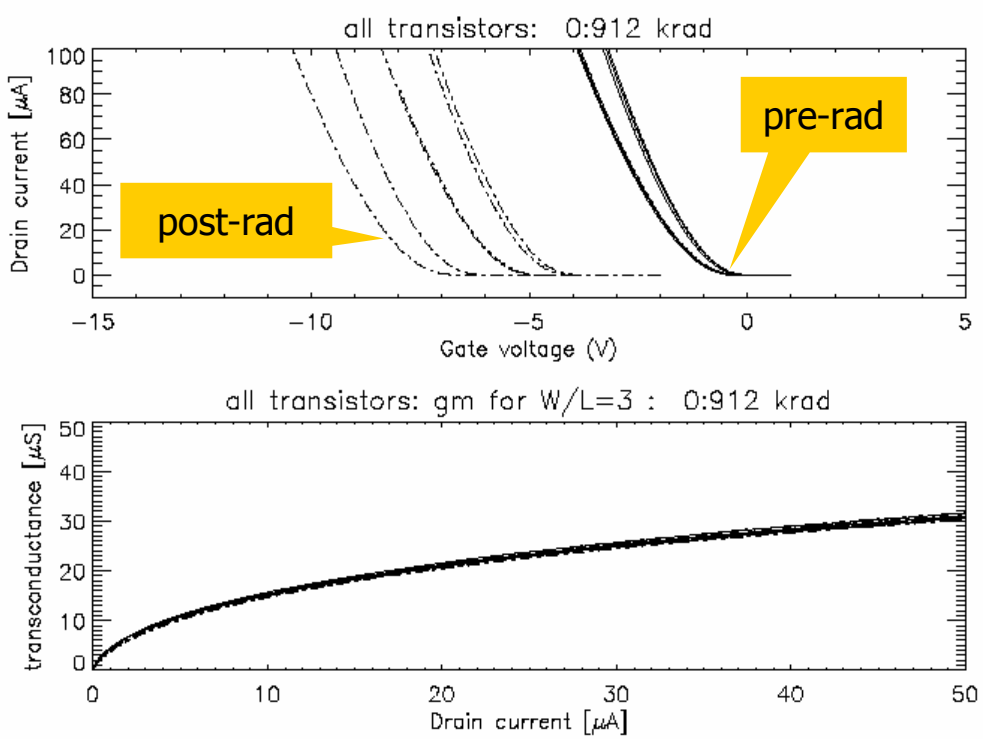


noise for multiple sampling



Irradiation of Single Pixels

- Crucial question: Threshold shift of the (external) MOSFET (oxide thickness ~200nm)
- Irradiations with ^{60}Co and Xrays (~17keV,Mo) up to ~1Mrad



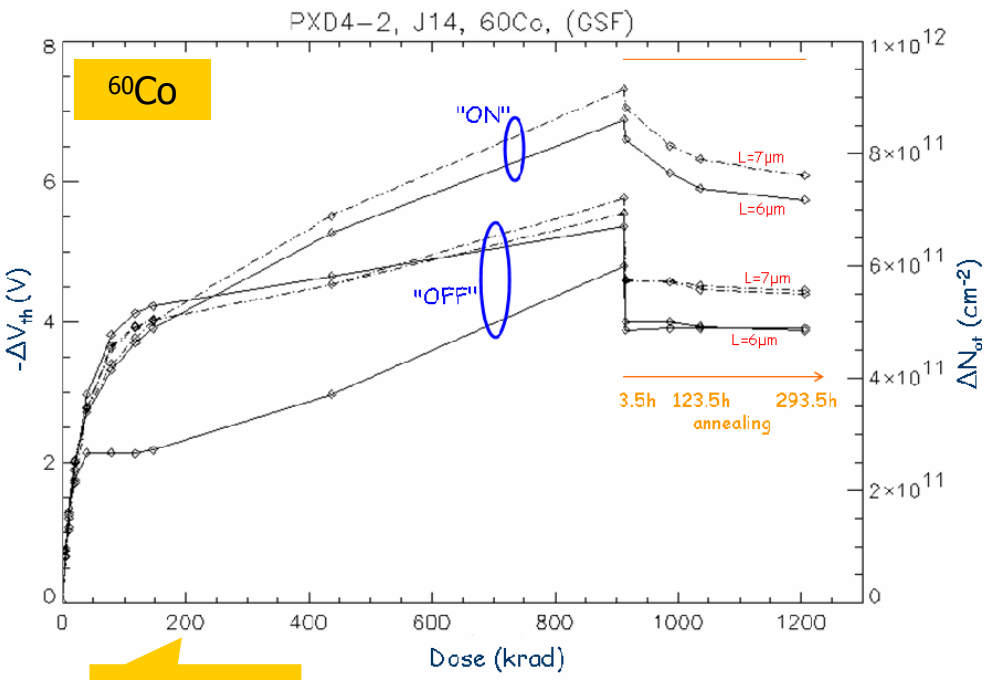
drain current vs. gate voltage

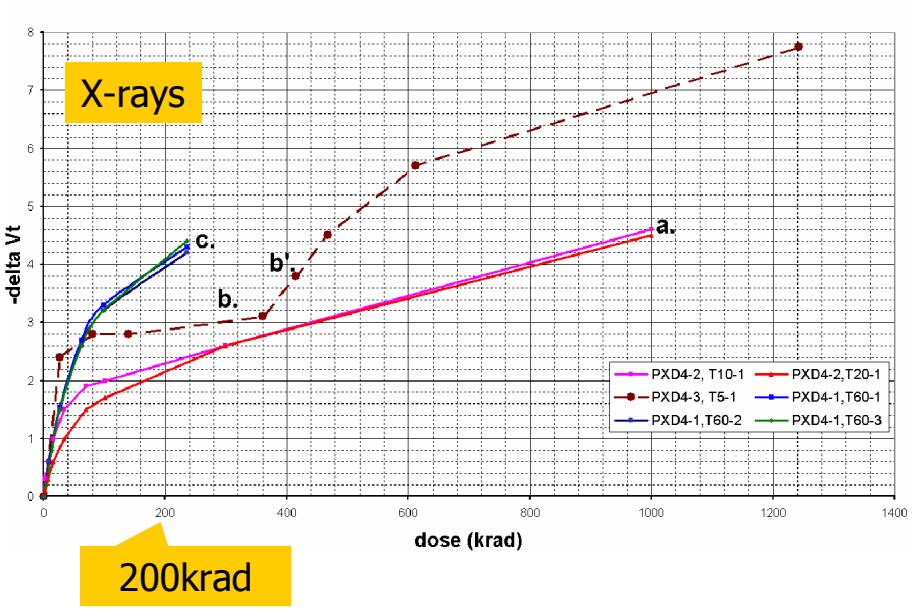
transconductance vs. drain current

- Threshold shifts are negative, as expected from positive oxide charge
- This can be compensated for by variation of bias voltages
- Transconductance remains unchanged ⇒ noise should not degrade

Effect of dose rate / annealing

- **Shifts are small**: only - 4...- 6 V
- Observe saturation after 200 krad
- Device 'off' state is slightly better – good: this is where devices are operated most of the time!

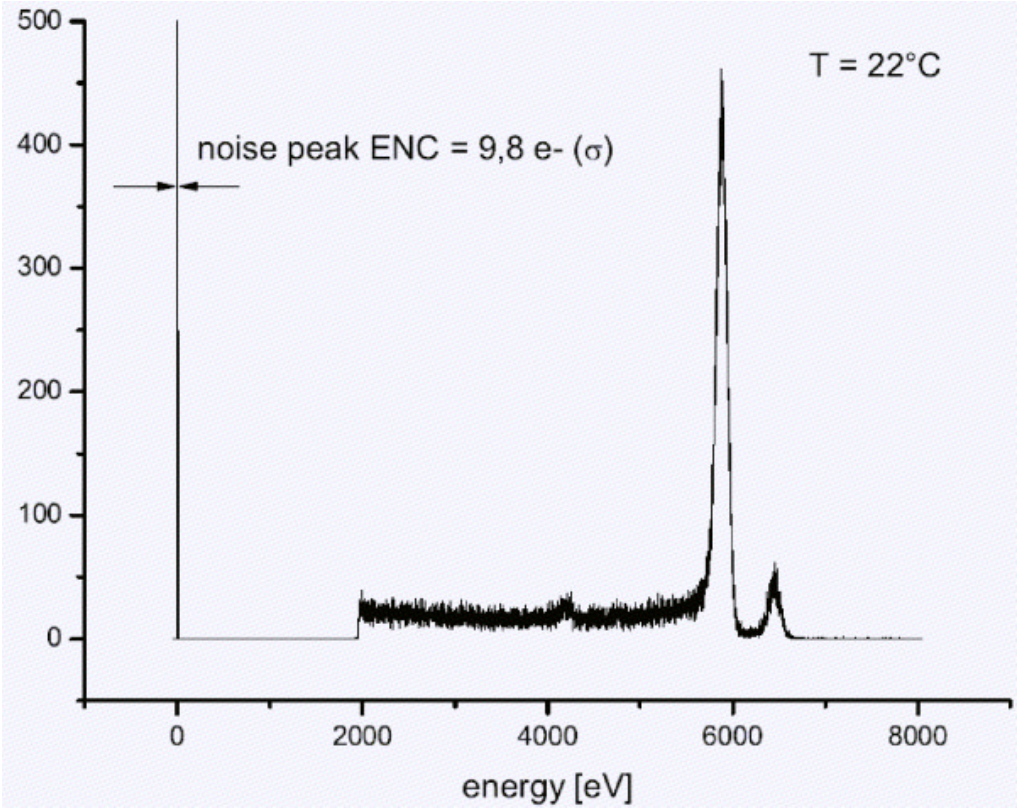




- But: possible explanations for these good results need to be confirmed

Measurements on ILC Pixels: Noise

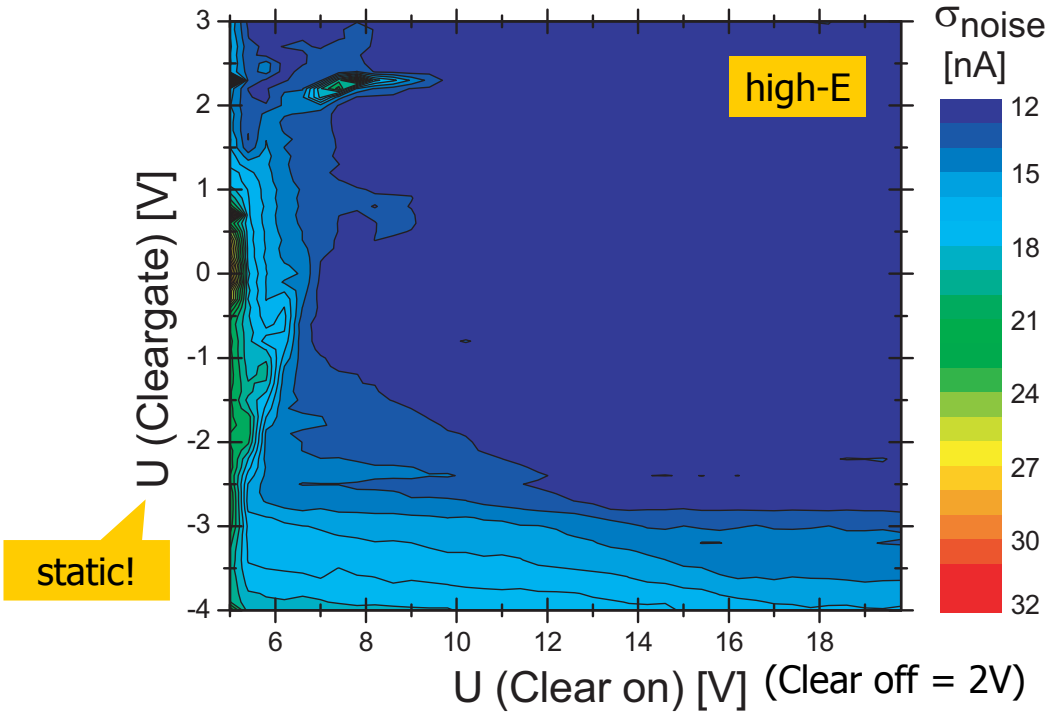
- ^{55}Fe spectrum with ILC structure taken at room temperature with 10µs shaping time:

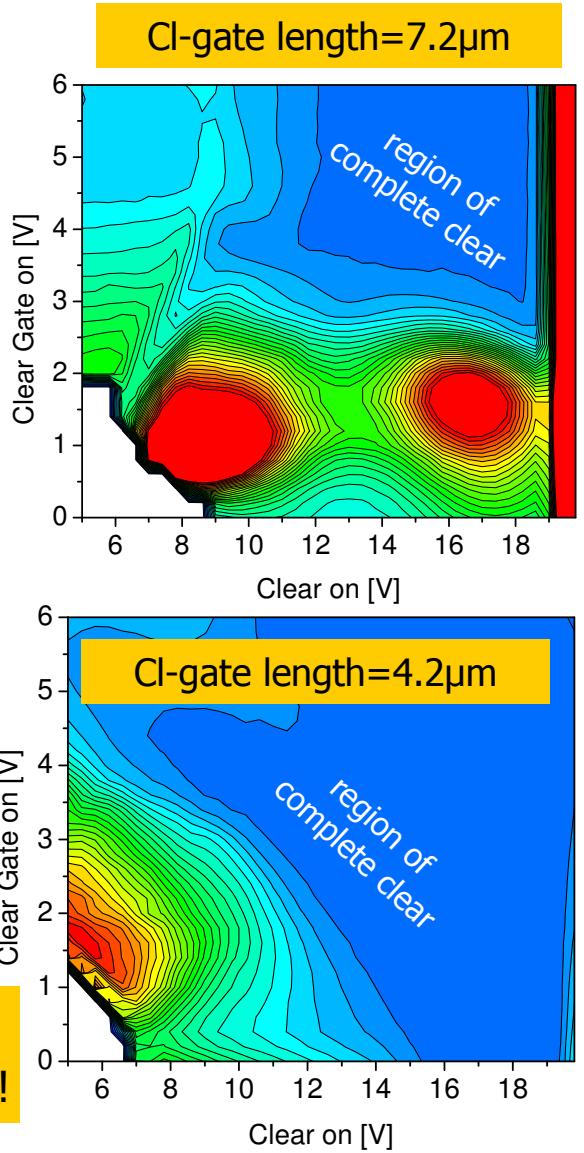


- Noise peak: 10e$^-$
- Best measurements so far (large XEUS structure, cold, slow): 2.2e$^-$
- **DEPFETs regularly provide noise below 10e$^-$** @ room temperature (single devices with slow shaping)!

Clear Efficiency

- Study mini matrix devices in laser setup
- Plot pedestal variations ('noise'). If they are constant, clearing is complete!
- Study various designs (high-E, no high-E), geometries (length of clear gate) and operating conditions (static or clocked clear gate)

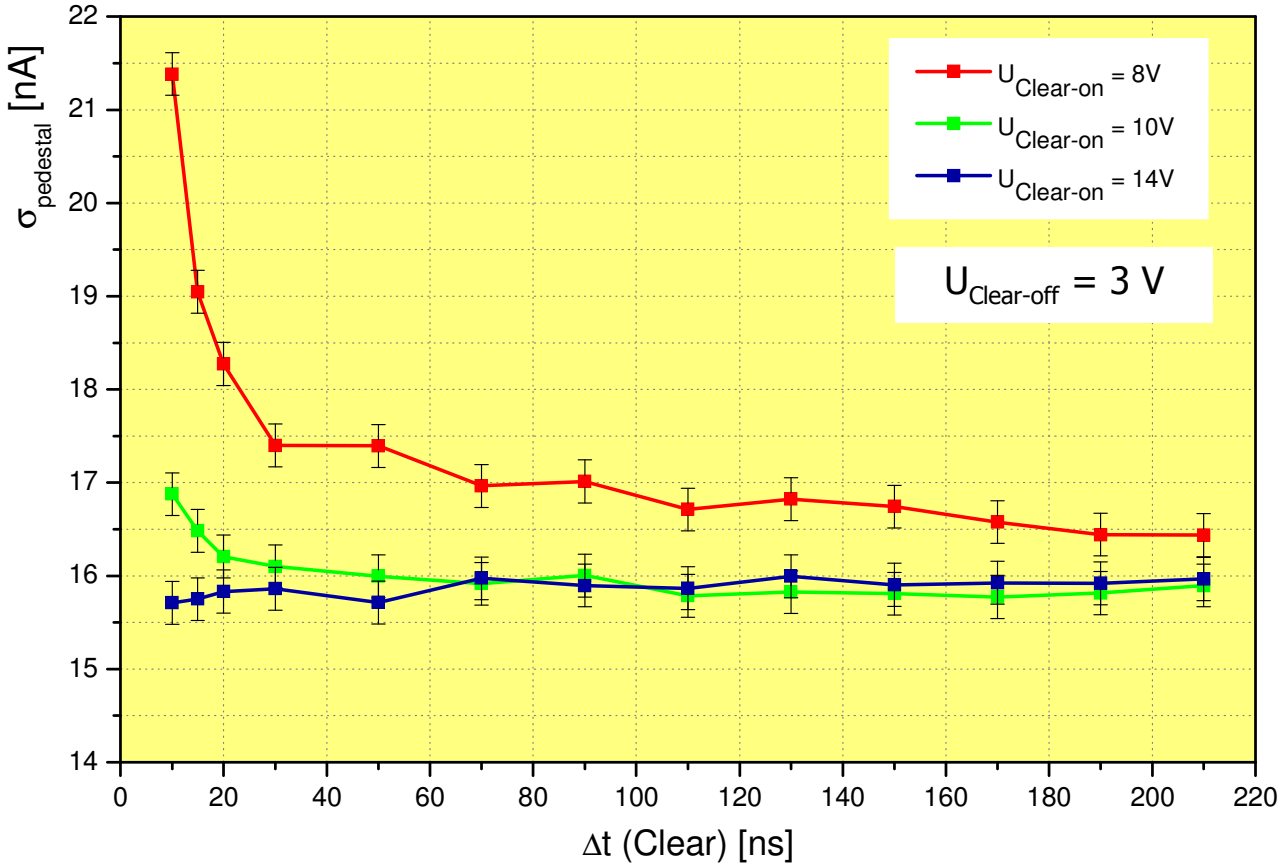




Complete clear achieved with static clear gate !
Required voltages are small (5-7V) – very important for future SWITCHER!

Fast Clearing

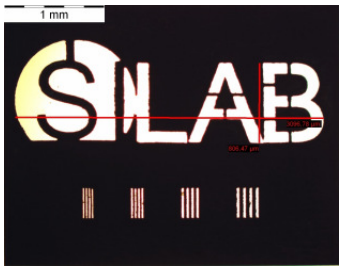
- Study clear efficiency for short clear pulses (new result, not in PRC report!)
- Device with common clear gate, High-E



Complete clear in only 10-20 ns @ ΔV_{clear} = 11-7 V

ILC DEPFET-System in the Lab

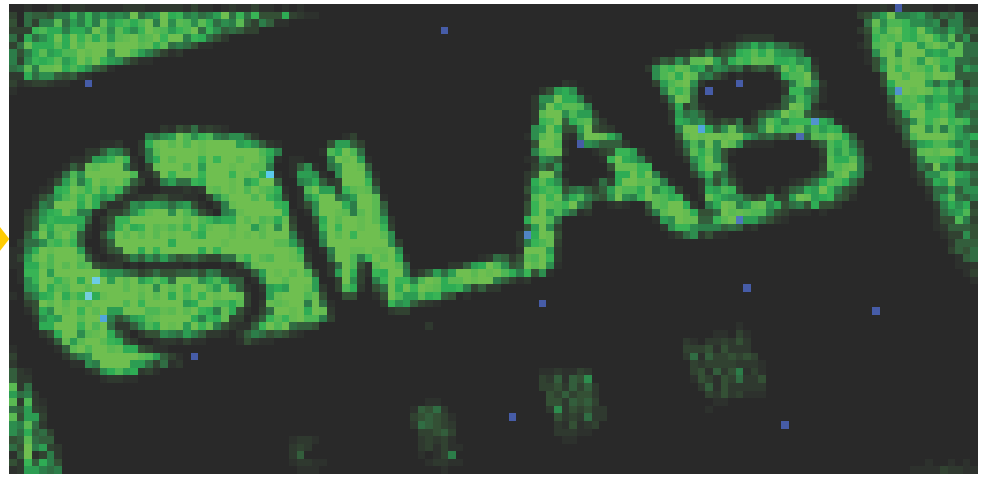
10µm thick Tungsten-Mask

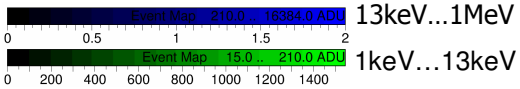


2.7 mm

3.4 mm

irradiation with ^{55}Fe
(6keV γ, 1700 e^-)





ILC system performance in the lab:

- **High speed**: row rate: 0.6 MHz
- **Noise: 230 e^-**

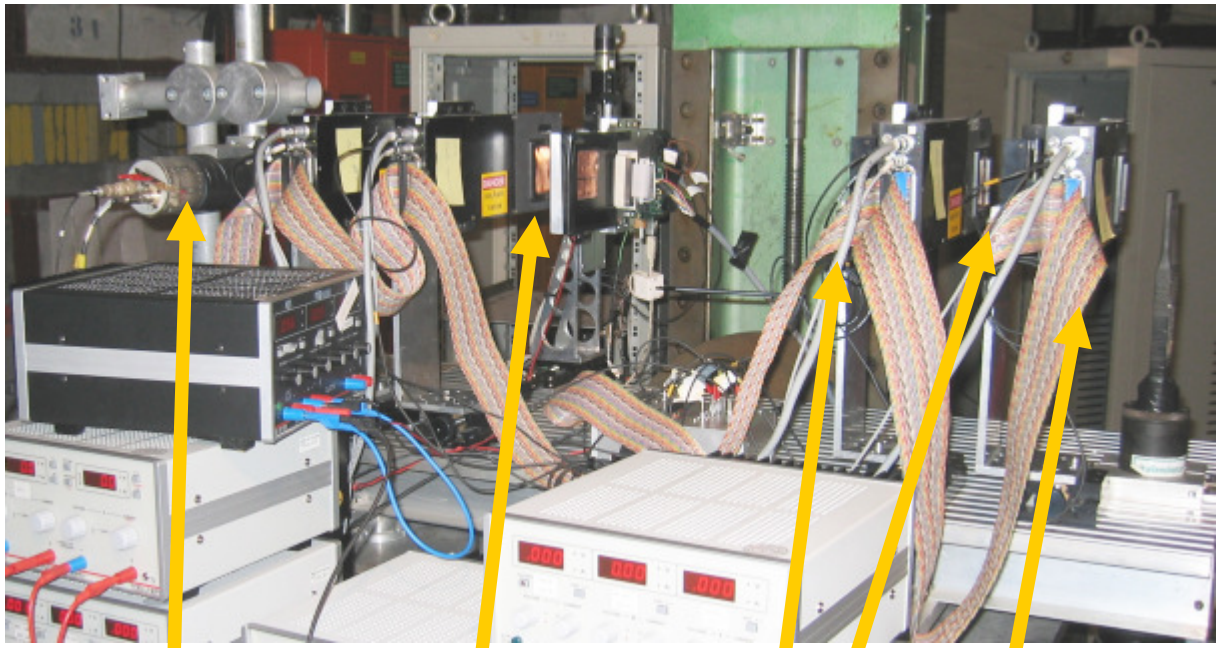
Noise contributions:

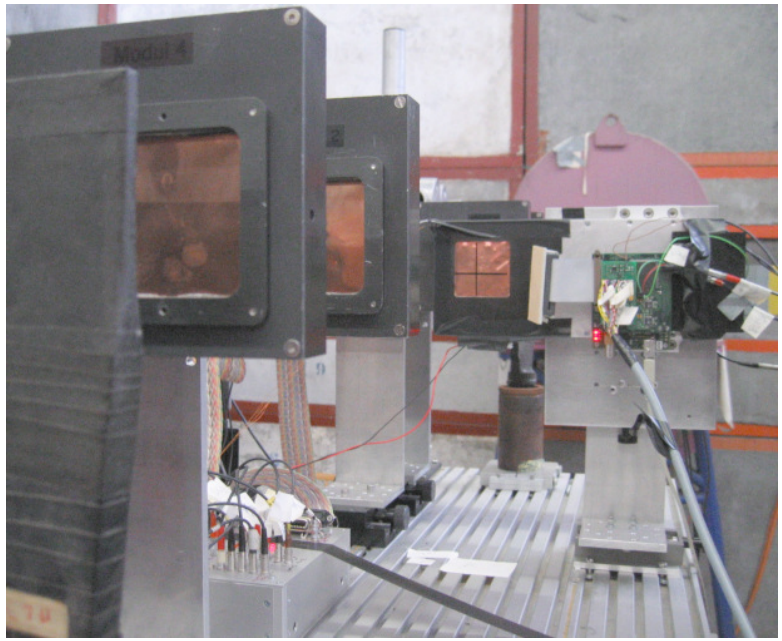
~ 100e- from CURO etc.

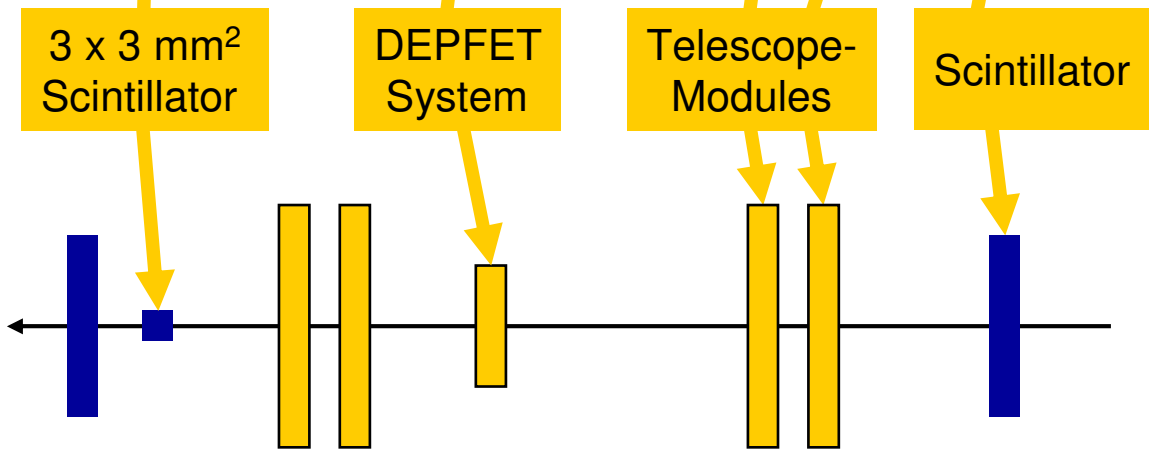
~ 60e- from I2U converter (CURO → ADC)

~ noise pickup of I2U converter

Test Beam Setup (Jan / Feb 2005 @ T24, DESY)



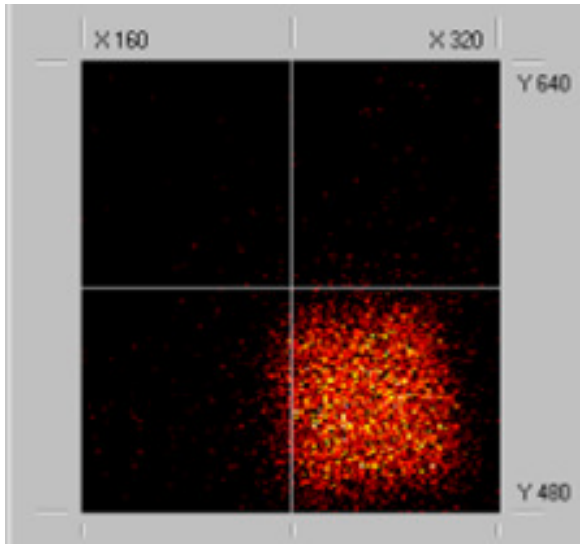




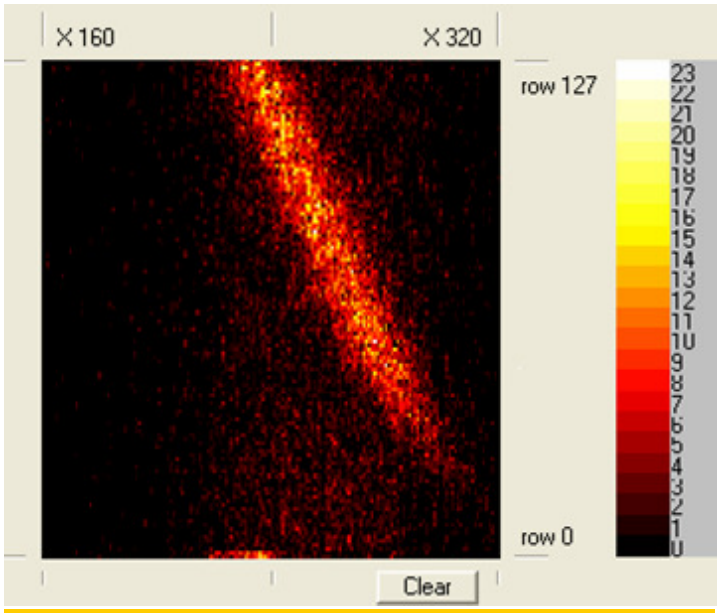
- Beam T24 @ DESY, Jan/Feb. 2005
- Electrons @ 4GeV
- Reference telescope:
  4 Si-strip planes (pitch in x- and y: 50µm)

- Two matrices have been tested with
  4 x 128 pixels of 36µm x 28.5µm

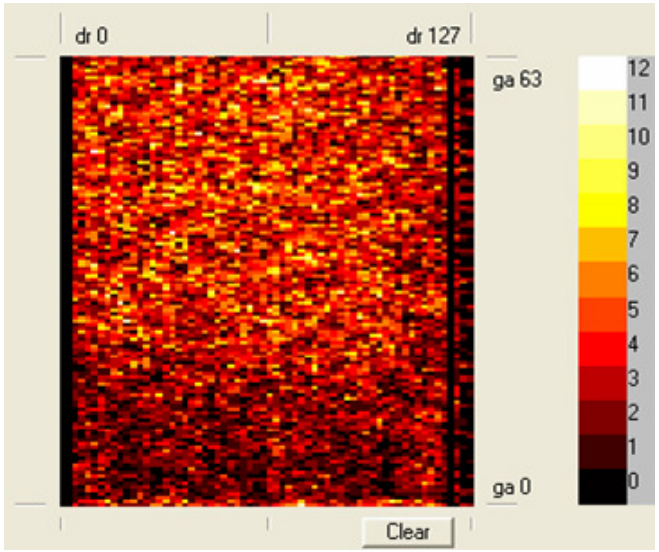
Test Beam Results: Online Correlations



Beam spot on telescope



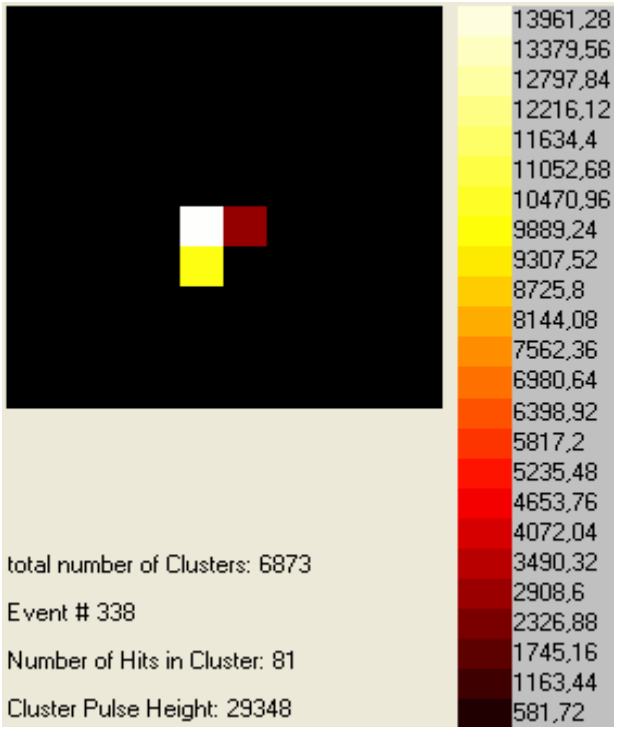
correlation telescope x ⇔ DEPFET x

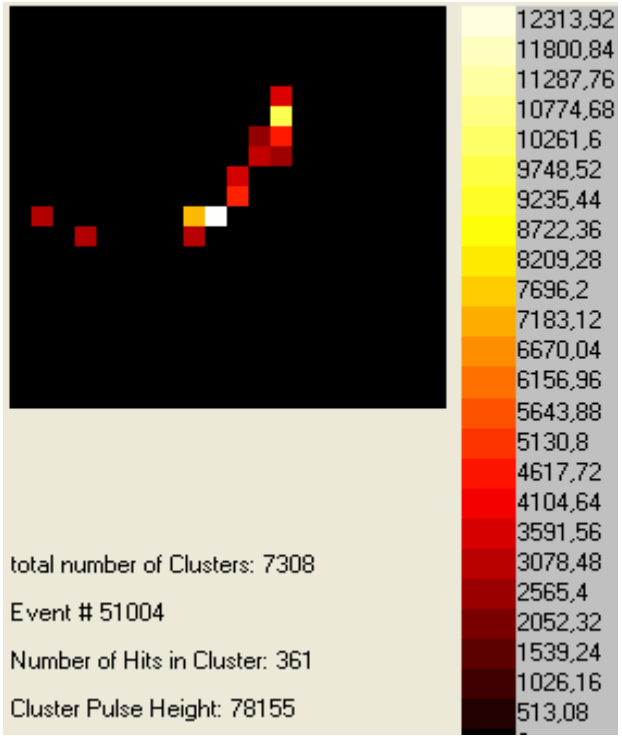


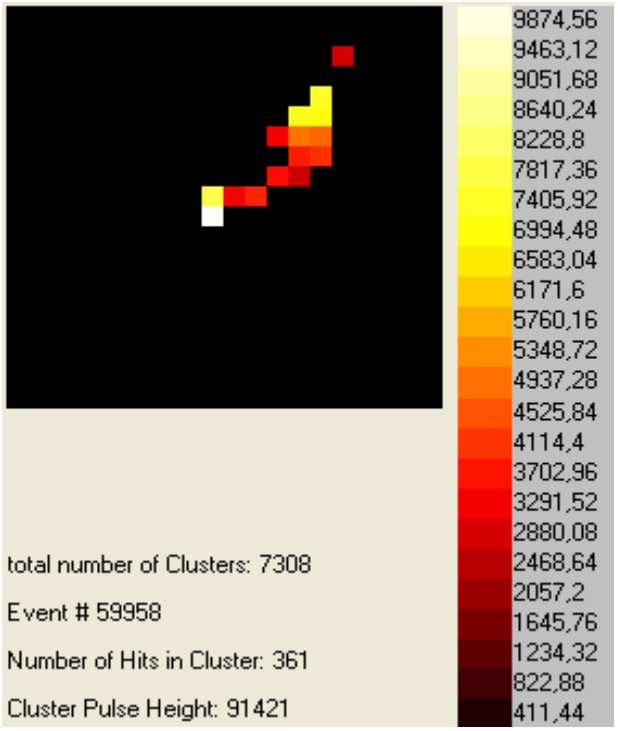
Beam spot on (small) DEPFET

- Event rate: 10Hz
- collected 10 million events
- highE / non-highE in beam
- data analysis ongoing

Test beam: Event Displays







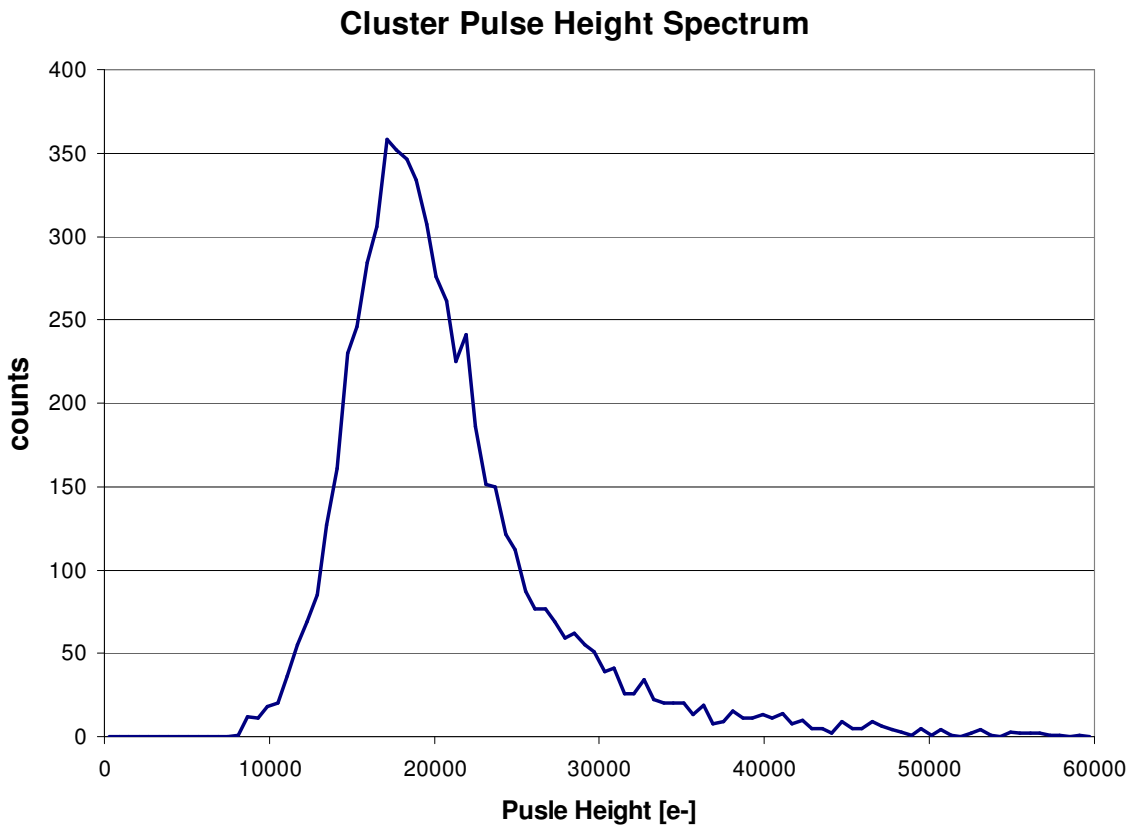
single hit cluster

Some δ-electrons with perpendicular tracks !
(range of tracks is ~ consistent with measured energy of few 100keV)

- Cluster: Only 1-2 pixels hit in x and y at perpendicular beam incidence
- Much more information about event structure due to spectroscopic quality of the device!

Custer Amplitudes

- Amplitude sum in cluster (with preliminary calibration…)



Expected Power Dissipation

- For V_{Drain} = 5V and I_{Drain} = 100µA (conservative values): P_{DEPFET} = 0.5mW per *active* device

- **Layer1** (8 Modules x 2 sides x 512 = 8192 pixels), duty cycle = 1/200:

Sensor:	only active pixels dissipate power	⇒ 8192 x 0.5mW / 200	=	**20 mW**
SWITCHER:	6.3mW per active channel at 50MHz (measured)	⇒ 16 x 6.3mW / 200	=	**0.5 mW**
CURO:	2.8mW / channel (measured)	⇒ 8192 x 2.8mW / 200	=	**114 mW**
			Sum:	**~ 135 mW**

- Scaling up from 18.7 Mpixels (L1) to ~493 Mpixels for **5 layers** gives: **Total: ~ 3.6 W**

- **Note:** Largest dissipation (CUROs) is outside active area where cooling is less problematic!

- This calculation assumes that all chips can be switched into a stand-by mode with ~ zero power dissipation between bunch trains. This feature must be included in future chip versions.

Conclusion

- Our DEPFET prototype module is close to ILC specs
- Achievements:
  - Technology for thin ($\leq$ 50µm) detectors established (total budget of sensor 0.11% X_0)
  - Present Pixel size: 24x33 µm^2 – can go to ~ 20x20 µm^2, limited only by manufacturing equipment !
  - Complete clearing works with short (10ns) clear pulses at moderate voltages. No need to clock clear gate !
  - Radiation tolerance (threshold voltage shift) demonstrated up to 1MRad !
- Advantages DEPFET
  - Charge collection in fully depleted bulk with high charge collection field
  - High S/N (~40 at 100e noise), high spatial resolution (expect ~2µm)
  - Low average power dissipation for full ILC system (4W)
  - Fast readout possible (some 10 MHz)
  - Low material
- Next steps
  - Irradiate chips and full system
  - Operate complete system at full ILC speed
  - Produce thin sensors with larger matrices
  - Design new SWITCHER (lower voltage operation, smaller chip, standby mode, radiation hardness?)
  - Design new CURO (deeper FIFO, standby mode, ADC?, …)