2001 - 2004 R&D on CMOS sensors for Charged Particle Tracking at a Future Linear Collider Vertex Detector

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Outline

- Reminder: principle of operation of CMOS sensors
- Summary of sensor prototypes fabricated since 1999
- New results on tracking performances of small sensors
- Test results of first real scale prototype
- Test results of low doping substrate sensor
- Radiation tolerance
- Next major R&D steps: Sensor & System Developments
- Summary

Advantages of Monolithic Active Pixel Sensors:

⋆ **MAPS combine advantages of CCDs and of Hybrid Pixels:**

♡ they provide as good spatial resolution as CCDs & can be thinned down to the same level

♡ they are much more resistent to neutron radiation and are potentialy much faster than CCDs

Principle of Operation:

⋆ p-type low-resistivity Si

◇ signal generated in epitaxial layer (low doping) → $Q_{mip} \sim$ 80 e^--h pairs / μm

◇ signal charge collected by n-well

◇ excess carriers diffuse thermally to n-wells with help of reflection on boundaries with p-well and substrate (high doping)

◇ no external depletion voltage

⇒ **watch feature size, epitaxial layer thickness, nb of metal layers, yield, ...**

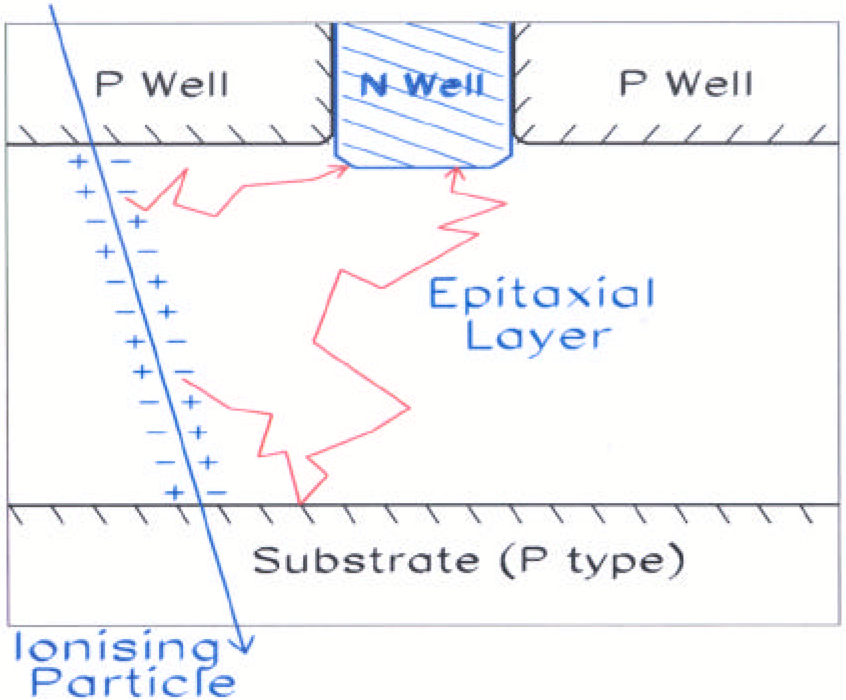


Figure 1: Schematic view of the charge collection in a CMOS sensor pixel designed for charged particle tracking.

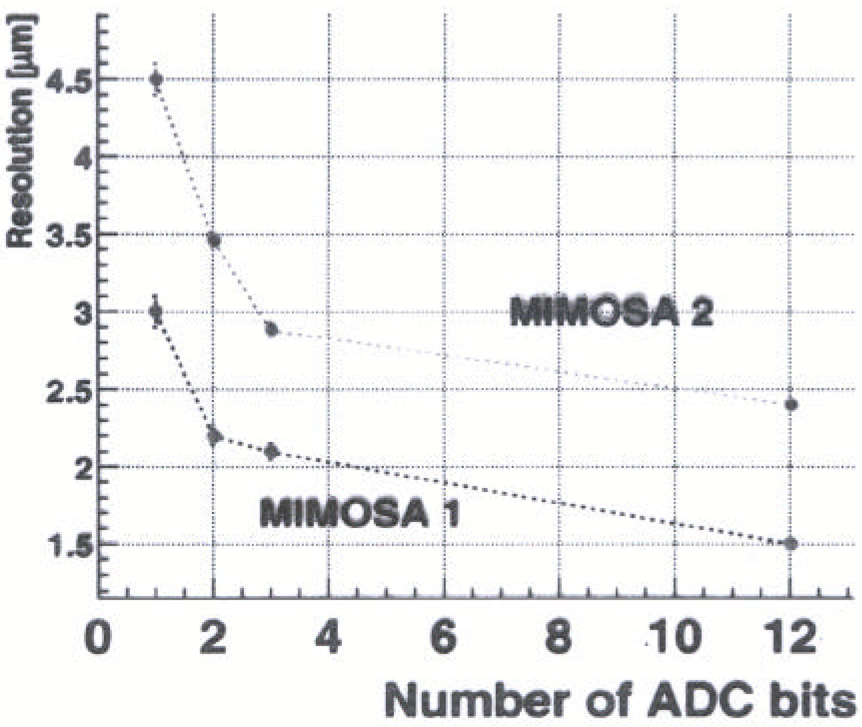
Summary of prototypes fabricated

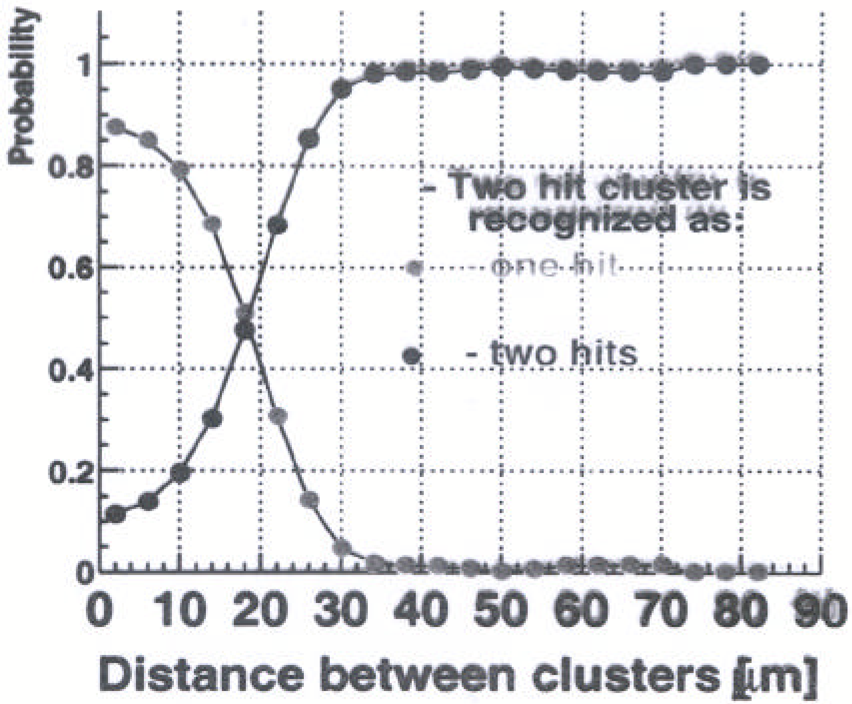
- 6 prototypes fabricated since 1999 (5 tested with 120 GeV/c π^- CERN-SPS)

sensor generation	year	process	epitax.	pitch	metal	peculiarity
MIMOSA-1	1999	AMS 0.6μm	14μm	20μm	3M	thick epitaxy
MIMOSA-2	2000	MIETEC 0.35μm	4.2μm	20μm	5M	thin epitaxy
MIMOSA-3	2001	IBM 0.25μm	2μm	8μm	3M	deep sub-μm
MIMOSA-4	2001	AMS 0.35μm	0 !	20μm	3M	low doping substrate
MIMOSA-5	2001	AMS 0.6μm	14μm	17μm	3M	real scale (10^6 pixels)
MIMOSA-6	2002	MIETEC 0.35μm	4.2μm	28μm	5M	column // r.o. integ. sparsif.

Spatial resolution

- $\sigma_{sp} \sim$ 1.5 (2.2) μm with 14 (4) μm epitaxial layer



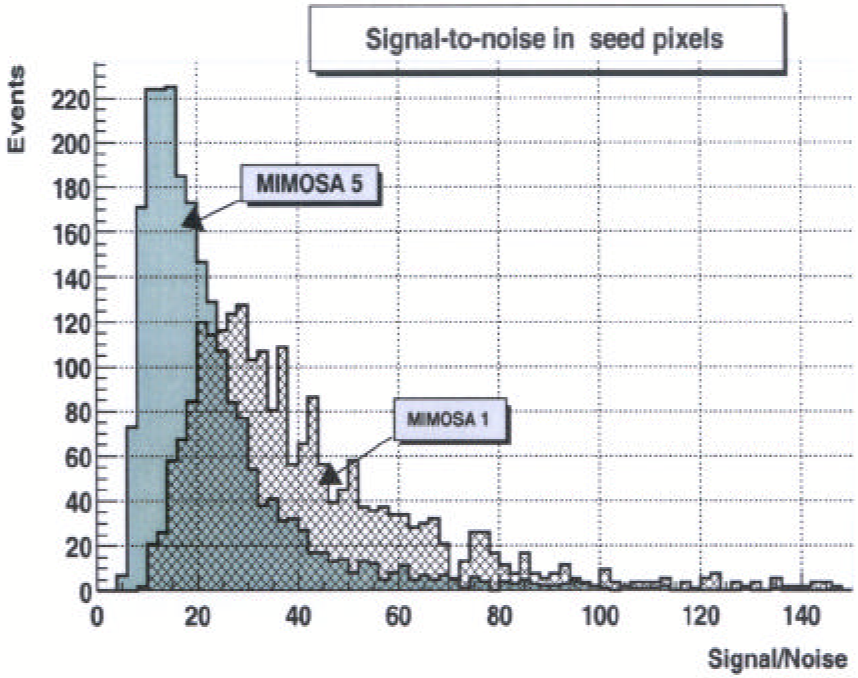


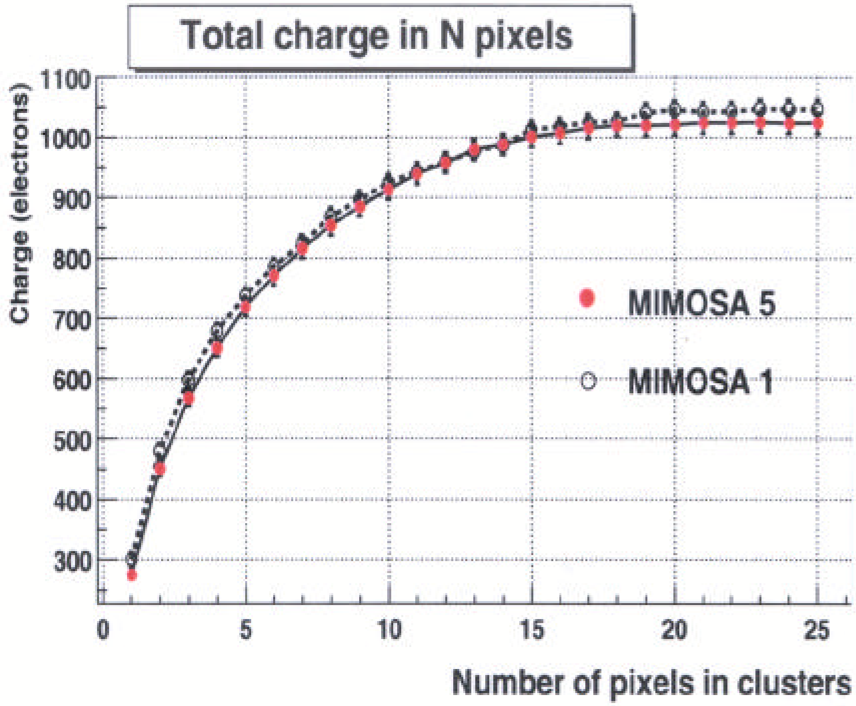
- single point resolution as a function of ADC-bit encoding:

  $\sigma_{sp} \sim$ 2-2.5 μm for 3 bits ($\sim$ 3-4 μm for 1 bit ...)
- double track (hit) resolution: excellent down to 30 μm distance

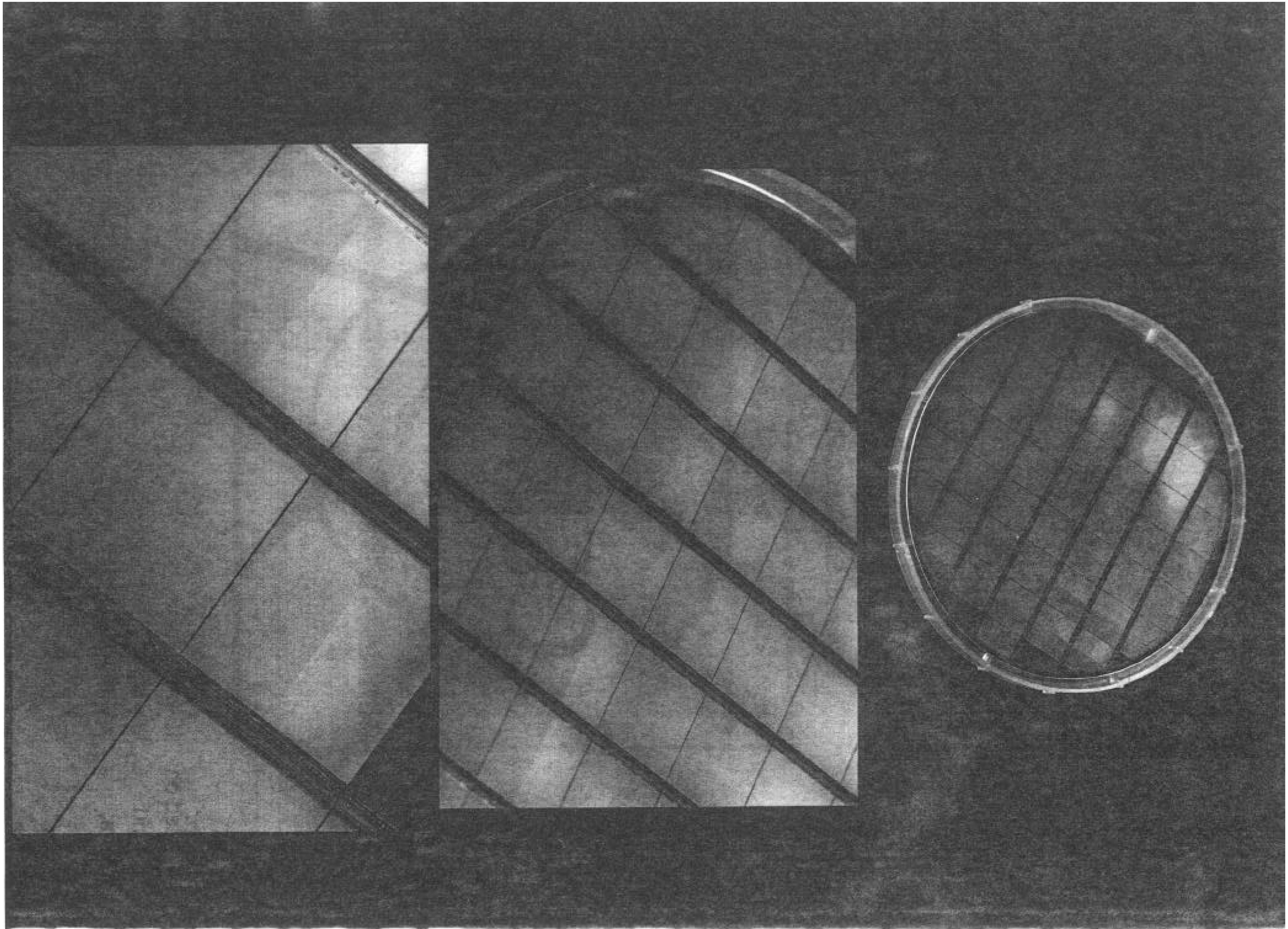
MIMOSA-5: 1st real scale prototype

- ▶ chip of 4 matrices of 512x512 ($17 \times 17\ \mu m^2$) pixels read-out in parallel, etched to 120 μm
  - $\hookrightarrow$ exposed to 120 GeV/c π^- beam at CERN-SPS
- • comparison with MIMOSA-1 (same 0.6 μm AMS process, but 64x64 pixels)



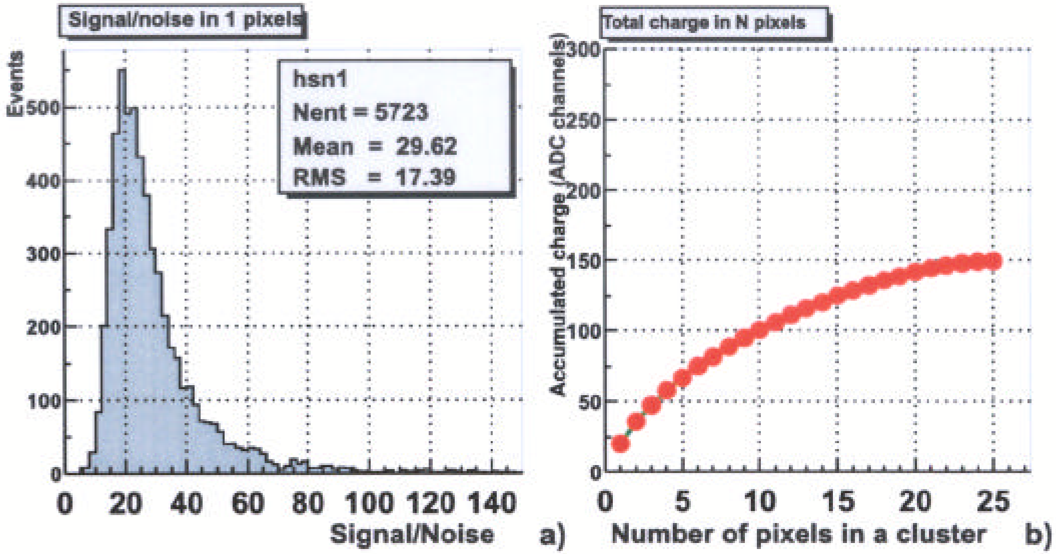


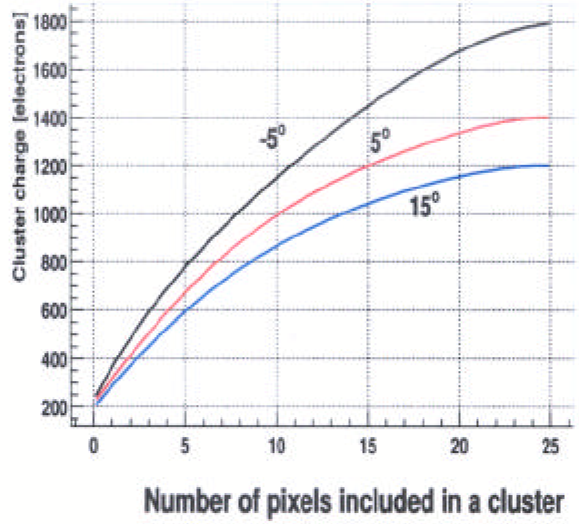
▶ prelim. result: detection efficiency $\sim$ 99.3 %, $\sigma_{sp} \sim 1.7\ \mu m$, $\sigma_{\overline{gain}} \sim 0.2$ %
(twice noise of M1 due to different serial r.o. architecture)



Test results with MIMOSA-4 (1/2)

► 0.35 μm AMS process without epitaxial layer but with low doping (resistivity) substrate





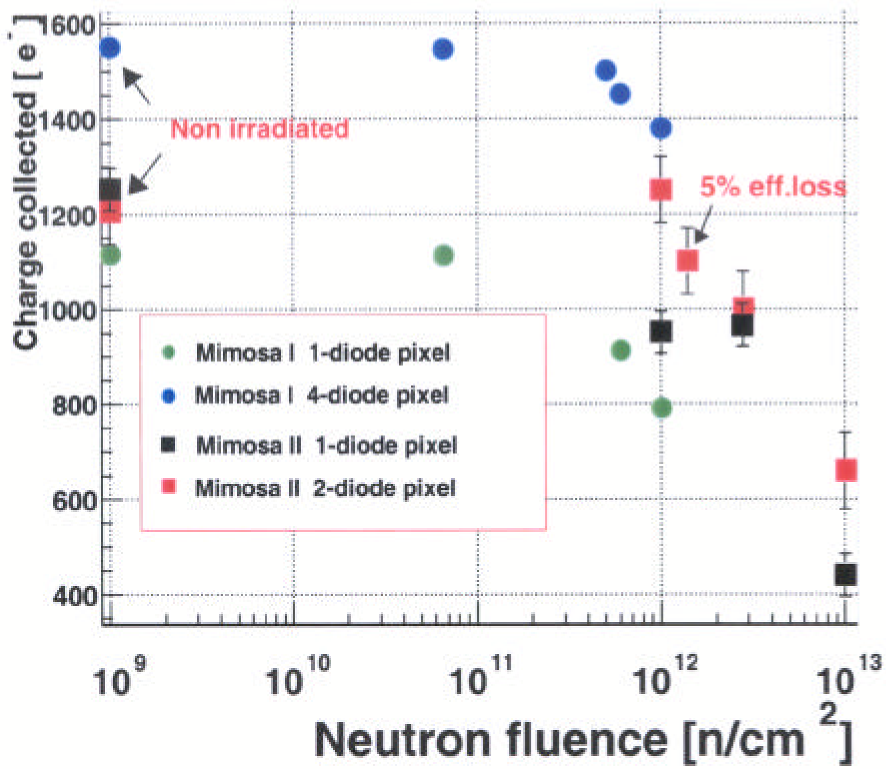
► Observed performances with 120 GeV/c π^- at CERN-SPS (T_{Room}):

♣ detection efficiency ~ 99.7 %   ♣ single point resolution ~ 4 μm (20 μm pitch)

► Low temperature still improve sensor performances (studies under way)

⇒ **Technology without epitaxial layer seems worth investigating & optimising**

Radiation tolerance



- ▶ Neutron irradiations up to $10^{13} \mathrm{n}_{eq}/cm^2$

  ↪ fluences of $\lesssim 10^{12} \mathrm{n}_{eq}/cm^2$ are still acceptable (T effect ?)

- ▶ Ionising radiation: few 100 kRad acceptable (better if $T << 0^{\circ}C$?)

  ↪ exact source(s) of performance loss under investigation

- ▶ Ccl: radiation tolerance at a FLC should not be an issue (yearly: $\sim 10^{9} \mathrm{n}_{eq}/cm^2$ and 50 kRad) X Safety Factor of 10 & 5 ?

Plans for 2003 – 2004

- Sensor development towards fast signal processing & data compression:
  - MIMOSA-6: col. // r.o. & integ. signal proc. $\rightarrow$ tests at CERN-SPS in June
  - MIMOSA-7: alternative signal collection & processing architecture (photoFET)
    $\hookrightarrow$ design in 0.25 μm AMS (8 μm epitaxy) $\rightarrow$ submission in June $\rightarrow$ tests in Autumn
  - MIMOSA-8/9: best out of MIMOSA-6/7 $\rightarrow$ fast medium size sensor $<$ Summer 2004

- System integration studies have started:
  - ◇ DAS card being designed
  - ◇ detailed effect of detector material, pixel size, etc. on $\gtrsim$ 500 GeV physics
  - ◇ GEANT-4 description of CMOS Vertex Detector started
  - ◇ pulsed powering studies with MIMOSA-5 in preparation
  - ◇ estimation of limit in $\overline{P_{diss}}$ compatible with modest active cooling
  - ◇ achieve $\lesssim$ 50 μm thinning on real scale chip (MIMOSA-5)

    $\Rightarrow$ preliminary ladder prototype in 2005 (?)

- Find optimum of granularity$\star$signal proc. speed$\star$mat. budget with physics simulations

Signal processing

- Governed by $N(e^{\pm}_{BS})$ in 1st Vertex Detector layer:
  $N^{sim}_{\pm}(90^{\circ}) \gtrsim 5\ e^{\pm} / cm^2$ / BX at 500 GeV (R=15 mm)
  $\hookrightarrow$ occupancy $\gtrsim$ 3-5 % in 100 μs ($m_{clust} \sim 5$)

- Safety factors (simulation accuracy, uncertainty on B, higher $\sqrt{s}$, shorter Δt_{BX})
  $\leadsto$ occ. $\gtrsim$ 15-25 % in 100 μs

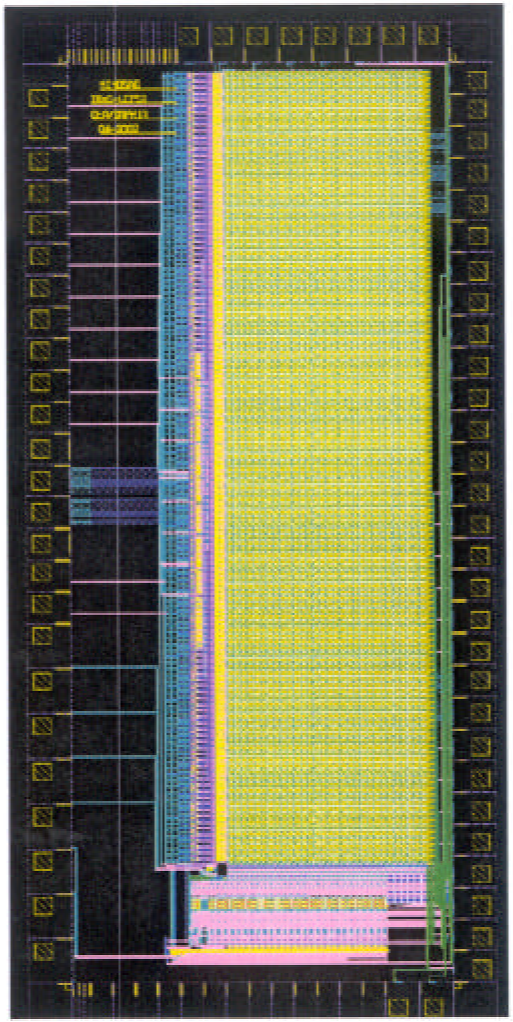
- Goal: $t_{L1} \sim$ 25-50 μs (R&D needed)
  $t^{L2-5}_{lect} \sim 100 \longrightarrow 200\ \mu s$ (no major difficulty)

- major obstacle: data flux (L1)
  $\hookrightarrow$ 15 bits/pixel, $t_{L1} \sim 25\ \mu s \longrightarrow \sim$ 500 Gbits/s/10^6 pixels ($e^{\pm}_{BS}$: 5 Gbits/s)

$\Rightarrow$ **Next CMOS sensor prototypes address**
Signal Processing Speed AND Data Compression

MIMOSA-6: 1st sensor with col.// r.o. & integ.sparsif.

- 1st sensor with sparsification integrated / substrate & column // r.o.:



⋗ amplification (x5.5) and noise suppression (CDS) on pixel

⋗ discriminator integrated on chip periphery (1 per column)

♣ 0.35 μm MIETEC technology (same as MIMOSA-2)

♣ 30 columns read-out in ⇊ (128 pixels per column)

⋗ 30 MHz r.o. frequency but 6 clock cycles per pixel

⇒ 5 MHz effective r.o. frequency

♣ pixels of 28 μm pitch (29 transistors, 3 capacitors)

⋖ $P_{diss} \sim 500\ \mu W$ per column and frame r.o. cycle

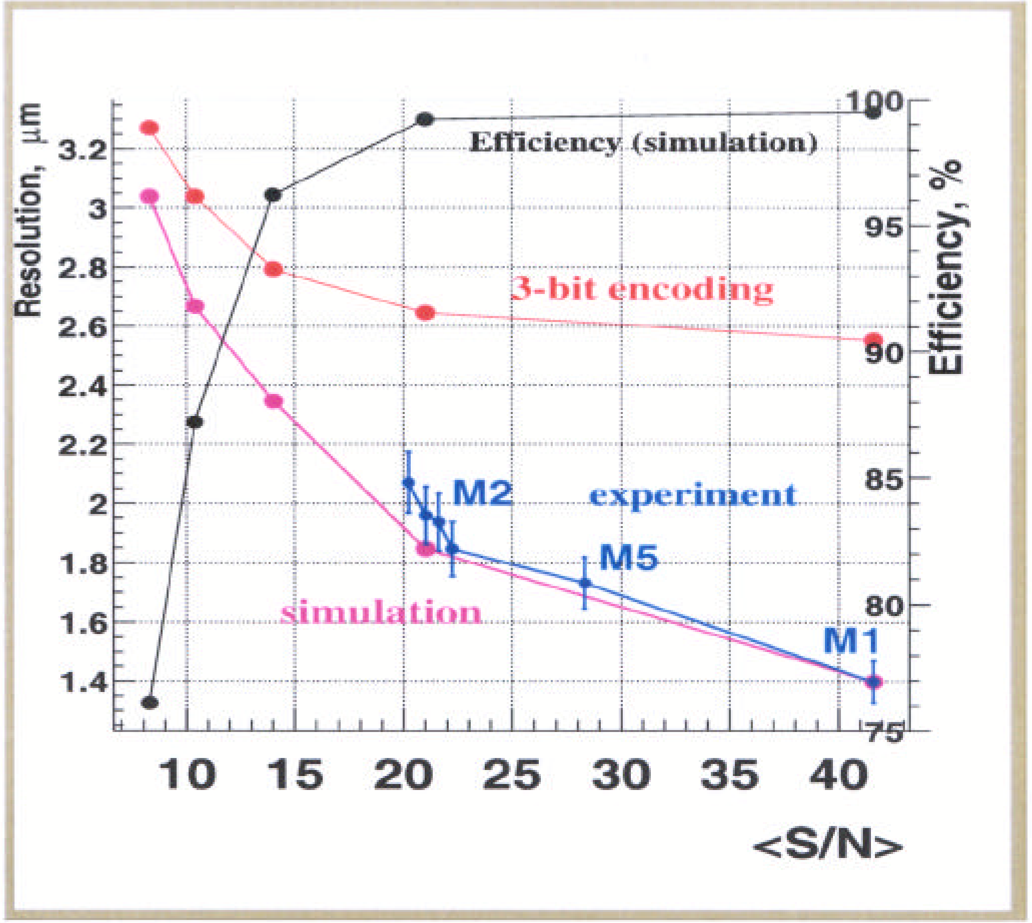
♣ tests under way in Strasbourg and Saclay

Fast Data Processing: Effect of Increased Noise

▶ on-chip data proc. to reduce data flux (∅) due to fast r.o. of very granular sensors

→ pre-amplif., noise supp., ADC, discri., ... shared between pixel and chip periphery

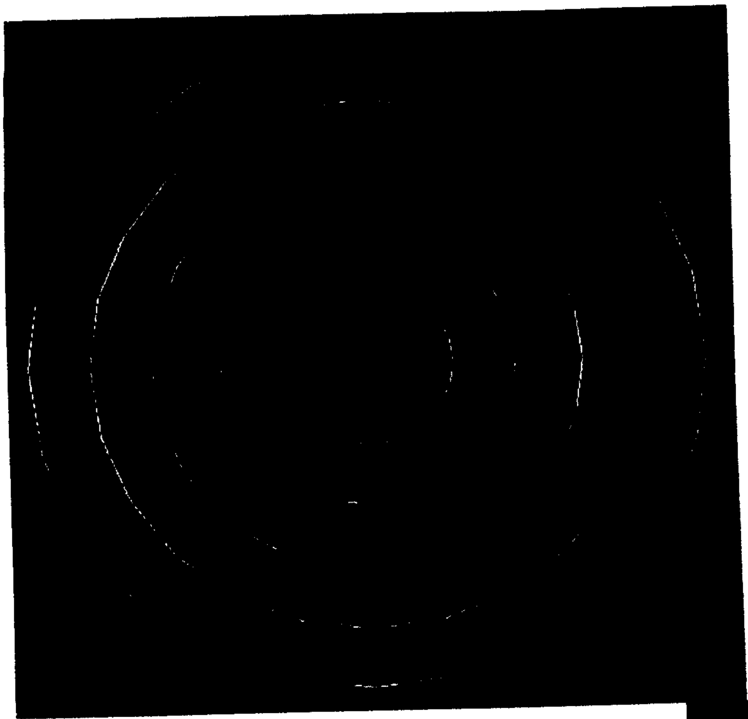
⇒ noise may increase substantially → csq on ϵ_{det} & σ_{sp} ?



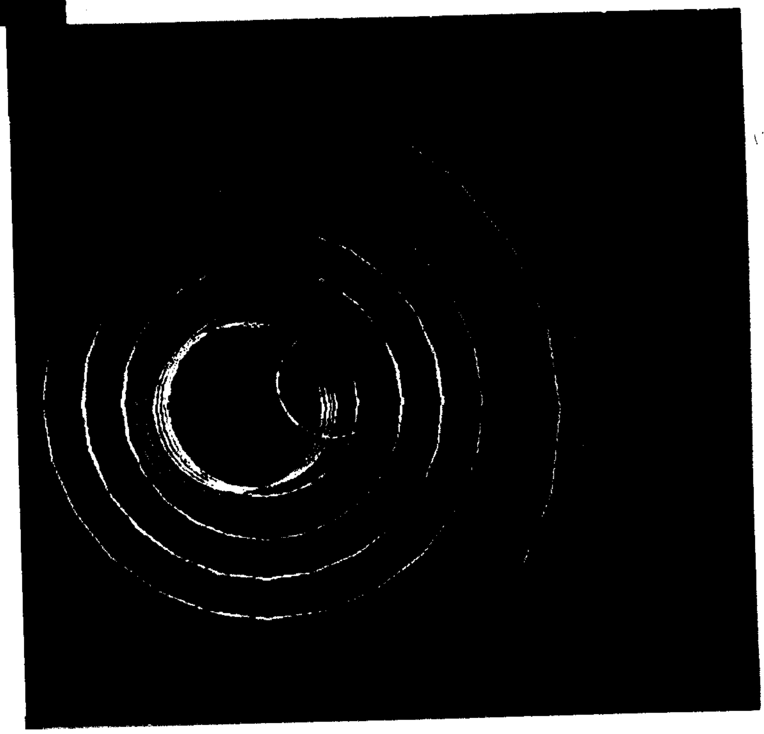
▶ Study based on M-1,-2,-5 data:

- $\epsilon_{det} \gtrsim 96$ % if S/N $\gtrsim 14$
- $\sigma_{sp} \lesssim 3\ \mu m$ even if S/N ~ 10 and only 3-bit encoding

View of the VXD in MOKKA



- 50 µm thick carbon fibre mecanical support
- 50 µm thick CMOS sensor
  - $X/X_0 \approx 0.08$ %



- Present Work :
  - tracking algorithm implementation
  - impact parameter resolution

- Caution ! This is just a starting point, the final geometry may be totally different.

Distribution of Tasks

R&D Topic	Univ. Geneva	Univ. Hamburg	IReS-LEPSI	DESY	NIKHEF Amster.	DAPNIA
Intrinsic Perfo.			X		X	X
R.O.Circuits			X			X
Chip Tests		X	X	X		X
Rad. Tolerance		x	X	x	x	
DAS circuits	X					
Thinning			X	x	X	
Mech. & Cool.		X		X	X	

Summary

⋄ CMOS sensors offer a very promising technical solution for a vertex detector of unprecedented performances at a future Linear Collider

⋄ Several requirements for this application are already fulfiled: detection efficiency, spatial resolution (3-bits), double hit resolution, radiation tolerance ($\sim$), real scale sensors, low doping substrate technology, etc.

⋄ Until 2004, substantial progress expected on fast signal processing (goal $\sim$ 25 μs) and system integration $\rightarrow$ prototype ladder in 2005 (?)