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A DEPFET Pixel Vertex Detector for TESLA Proposal and Prototyping Report

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Abstract

DEPFET pixels offer a unique possibility for a high resolution pixel vertex detector as the innermost component of the tracking system in the TESLA detector. DEPFET pixels excel in comparison to other pixel detectors in the simultaneous achievement of high spatial, energy and time resolution even at room temperature operation. In the DEPFET pixel scheme the signal charge is not shifted out but is stored in the pixel until readout. Multiple readout is possible. The detector itself can be made very thin and does consume very little power. In this note the concept to use the DEPFET technology for the TESLA vertex detector is discussed. Possible design options for a DEPFET based vertex detector are presented and the progress of the R&D program which is presently carried out to meet the requirements at TESLA is described. In particular the advancements in sensor optimization and in the development of a fast readout scheme are discussed.

1 Introduction

At TESLA efficient and good flavor identification and separation is required, for example the accurate determination of the Higgs branching ratios $H \to b\bar{b}, c\bar{c}, gg, \tau^+\tau^-$. Identification of charm quarks is also relevant for a complete reconstruction of the kinematics e.g. in the process $e^+e^- \to W^+W^- \to c\bar{s}l^-\nu$. Another important aspect is the separation of $b(c)$ from $\bar{b}(\bar{c})$ decays via the vertex charge to optimize the sensitivity in the angular analysis of W pair or Higgs production which is sensitive to new anomalous couplings [1].

The average impact parameter of tracks from B-hadron decays is approximately $300\,\mu$m and therefore might suggest that modest impact parameter performance may be sufficient. This is misleading for several reasons: first, the average impact parameters from τ and charmed particle decays are smaller by a factor of 3 to 4. In addition the experience at LEP and SLD has shown that it is desirable to perform a correct assignment of all tracks to primary, secondary and tertiary vertices in order to allow to determine the vertex mass and charge. The former will greatly improve the separation between b, c and light quarks while the latter will to some extent allow to separate between quark and anti-quark.

The performance goal as defined in the TESLA TDR corresponds to an impact parameter resolution of $\sigma_d = 5\,\mu\text{m} \oplus \frac{10\mu m\, GeV/c}{P \sin^{3/2}\theta}$ [1], where P denotes the momentum and θ the angle of incidence with respect to the sensor surface of the charged particle. The first contribution depends on the point resolution which itself is dominated by the pixel size and the mechanical stability of the device. The second term is due to multiple scattering which depends on the amount of material the charged particle has to traverse on its path.

In addition the background conditions and time structure of the accelerator[1] influence the design of the vertex detector. Due to very prominent beamstrahlung near the interaction point the number of hits in layer 1, situated at a radius of 15 mm just outside the beam pipe, for each bunch crossing and per mm^2 is 0.03 (0.05) for $\sqrt{s}$=500 (800) GeV and a magnetic field of 4 T [1]. In order to assure an occupancy of the vertex detector which does not compromise the pattern recognition abilities the pixel size needs to be kept small and the readout speed large. On the other hand the amount of material should be minimised disfavouring a solution where each pixel sensor

[1] bunch spacing 337 (176) ns, pulse length 950 (860) μs, bunches per pulse 2820 (4886), repetition rate 5 (4) Hz at $\sqrt{s}$ = 500 (800) GeV

is instrumented by its own readout unit e.g. via bump bond connections as discussed in the hybrid pixel option [1].

2 The DEPFET principle and operation

The DEPleted Field Effect Transistor structure, abbreviated DEPFET, provides detection and amplification properties jointly. The concept was proposed in 1987 [2] and experimentally confirmed in 1990 [3]. A 2×2 DEPFET pixel matrix was realized and operated in 1997 [4] and a 32×32 [5] and a 64×64 pixel imaging system presented in 1999 and 2000 [6–9].

The DEPFET principle of operation is shown in figure 1. A MOS or junction field effect transistor is integrated onto a detector substrate. By means of sidewards depletion [11] and additional n-implants below the transistor a potential minimum for electrons is created underneath ($\sim 1\,\mu$m) the transistor channel. This can be considered as an internal gate of the transistor. A particle entering the detector creates electron-hole pairs in the fully depleted silicon substrate. While the holes drift into the rear contact of the detector, the electrons are collected in the internal gate where they are stored. The signal charge leads to a change in the potential of the internal gate, resulting in a modulation of the channel current of the transistor.

The simultaneous detection and amplification feature makes DEPFET pixel detectors very attractive for low noise operation [8, 10]. In the case of TESLA the use of very thin ($\sim 50\,\mu$m) detectors operated with very low power consumption (see detailed discussion below) should be possible. The low noise operation is obtained because the capacitance of the internal gate can be made very small (several 10 fF), much smaller than the cell area suggests. Furthermore, no external connection circuitry to the first amplification stage is needed. External amplification enters only at the second level stage. This leads to an excellent noise performance already at room temperature. The pixel delivers a current signal which is roughly proportional to the number of collected electrons in the internal gate. Signal electrons as well as electrons accumulated from bulk leakage current must be removed from the internal gate after readout. Clearing is obtained by periodically applying a positive voltage pulse to a clear contact (pulsed clear mechanism). Other clear mechanisms have also been studied [4].

The principle of operation of a large DEPFET matrix is shown in fig. 2. Rows are selected by applying a voltage to the external gate of a row. Drains

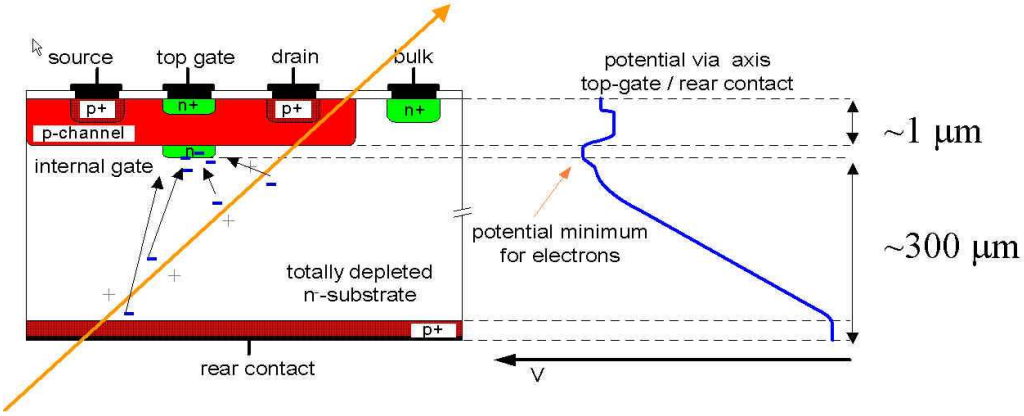

Figure 1: *Cross-section of a DEPFET pixel (left side) and potential between top gate and rear contact as function of depth (right side).*

are connected column-wise. The drain current of each pixel in a selected row is detected and amplified in a dedicated amplification circuit. Pedestals are taken the same way several cycles before and subtracted. Finally, clear pulses are applied to the clear contacts to empty the internal gates. On the right of fig. 2 a photograph of a DEPFET-Matrix hybrid assembly used for imaging is shown.

3 DEPFET application fields

The advantages of spatially resolved, low noise, room temperature operation and the possibility of backside illumination with a thin entrance window make DEPFET a pioneering device for many applications. Three examples are the following systems:

- For biomedical applications DEPFET pixel matrices can be used in autoradiography to image radioactively labeled tissue, even if Tritium is used as marker. A detection system with 64×64 pixels has been successfully operated [6–9].

- In high-resolution X-ray astronomy [13, 14] DEPFET pixels possess several advantageous properties compared to fully depleted pn-CCDs [12] such as a large ratio of integration time to read out time and the

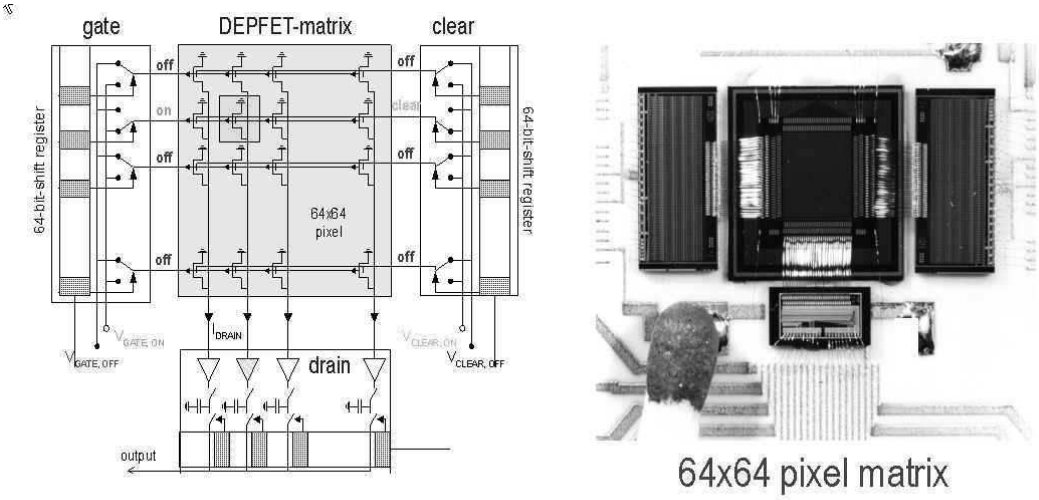

Figure 2: Principle of operation (left) and photograph (right) of a DEPFET pixel matrix showing two steering ICs for gate and clear control, respectively, as well as the current amplification stage at the bottom.

avoidance of ghost hits rendering them an attractive future detection system.

- High-resolution tracking in future high energy physics experiments at high rates such as the future e^+e^- linear collider TESLA as discussed here.

4 The DEPFET collaboration

DEPFET pixels are currently developed in a collaboration of Bonn University (N. Wermes et al.), Mannheim University (P. Fischer et al.) and the Halbleiterlabor at MPI Munich (G. Lutz, L. Strüder et al.). For TESLA emphasis is given to increase the readout speed in order to cope with the high rate requirements at TESLA, minimize and optimize the DEPFET pixel cell size to $\sim 20-30\,\mu$m using MOS transistors, to thin the DEPFET structures from the backside and to minimize the power consumption.

5 Summary of the performance of DEPFET devices so far

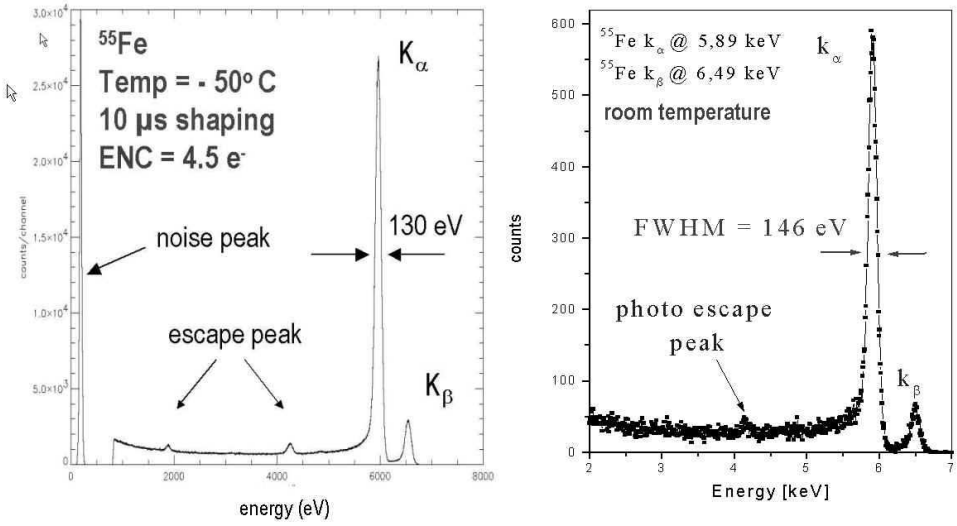

Figure 3: *(a)*^{55}*Fe-spectrum taken at -50° C, and (b) at room temperature.*

Measurements on single pixel devices have demonstrated the low noise potential of DEPFET pixels. Figure 3 shows the recorded energy spectrum obtained by the irradiation with an ^{55}Fe-source with a shaping time of 10 μs obtaines at -50°C. The K_α-line at 5.89 KeV, K_β-line at 6.49 keV and two escape peaks at ∼4.15 keV and ∼1.8 keV can be observed. The low energy tail is due to split events caused by charge sharing of one pixel with its environment. From the noise peak an equivalent noise charge of ENC=(4.5±0.1) e^- is extracted. The energy resolution (FWHM) of (130±5) eV at 6 keV as obtained from the K_α peak in figure 3 is however dominated by the Fano noise contribution of (14.2±0.3) e^-. At room temperature these values only change slightly to ENC=(4.8±0.1) e^-, and σ_E = 146±8 eV, respectively. The signal to noise ratio at 6 keV measured at room temperature is thus (96±4) [8]. In matrix operation these low noise figures have not been yet achieved. In [15] for a 64×64 matrix a noise of 114 e^- has been measured. The difference is understood and due to the matrix operation mode which requires the measurement and subtraction of signal and pedestal currents in successive turns

through the rows of the matrix. The leakage current accumulated during this time interval causes the differences in noise observed in single pixel (source follower) readout and in matrix (drain) readout and is quantitatively understood. Cooling of the DEPFET matrix by only 10° (from 45°C to 35°C) already reduces the measured noise from 114 e^- to 69 e^-

For TESLA a faster matrix operation and a shorter time difference between signal and pedestal measurements is designed leading to noise figures below 100 e^- (see below).

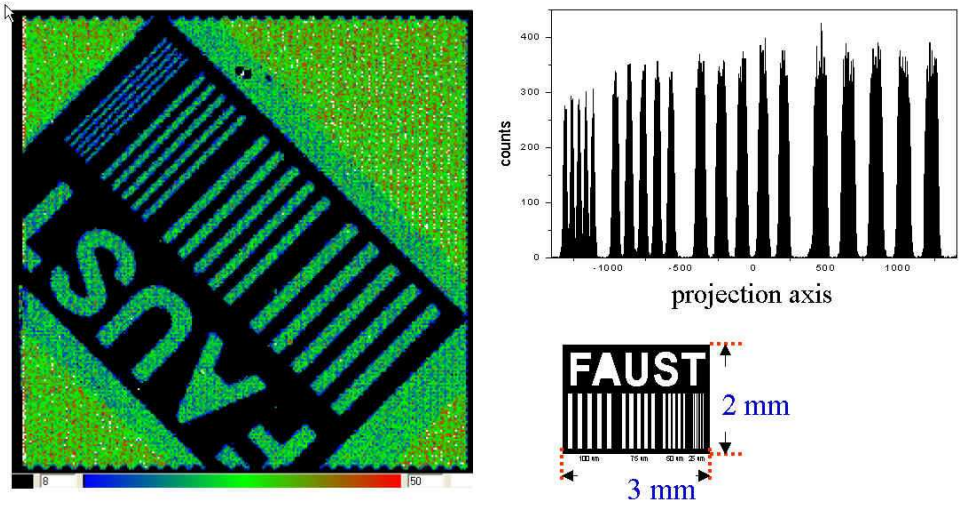

Figure 4: *(a) Space resolution test chart with different slit pitches and widths. (b) Image of the slit pattern obtained with a DEPFET matrix (from [15]).*

The homogenity and spatial resolution have been measured using a matrix of 64×64 DEPFET pixels with pixel sizes of $50\times50\,\mu m^2$. As a results of a laser scan across the whole pixel the homogenity of the charge collection has been determined to be better than 95% [8], where the deficit is mainly due to the uncertainty in the amount of the deposited charge. In order to determine the spatial resolution a tungsten Modulation Tranfer Function (MTF) test chart shown in fig. 4 with slits between 100μm and 15μm widths was placed on the backside of the detector [15]. The detector was illuminated with a ^{55}Fe-source. The function describing the intensity distribution around the

edges of the lines is given by an error function. The width of the Gaussian obtained after differentiating this distribution corresponds to

$$6.7 \pm 0.7\,\mu m \quad \text{or} \quad 37 \text{ lp/mm} \quad \text{for} \quad {}^{55}\text{Fe}\,(6\text{keV})$$
$$4.3 \pm 0.8\,\mu m \quad \text{or} \quad 57 \text{ lp/mm} \quad \text{for} \quad {}^{109}\text{Cd}\,(22\text{keV})$$

6 Design considerations for a DEPFET Pixeldetector for TESLA

The challenge of a TESLA vertex detector is to develop the successfully demonstrated principle of the slow (50 kHz) DEPFET BIOSCOPE imaging system towards a fast (50 MHz) system suited for TESLA.

6.1 General layout

The proposed geometrical layout of the detector follows the one given in the TESLA TDR [1] for the CCD detector option and is summarized in table 1. Five layers of DEPFET pixel sensors with a size of $25\times25\,\mu\text{m}^2$ are considered. The aim is to reach a total readout time of $50\,\mu$s or better for layer 1 and $250\,\mu$s for layers 2 to 5.

Layer	Radius	Ladder L× W	Nr. of Pixels	Nr. of Ladders	Clock rate / read out time	Nr. of Hits
	mm	mm^2	MPix	r-ϕ/z	MHz / μs	/BX/mm^2
1	15	100 × 13	2.1	8/1	40/50	4.3
2	26	125 × 22	4.4	8/2	20 /250	2.4
3	37	125 × 22	4.4	12/2	20/250	0.6
4	48	125 × 22	4.4	16/2	20/250	0.1
5	60	125 × 22	4.4	20/2	20/250	0.1

Table 1: *Key parameters of the vertex detector design (from [1]).*

An example of a ladder in layer 1, which is the most critical one concerning occupancy and readout speed, is shown in figure 5 (left).

Each of the ladders in layer 1 is subdivided in 4000 rows × 520 columns. The sensor area of each ladder is thinned to $50\,\mu$m or less. It is surrounded

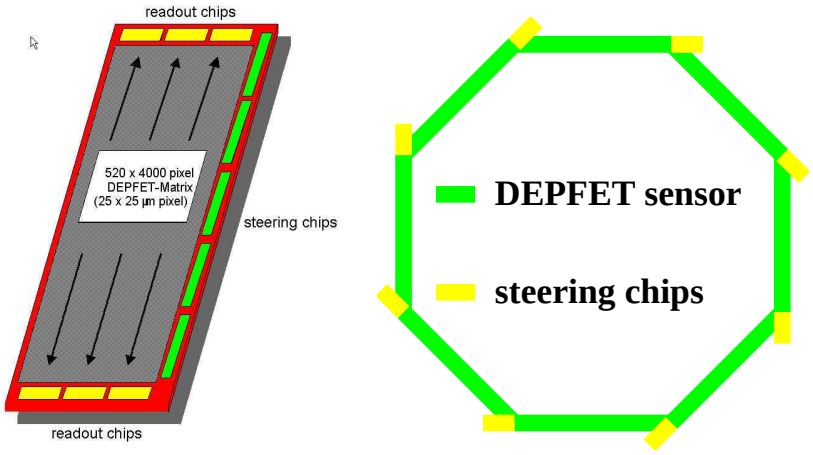

Figure 5: *Concept of a pixel detector ladder with 500×4000 DEPFET pixels. Steering and readout chips are placed at the sides and ends of the sensor area, respectively (left). $r-\phi$ view of the eight sensor ladders of the innermost layer (right).*

by a thicker (200 μm - 300 μm) silicon frame for mechanical stabilization (see below). In order to provide the appropriate driving voltages for the gate rows steering chips are placed at one ladder side of the frame area. Readout chips are attached at both ladder ends for the innermost layer, where only one sensor ladder extends along the z-direction, and at the outwards pointing edges of the ladders in layer 2 to 5, where two sensor ladders extend along the z-direction. In order to reach a very low radiation length in the detector area all electronic chips are also thinned down to $\sim 50\,\mu$m. The arrangement of the eight ladders with their steering chips in the innermost layer in the r-ϕ view is shown in figure 5 (right). The depicted design ensures that there are no insensitive regions in ϕ.

6.2 Readout scheme: from the present to TESLA

In figure 6 an array of DEPFET pixels is schematically shown. The gate and clear contacts of the pixels are connected to each other row-wise by aluminium traces. They are connected by wire bonds at the edges of the sensor matrix to the steering chips. The drains of the transistors are connected

column-wise and can be contacted at the bottom and/or top of the matrix to the readout chip.

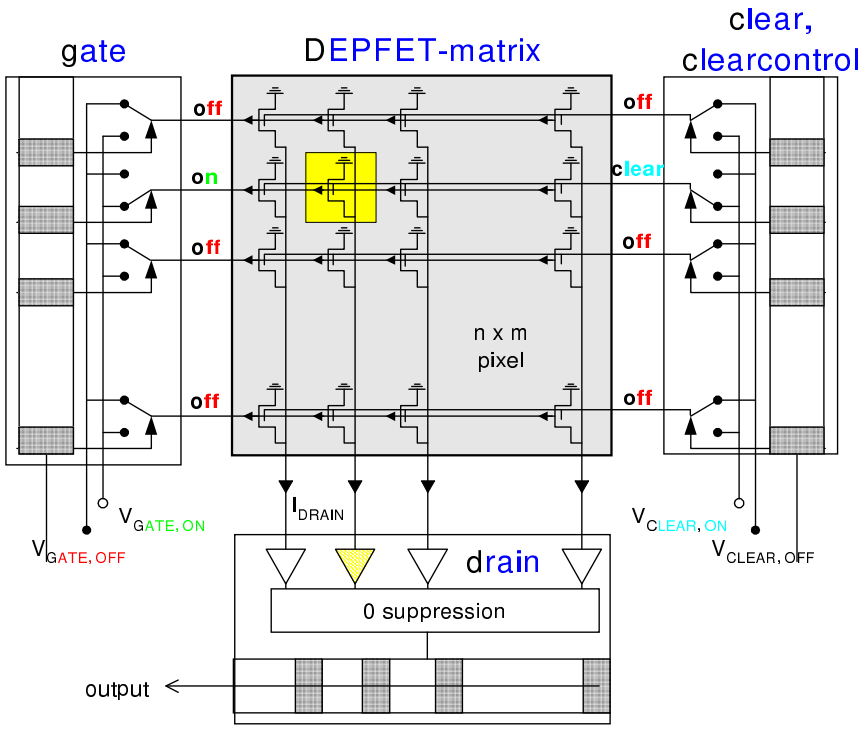

Figure 6: *Principle of operation of a full DEPFET pixel array (schematic only). In the proposed design the steering electronics for gate and clear contacts will be implemented on one chip placed at one side of the sensor area.*

The pixels are read out row-wise by applying a voltage to the external gates of the DEPFETs. At the bottom of each column the current is transferred to one channel of the readout chip. This allows random access to the individual pixels in the matrix. For layer 1 with only one ladder in z direction half of the rows will be read out at the upper and half of them at the lower end of the sensor area (see figure 7 top). For layers 2 to 5 with two ladders in z direction one will be read out at the bottom and one ladder at the top.

At present in the BIOSCOPE application the line rate is 50 kHz, the time for one frame of 64×64 pixels is 1ms. The expected pixel occupancy at TESLA would be 20%, if only one frame is read out during the crossing of a

bunch train. In order to reduce this high number to ∼1% 20 frame readout cycles must be achieved during on train crossing. This requires a row rate of 50 MHz and a 20 kHz frame (500×4000 pixels) rate.

The concept of the steering chips used in the above mentioned BIOSCOPE-system is in general also suitable for TESLA [16]. The readout chip must be adapted to the more challenging demands of the high speed operation at TESLA. We propose and have already tested a *current based readout scheme* for this purpose, since DEPFET pixels provide current signals rather than a charge signals. Further on-chip processing of the signal, i.e. temporary signal storage, pedestal subtraction, discrimination and hit fining, is thus based on a current-mode operation and is very fast.

A full readout cycle of one row of the matrix can be described as follows.

1. The signal currents of the row of pixels are buffered in the readout chip for the later hit recognition.

2. The row of pixels is reset by applying a short pulse to the clear contacts of this row.

3. The pedestal current is read from the same row and also transferred to the readout chip.

Hit detection (zero suppression) is performed in complete analog operation by comparing signal and pedestal currents on the fly i.e. in the readout chip itself. An on-chip ADC is used at the end of the chain to digitize only those hits which were found by the hit scanner. Due to the immense data reduction one ADC operating at about 50 MHz is sufficient for each readout chip which influences positively the power consumption of the readout electronic as well as the achievable ADC resolution. All hits collected during one bunch train are stored in a RAM and transferred to further components of the readout chain during the relatively long time between bunch trains (200 ms). The expected performance of the readout chip is matched to the noise performance of the DEPFET-sensor (<100e) and a position resolution well below the pixel size should be possible. Furthermore, on-chip double correlated sampling (two relative measurements within several 10ns) can reduce the 1/f noise of the system. In order to fulfill the radiation demands for the operation at TESLA (100 krad for 5 years from pair-produced electron pairs and 10^9 1 MeV-equivalent neutrons/(cm^2 year) [1]) the chips are fabricated in submicron technology using radiation hard design rules and annular

transistor structures as used for the LHC experiments [21]. The proposed scenario allows recognition of hits, zero suppression and digitization on the readout chip and will therefore minimize the data volume transferred to the following members of the readout chain.

6.3 Power consumption

One of the main assets of the DEPFET concept we believe is the potential of low power operation, in particular of the DEPFET sensor in the active area of the detector which to actively cool will be difficult. The readout and steering chips, situated at the boarder of the modules, can be cooled more easily.

The power consumption of the sensor has been estimated assuming V_{Drain}= 5 V and I_{drain}=100μA corresponding to 500 μW per active DEPFET. A further reduction of this value per active pixel is foreseen during the ongoing R&D program. The number of pixels in layer one active at the same time is 8320 located in 16 rows (2 on each of the 8 ladders) with 520 pixels each. The peak power consumption is thus 4.16 W. However the bunch structure at TESLA with a duty cycle of $\approx 1/200$ gives an average power consumption of only 0.021 W for layer one. In layers two to five 112 rows with 880 pixels each are active at the same time. This corresponds to a peak power consumption of 55 W and an average power consumption of 0.32 W for the whole DEPFET sensor area.

This calculation does not take into account any dissipative effects during switching on and off the DEPFET pixels. But due to the fact that only a single row of pixels per matrix is selected at the same time these effects are expected to be negligible. Furthermore the system achieves a sufficient noise performance at room temperature and will need no extra cooling.

In order to meet the performance goal of 50μs readout time per frame in layer 1 the above described three steps of reading signal current, clearing of the internal gate and determining the pedestal current need to be performed in 20 ns, which seems to be a quite ambitious goal, which is, however, well in reach (see below). In order to decrease the readout time for the whole detector two further options have been considered:

- The number of readout chips at each of the ladder may be doubled (see figure 7 bottom), such that for layer 1 only a quarter of rows of each ladder (only half of the rows in layers 2 to 5) will be readout by a single

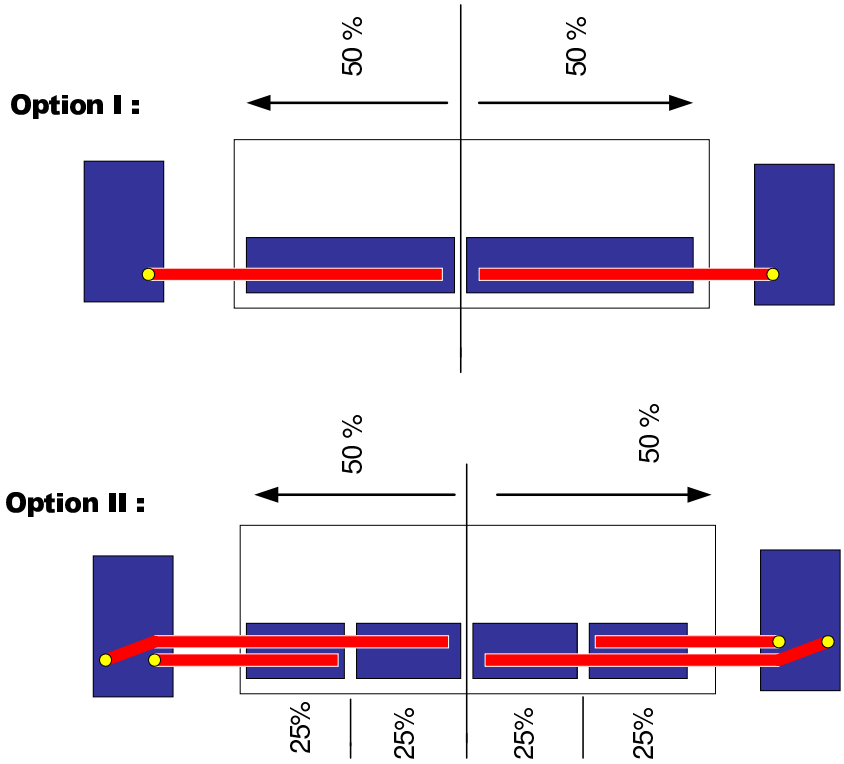

Figure 7: *Read out principle for layer one. Option 1 (top): the two halfs of the ladder are read out in parallel at each side. Option 2 (bottom): the ladder is devided in four parts for the readout. Two quarters are read out at each side.*

readout chip. This allows to reduce the readout time by a factor of ∼2 at the cost of doubling the power consumption assuming the same clock rate.

- As there are steering and readout chips placed at the ladder end as well as at one ladder side (see fig. 7) a modified arrangement is possible where the location of steering and readout chips are exchanged and the ladder is readout in the direction perpendicular to the one proposed here so far. This would improve the readout speed by a factor of 3.8 for layer 1 but will increase the power consumption of the whole system and especially the heating in the sensor area itself. Both strategies have

to be balanced to find the most advantageous concept for TESLA.

7 R&D and Prototyping Achievements to date

The R&D work carried out by the collaboration has concentrated on the following areas which are critical for a TESLA vertex detector

- development of third generation DEPFET sensors suited for TESLA including thinning
- development of a fast readout scheme suited for operation at TESLA

7.1 Development of new DEPFET sensors

The DEPFET sensors are manufactured, as other silicon detectors for particle physics, in the silicon detector production line of the MPI/MPG semiconductor laboratory in Munich. Following the encouraging results with DEPFET structures and smaller DEPFET pixel prototype matrices we have concentrated on the requirements for full size detectors for TESLA and XEUS. This change has consequences not only for the design. It requires also the extension of the technological capabilities of the semiconductor laboratory. There are several reasons for this extension of the silicon technology:

1. The required small size of individual pixels forced the change from closed transistor geometries to linear structures. This in turn leads to the need of self aligned geometries which was possible only with two layers of polysilicon.

2. The wiring of large size matrices in two orthogonal directions leads to the need of two conducting metal layers separated by an insulation layer. While the first of these extensions has already successfully been accomplished, equipment for the second task is still to be delivered in the middle of this year. In the following the present status of the development will be described. It concentrates on two main aspects: a) The DEPFET sensor with its requirements of large granularity and high readout speed and b) The development of a technology for producing thin ($< 50\mu$m) detectors. While the first development is initially done on thick (450μm) wafers, thinning has been initially studied on simple

diode structures. Both of these developments will be combined in a second stage.

7.1.1 DEPFET sensor: design and technology

As mentioned previously already, the DEPFET device concept was up to now evaluated mainly on circularly shaped JFETs[2]. However, a position resolution in the range of 5μm as needed for vertexing at TESLA requires pixel cell sizes of about $25 \times 25\mu\text{m}^2$. This is impossible to achieve with JFETs at the presently given minimum technological feature sizes of 2μm to 3μm. Linear structures are inherently smaller than circular ones but the fabrication of linear JFETs is very complicated due to the problem of lateral channel isolation. Another intrinsic difficulty of JFET technologies is the pinch off voltage variation over the wafer, within fabrication batches and from batch to batch. Therefore we have for this project switched to the use of MOS devices. In principle MOSFETs can be produced in any shape, linear as well as circular. In terms of reliability and homogeneity they are suitable for large area devices and have a much higher geometrical scaling potential than JFETs. Figure 8 shows the layout of a unit cell containing two pixels with a common clear structure (N^+ green) a common source (center P^+) and two drain contacts (top and bottom P^+). Channel and clear contact are separated by the clear gate (Poly 1) that simultaneously provides self alignment between internal and external gate. Repeating the structure in two dimensions one obtains a pixel detector in which gates and clear contacts are running row like and drains are connected column wise while the sources of the complete matrix are all connected with each other in a net-like fashion. One row addresses always a pair of pixels with the drains connected to two separate column like output busses. Row like busses are laid out in metal 1, column like busses in metal 2. The introduction of the second metal layer was mandatory to fabricate low impedance connections in large matrices in order to allow high speed operation of the devices. This technology has already been developed at the MPI semiconductor laboratory. Meanwhile the first prototype production run is well on the way. A variety of pixel matrices have been implemented, part of them needing only one metallization layer. These, although having larger pixel sizes and worse conduction prop-

[2]'Circularly shaped' means a closed transistor where the drain surrounds the source region or vice versa, in contrast to linearly shaped transistors having a lateral confinement of the channel by an isolation structure.

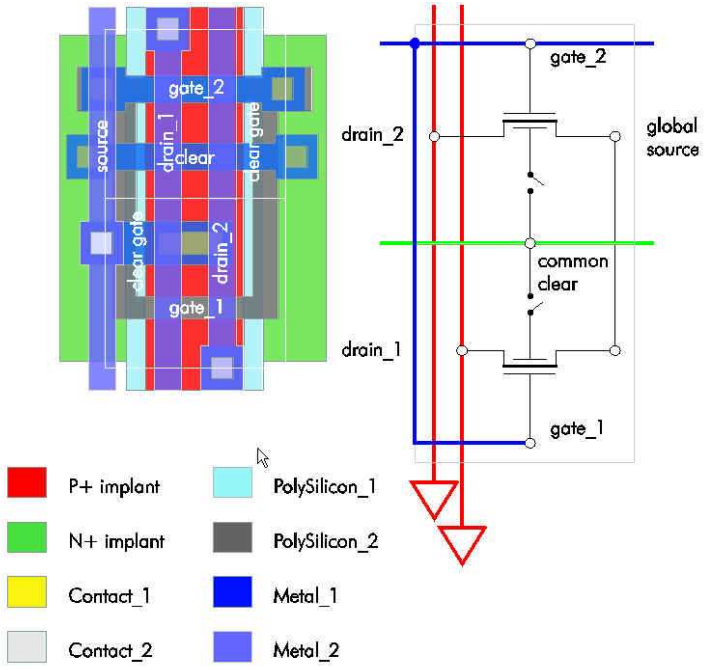

Figure 8: *Layout example (left) and equivalent circuitry diagram (right) for a linear double pixel cell. Each white rectangle surrounds a DEPMOS.*

erties, will be ready for testing in early summer of this year. They will be extremely valuable in showing the principal properties and for getting the readout electronics operating properly.

In designing these devices several partially conflicting requirements had to be met:

- The internal gate has to be fully cleared by applying a positive pulse onto the N^+ doped clear contacts. (This means that no charge is left over after clearing.)
- Nevertheless it has to be assured that during all other times the clear contact is hidden and all signal charge reaches the internal gate.
- The internal gate (formed by a buried n-type implant) is aligned with the transistor channel.

- The device must be free of potential pockets capable of attracting signal charges on their way towards the internal gate

All of these (and some additional) requirements have been met and verified by extended device simulations, some of which will be shown in the next section.

7.1.2 Device simulations

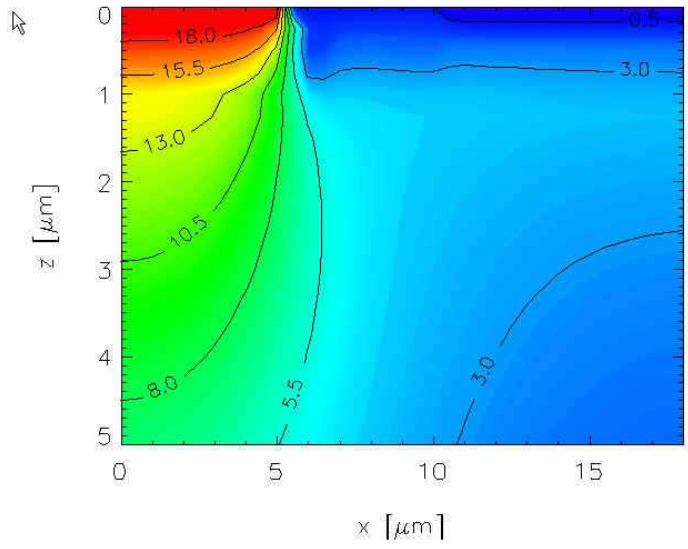

Figure 9: *Potential distribution during the clear operation simulated with the 3D-Poisson solver Poseidon [18] (V_{Clear} = 20V, V_{Back} = -30V, V_{Source} = 0V, V_{Drain} = -5V, V_{Gate} = -3V, $V_{Clear-Gate}$ = 1V).*

Two and three dimensional simulation tools were used to optimize the layout and the technology parameters. Figure 9 shows the simulated potential distribution during the clear operation. The simulation illustrates that the electrons can flow unopposed from the internal gate (right side at 1μm depth) into the clear contact (left side on top). The applied clear voltage of 20V can be reduced by lowering the potential barrier in the clear gate region. During charge collection the transistor is switched off and the potential of the internal gate can be adjusted by the voltage of the external gate. Figure

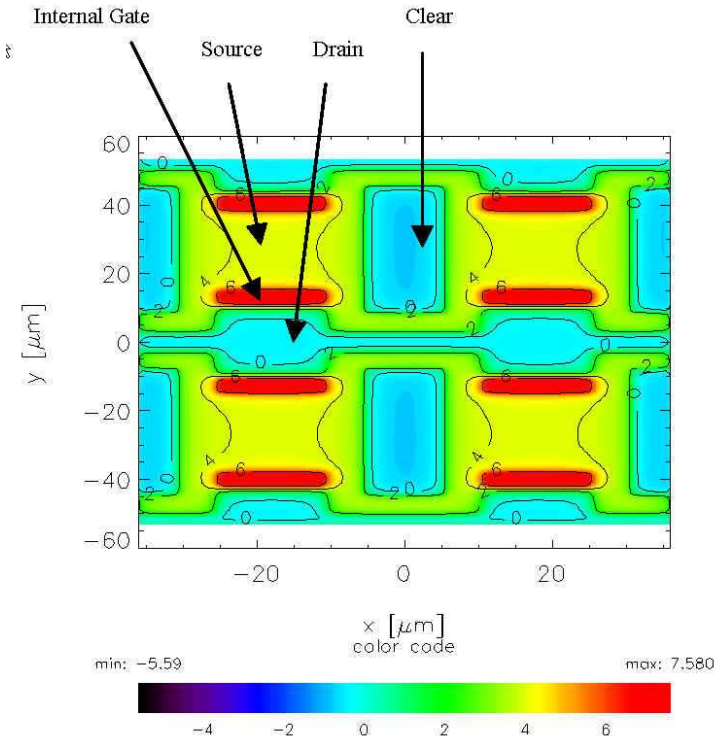

Figure 10: Potential distribution of a 2x4 array section parallel to the surface at a depth of z=1m during charge collection simulated with Poseidon (V_{Clear} = 3V, V_{Back} = -25V, V_{Source} = 0V, V_{Drain} = -5V, V_{Gate} = 2V, $V_{Clear-Gate}$ = 1V). A single cell is marked by the dashed line.

10 demonstrates that there are no potential pockets attracting electrons. It shows the potential at a depth of 1μm seen by drifting electrons generated in the bulk. Note the result of the negative space charge of a deep boron doping implanted beneath the clear region. By switching on the external gate the device current is read out. The drain current response to a given signal charge defines the amplification of the internal gate $g_q = dI_D/dq$. To analyze the signal response of the DEPFET 1600 electron-hole pairs were introduced by a locally and temporally limited increase of the Shockley-Read-Hall generation rate using the two dimensional device simulator TeSCA.

Figures 11 and 12 show simulations of the DEPFET in its on-state as is the case during readout. Only the uppermost 20μm of the device is shown

displaying the result of a two dimensional device simulation along the channel direction from source to drain. The gate length is 5μm, the internal gate in which the signal electrons are collected assumes a positive potential of 3V.

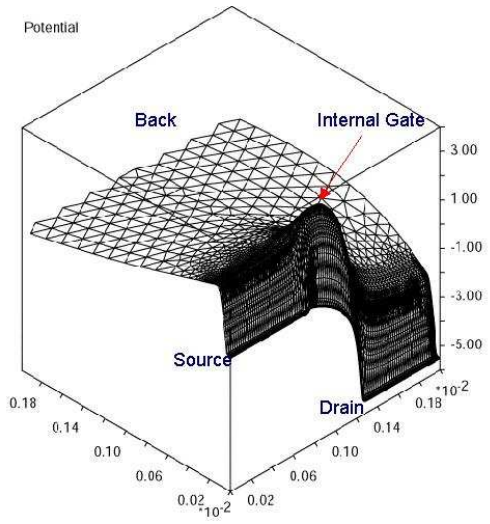

Figure 11: *2-D Simulation along the channel of a DEPFET during readout (ID=100μm, V_D=-5V): the potential up to a depth of 20μm is shown. The internal gate is at a potential of +3V.*

The simulated signal response shown in fig. 12 demonstrates the possibility of an amplification of more than 1nA per electron collected in the internal gate for optimized TESLA DEPFET structures. In this simulation the DEPFET was permanently turned on - contrary to operation within the final detector where the transistor is only turned on during short intervals before and after clearing. The nevertheless rapid risetime reflects the charge collection process.

7.1.3 Pixel detector fabrication

The detectors are produced using the 150mm (6") double sided processing line available at the MPI semiconductor laboratory in Munich. An impression of the structures contained in the first production is given in the layout drawing shown in fig. 13. The wafer contains a variety of small size pixel

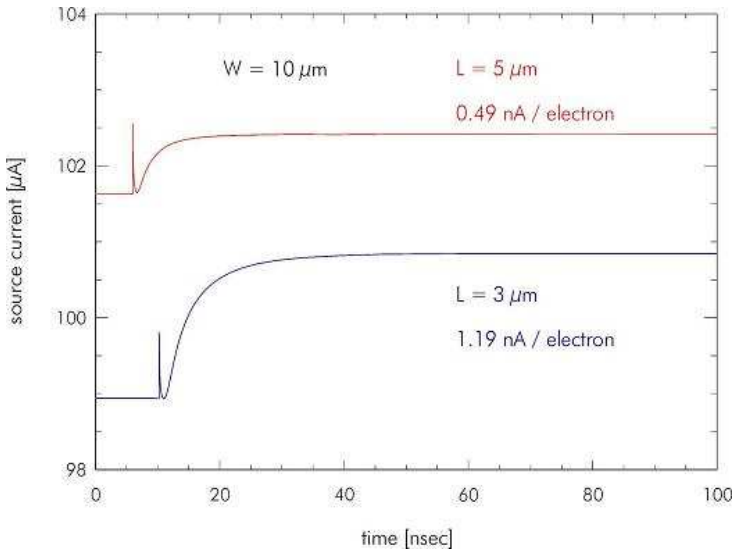

Figure 12: *Simulated signal response to a signal charge generation of 1600 electron-hole pairs.*

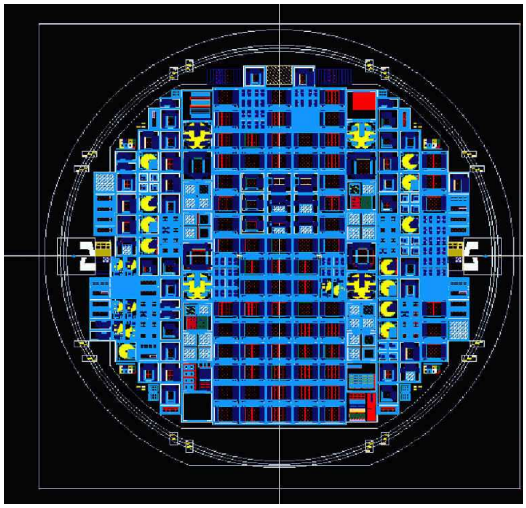

Figure 13: *Wafer layout with DEPFETpixel detector prototypes for the TESLA and XEUS projects and a variety of test structures presently in production at the MPI semiconductor detector laboratory.*

devices with circular and linear geometries and up to 128x128 pixels, single pixel cells and a variety of special test structures. The smallest pixel size is

XEUS		TESLA
imaging spectroscopy	**purpose**	particle tracking
7.68 x 7.68 cm² 1024 x 1024 pixels 1 Mpix	**detector format**	1.3 x 10 cm² (x 8) 520 x 4000 pixels (x 8) 2.1 Mpix (x120)=2.5 x 10^8
75 µm	**pixel size**	25 µm
300 ... 500 µm	**sensor thickness**	50 µm
4 el. ENC	**noise**	~ 50 el. ENC
1.2 msec 2.5 µsec	**readout time ... per detector ... per row**	50 µsec 20 nsec

Figure 14: *The requirements on DEPFET pixels for TESLA and the X-ray astronomy project XEUS in comparison.*

30x30 μm^2. Devices have been designed both in view of TESLA and with the aim of equipping the focal detector of the future European XEUS X-ray observatory. The different requirements of these two projects are shown in table 14. Part of the structures are already working using only the first metallization layer so that a couple of wafers will be produced only up to this point in order to have structures available in relatively short time (May 2003). The rest is expected to be finished after installation of equipment and commissioning the processes for the second metal layer. At present the production is done up to the first metallization. Fig 7 shows a detail photograph out of one pixel detector. Clearly visible are the structures in the two polysilicon layers (yellow) and the contact holes for later metal connections.

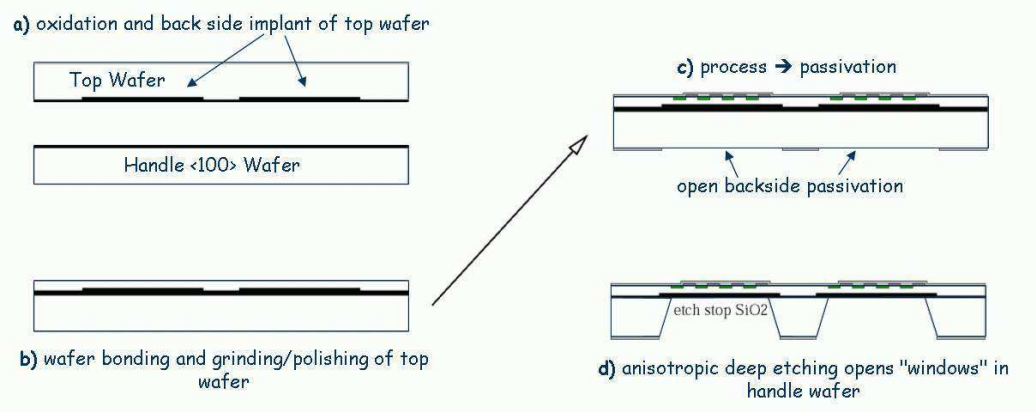

Figure 15: Joint process sequence of wafer thinning and DEPFET production.

7.1.4 Wafer thinning technology

Production of double sided detectors - as needed for DEPFETs - on thin (50μm) wafers is not possible in normal technology. For that reason a new processing scheme is under development in collaboration with the MPI für Mikrostrukturphysik in Halle. It makes use of the technique of wafer bonding. It leads to a thin structure which is stiffened by a frame of thicker silicon with the detector also sensitive below these thicker regions. The processing sequence is explained in fig. 15. One starts with two thick wafers. Fig. 15(a): the top (detector) wafer has already processed diodes on its lower side, the bottom wafer is only oxidized and serves only for mechanical support. Fig. 15(b): the two wafers have been bonded and the top wafer has been ground and polished to 50μm thickness while being supported by the carrier. Fig. 15(c): The top side of the two-wafer assembly has been completely processed and the backside oxide patterned to prepare for anisotropic etching of the silicon. Fig. 15(d): backside etching stops at the oxide layer located at the interface between the two wafers. This oxide can be removed by a further etching step.

Wafer thinning was first tried without detector processing. A photo of the first samples is presented in fig. 16. Their size corresponds to that foreseen for modules in the TESLA vertex detector. Further tests with processed diodes are under way.

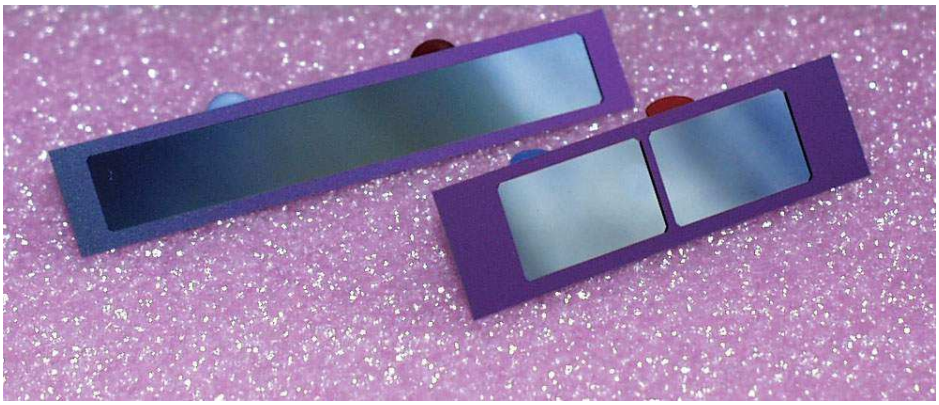

Figure 16: First results of the thinning technology development - mechanical samples. The size of the upper part is 800x104mm. A 300 μm thick silicon substrate which is thinned down to a thickness of 50 μm in the central area.

7.2 Readout Scheme Prototyping for TESLA

The readout scheme for TESLA is shown in fig. 17. A cascode stage at the input of the readout chip keeps the drain line at a constant potential so that the DEPFET current does not have to charge the relatively large bus capacitance. A row is selected for readout after the charge accumulation interval. The selected DEPFET transistors output a signal current superimposed to a pedestal current. This current $I_{ped} + I_{sig}$ is recorded in a current memory cell per column in the readout chip. After a reset of the row (assuming a perfect clearing of the internal gate) only the pedestal current I_{ped} remains in the DEPFETs. The signal part is therefore obtained by simply summing the current provided be the DEPFET after the reset and the output of the current memory cell (which is the inverse of the value written). The signal current $-I_{sig}$ is then stored in an analog FIFO made up of several current memory cells. A fast current comparison with a programmable hit threshold simultaneously generates a digital hit pattern which is recorded in an additional, digital FIFO. Analog FIFO cells with no hits can be switched off to save power. While the FIFOs are filled with events containing at least one hit, a fast scanner searches for hits in the digital FIFO. The corresponding analog values are selected with a multiplexer and fed to one or several ADCs. The digitized amplitude, the column address and further information like a time stamp and status bits are buffered in a data RAM before they are read

out.

The design goal is a ro rate of 50 MHz. This requires fast settling times for the current memory cells and a fast hit finder. These crucial elements have therefore been designed, submitted and tested with a readout test chip containing all essential elements of the readout scheme [17]. The chip was fabricated in $0.25\mu m$ technology and is shown in fig. 19a. Enclosed NMOS devices have been used to ensure radiation tolerance [21]. It is not yet clear whether the high radiation tolerance obtained by this technique is really required for TESLA. Standard layout techniques would simplify the design because the use of the fairly large annular NMOS transistors with their relatively large capacitances makes it more difficult to obtain a high operation speed. We nevertheless have chosen a radhard design already at this stage. Two building blocks are crucial for this readout concept:

- *The switched current memory cell* is the most challenging part of the readout architecture and is shown schematically in fig. 18. It provides a fast and precise buffering of the DEPFET-current for pedestal subtraction and the storage in the analog FIFO. The basic principle [19] can be divided into three phases (note that C_G is the gate capacitance of the transistor M1):

  1. S1 and S2 are closed, S3 open. The gate capacitance of the transistor M1 is charged until the device provides the combined input and bias current ($I_{M1} = I_{in} + I_B$).
  2. S2 is opened. The gate voltage and therefore the transistor current ideally remain unchanged.
  3. Immediately after sampling S1 is opened and S3 closed. As the current through M1 is still $I_{M1} = I_{in} + I_B$, I_{in} must be delivered by the output node.

  Thus in the ideal case $I_{out} = -I_{in}$. However, this simple circuit suffers from several non-ideal effects like charge-injection of the sampling switch S2 and the limited output conductance of the transistor M1 and the biasing current source. Therefore in the real case $I_{out} = -I_{in} + \delta I$ where δI indicates the error made by the sampling process. A lot of techniques to cope with these deficiencies have been treated in literature [20]. In this design cascode techniques have been used for the

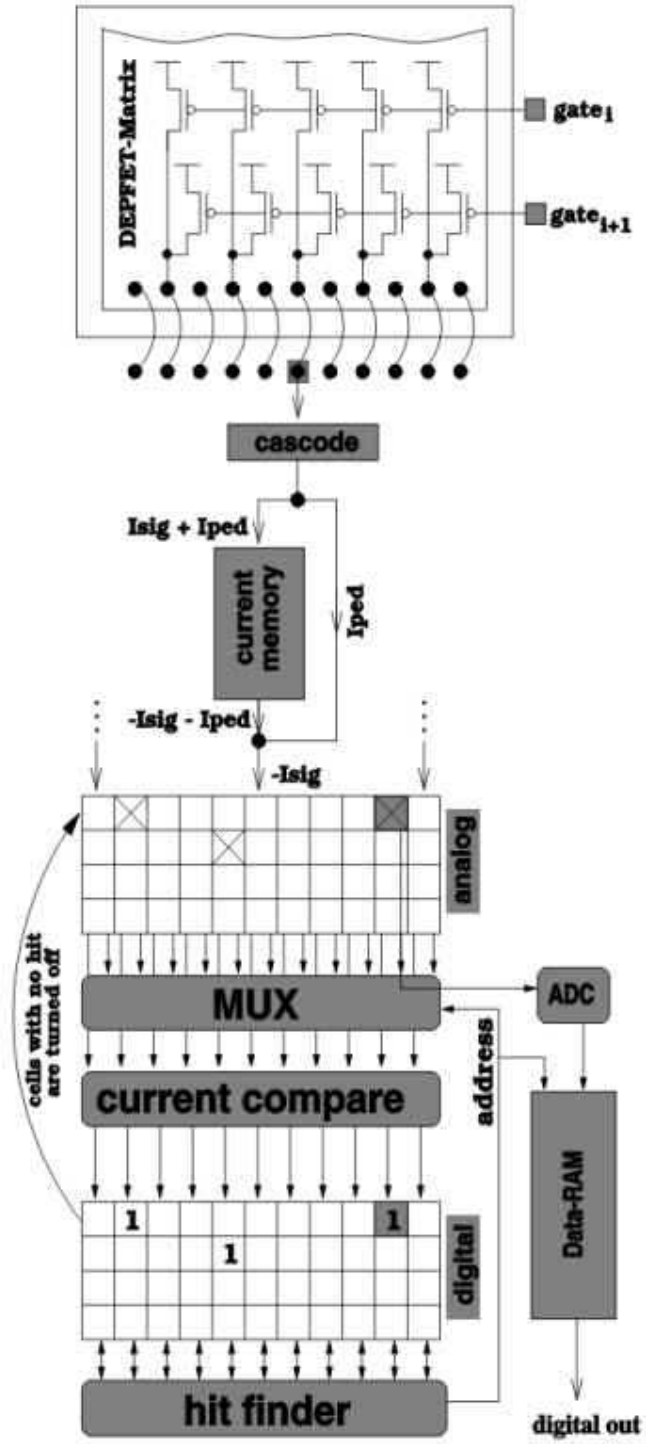

Figure 17: Readout scheme for DEPFET pixel matrices at TESLA.

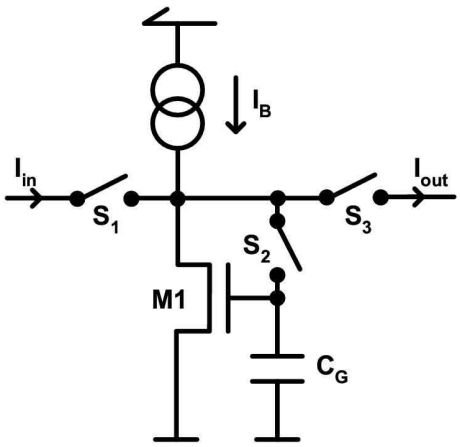

Figure 18: Principle of the current memory cell

sampling transistor and the current source to decrease the output conductance. The actually implemented circuitry uses a two stage design to cancel charge injection and to achieve a high dynamic range with a small storage error. Measurements on the test chip at a 25MHz sampling rate (limited by the test setup) show a differential non-linearity of 0.1% within a sufficient dynamic range. The total standing current in the memory cell operated at a supply voltage of 2.5V is $150\mu A$ so that for the input stage the calculated power consumption is $2mW$ per channel/DEPFET column. The cell occupies an area of $25 \times 50\mu m^2$. The same type of cell is used for the current subtraction at the input and for the storage of the hit amplitudes in the analog FIFO.

- *The hit finder* uses a binary tree structure as first proposed in [22] to find two hits out of a pattern of 128 digital inputs within one clock cycle. Measurements on the hit finder circuitry implemented on the test chip confirm that a speed of 50MHz is easily achievable in the chosen technology.

The second chip (SWITCHER) required for matrix operation generates the steering signals for the gate and clear rows. In order to provide a wide voltage range for testing of the first matrices, a special 'high voltage' $0.8\mu m$ technology has been chosen for this first version which, however, contains already the full functionality. The chip (photo in fig. 19b) contains 64 channels

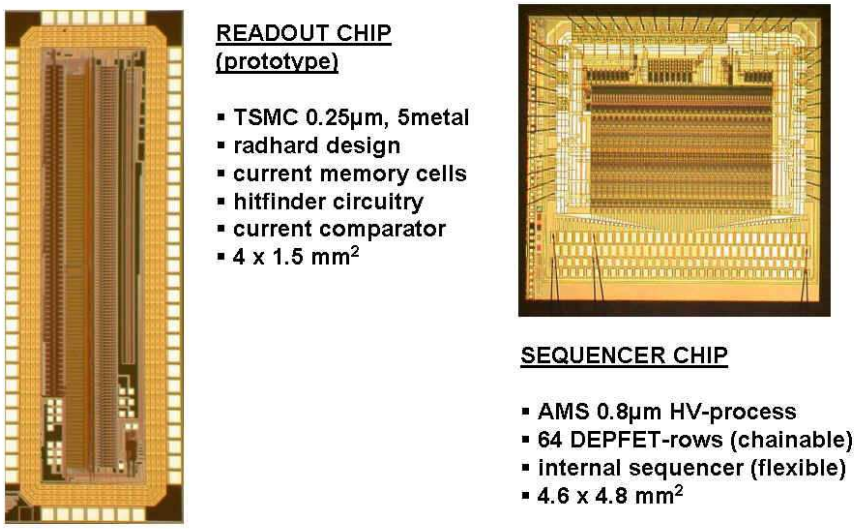

Figure 19: (a) Readout chip prototype containing the main building blocks of a readout chip for TESLA (current memory, hit finder, comparator), and (b) sequencer chip for TESLA and XEUS

with analog multiplexers, a digital sequencer and control logic. It is designed to be suited for of all fabricated DEPFET matrices for the different applications including 50MHz operation at TESLA. Several chips can be daisy chained to control larger arrays. Measurements on the fabricated prototype chip show that it is fully functional at the desired speed.

8 Further Planning

The first step in the DEPFET-R&D-Program for TESLA is to build a prototype system employing a 64×128 DEPFET-Matrix with pixels of size $30\,\mu$m $\times$ $30\,\mu$m and a thickness of $300\,\mu$m) driven by one steering and one readout chip. The chips will be realized in such a way that a system with larger sensor area can be obtained by adding more chips.

A chip containing the crucial building blocks of the readout and a full steering chip have been designed and submitted for production. The fab-

ricated prototypes are presently being tested. A first readout chip suitable for matrix readout is being designed and will be submitted by the middle of 2003. The production of DEPFET sensors for TESLA has been started. First wafers are expected by the middle of 2003.

The next goals are to aim for a stable operation of the described prototype device with efficient clearing of the matrix and a as high readout speed as possible for the three readout steps. Other R&D issues which will be addressed are the thinning of sensor and readout chips and the shortening of the clearing period.

9 Conclusions

The DEPFET technology seems to be a viable and promising alternative to the so-far discussed technologies for the TESLA pixel vertex detector. The DEPFET pixel concept is based on the in-pixel-amplification of a charge signal offering very low noise operation at room temperature ($4.9\,e^-$ for a single pixel device) anticipating an excellent signal-to-noise ratio. Power is consumed only during readout and for the proposed design the average consumption is well below 1 W for the whole pixel detector, due to the fact that only a small number of pixels rows are active at the same time. Both facts reduce and simplify significantly the cooling system.

The readout scheme allows random access of the individual pixels avoiding the reconstruction of hits at a wrong location. The aim is to reach high speed operation with a readout time of $50\,\mu$s for layer 1. Several options of how this can be achieved are envisaged.

The proposed pixel sizes are $25\times25\,\mu m^2$. Sensor and electronics will be thinned down to a thickness of $50\,\mu$m corresponding to a material budget of less than 0.1 % of a radiation length per layer.

DEPFET pixel matrices have already been built and operated successfully for other applications such as biomedical imaging. A prototype system addressing the specific requirements of TESLA is being developed in the next years.

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