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Project: CMOS sensor based Vertex Detector for the ILC
Status Report

Developement of a High Precision and Swift Vertex Detector based on CMOS Sensors for the International Linear Collider

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Abstract

CMOS sensors are being developed to equip a vertex detector offering the perfomances required for the physics programme at the International Linear Collider. The progress realised from Spring 2003 to Spring 2005 is exposed in this report. It addresses the exploration of new fabrication processes, the design of fast integrated signal processing micro-circuits, the assessment and improvement of the radiation tolerance, the reduction of the power dissipation, the thinning of the sensors, the design of a light mechanical support and cooling studies.

Progresses were also achieved on a detector design exploiting the features of CMOS sensors. Since several performance requirements are dictated by the beamstrahlung electron rate, the latter was revisited and assessed with improved accuracy. The constraints coming out from this study are significantly more stringent than those written in the TESLA TDR.

Contents (*contributors*):

1 Introduction

The physics programme of the Linear Collider requires tagging the flavour of most of the numerous jets produced in the final states of interest. This goal translates into drastic requirements for the vertex detector, well beyond the performances achieved with existing devices. CMOS sensors are particularly well suited to this framework as they are likely to provide an attractive trade-off between granularity, material budget, read-out speed, radiation tolerance and power dissipation.

CMOS sensors are manufactured in standard CMOS technology, which offers low fabrication costs and fast turn-over for their development. The key element of this novel technology is the use of an n-well/p-epi diode to collect, through thermal diffusion, the charge generated by the impinging particle in the thin (typically 5 - 15 μm) epitaxial layer underneath the read-out electronics [1].

An attractive peculiarity of the sensors is that they allow to fabricate System-on-Chips (SoC) by integrating signal processing micro-circuits (amplification, pedestal correction, digitisation, sparsification, etc.) on the detector substrate. Moreover, the latter may be thinned down to a few tens of microns since the active volume is less than 20 μm thick.

The development of CMOS sensors for charged particle tracking was pioneered in Strasbourg in 1999. The first years of the development allowed to demonstrate that this technology provides excellent detection efficiency and spatial resolution. Based on this success, a reticle size sensor (3.5 cm^2 large) exploiting the architecture of the first (a few mm^2 wide) prototypes, was fabricated. Made of 1 million pixels, it allowed to show that the performances obtained with small prototypes were indeed reproduceable with a macroscopic detector element [2].

The progress realised from Spring 2003 to Spring 2005 is summarised in this report. It addresses first the most demanding constraints on the inner most layer performances, which come from the rate of beamstrahlung electrons. This rate is being reevaluated with higher precision than previously in section 2, and new constraints on the read-out speed and the radiation tolerance are derived. The progress achieved on the design of the two read-out architectures foreseen to equip the 2 inner and 3 outer detector layers is summarised in section 3, emphasising a fast, column parallel, architecture providing low pixel noise and pixel-to-pixel dispersion. Several new measurements of the sensor radiation tolerance were performed, which are exposed in section 4. In particular, the tolerance to $\sim$ 10 MeV electrons, such as those expected from beamstrahlung, was studied for the first time. Section 5 summarises the results of the exploration of a new fabrication process, providing particularly satisfactory detection performances. Section 6 exposes new results on industrial thinning allowing for $\sim$ 50 μm thickness. The design of a vertex detector geometry exploiting best the specificity of CMOS sensors is described in section 7. It departs from the TESLA TDR baseline in several aspects. A first estimate of the expected power dissipation is derived. Section 8 gives an overview of the status of on-going cooling studies. Section 9 gives a short summary of mechanical support studies performed at LBNL for the STAR vertex detector upgrade, based on MIMOSA sensors. Section 10 provides an outlook for the two coming years. The report summary and conclusions are given in section 11.

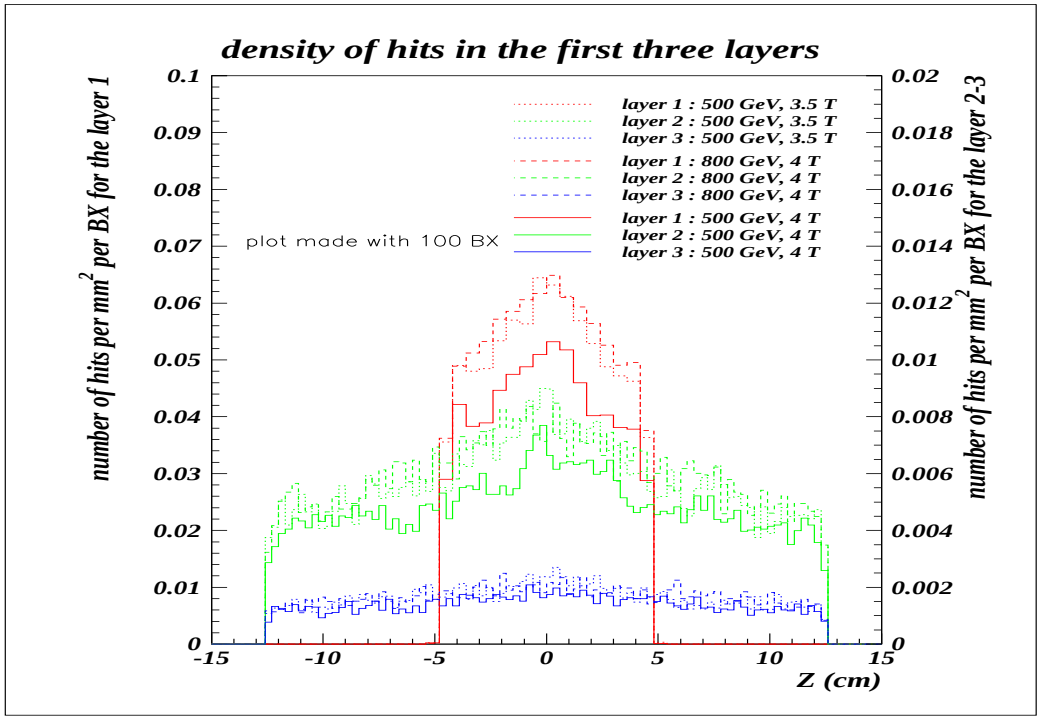


Figure 1: Distribution of beamstrahlung hits in the three inner layers of the vertex detector along the direction parallel to the beam axes. The left vertical scale applies to the inner most layer (red lines), while the right scale stands for the two other layers (green and blue lines). The rates are shown for two different values of the experimental magnetic field (4 and 3.5 T) and of the collision energy (500 and 800 GeV).

2 Improved assessment of running conditions

The knowledge of the rate of beamstrahlung electrons traversing each detector layer deserves much attention since its magnitude dictates the necessary read-out speed (due to occupancy) and dominates the radiation tolerance requirements. The electron rate was already determined for the TESLA TDR. It was however based on the simulation of a single bunch crossing (BX) only, leading to a statistical accuracy insufficient to provide enough information on the hit spatial distribution. The study was therefore repeated in order to refine the requirements on the corresponding vertex detector performances.

2.1 Estimate of the beamstrahlung rate

Improved computing power available in the last years allowed to repeat with 100 BX the GUINEA-PIG simulations performed for the TESLA TDR with 1 BX. The size of the simulated sample was large enough to access the hit distribution along the beam directions (z axis). It is shown in Fig.1 for the 3 inner layers of the detector, located at radii of 15, 26 and 37 mm.

One observes that the hit density in the inner most layer varies from about 3 hits/cm^2/BX at the acceptance edges to more than 5 hits/cm^2/BX near the vertical to the interaction point. This

sizeable difference is due to $\sim$ 10 MeV electrons produced close to 90° and traversing a large number of times ($>$ 10) the inner most layer while they spirale in the 4 T magnetic field of the apparatus.

The momenta of beamstrahlung electrons reaching the detector concentrate near 9-10 MeV/c. The hit rate decreases therefore rapidly with increasing radius: it is $\sim$ 8 times smaller in the second layer and is still $\sim$ 3 times smaller in the third layer.

The rates shown in Fig.1 are subject to uncertainties or unknowns which need to be considered when deriving constraints on the vertex detector performances. For instance, the rates increase by $\sim$ 20 % if the experimental magnetic field happens to be of 3.5 T only, or if the collider is run at a collision energy of 800 GeV instead of 500 GeV. Moreover, the very limited accuracy of the generator should be taken into account, since the electrons of concern are at the edge of the phase space and since the process generation is still to be confronted to real data (the ILC will presumably provide the first opportunity for such a comparison). It is mandatory to take this uncertainty into account in the required detector performances. A global safety factor of 3 was chosen for this purpose, to apply on the raw Monte-Carlo output. The hit density at 90° can therefore be estimated to possibly reach 15 hits/cm^2/BX. This upper limit determines the conditions in which the vertex detector should still be fully operational. The corresponding requirements on the signal processing electronics and on the radiation tolerance are discussed hereafter.

2.2 Consequences on the signal processing electronics

To evaluate how fast the signals of the inner most layers should be processed, the occupancy was first estimated for a typical read-out time of 50 μs (as mentioned in the TESLA TDR), assuming a pixel pitch of 20 μm. The upper limit on the hit occupancy comes out to be $\sim$ 0.9 % in this case. Accounting for the cluster multiplicity ($\sim$ 5-10), 4.5-9 % of the pixels would be collecting a signal charge. The example shows that the hit rate in the inner most layer calls for a read-out time still shorter than the 50 μs claimed in the TESLA TDR. The target value was therefore fixed to $\lesssim$ 25 μs, which is still not comfortable, but reflects a compromise which accounts for power dissipation, material budget and detector design considerations.

Moreover, a very valuable back-up for handling the occupancy in the inner most layer may come from the $\sim$ 8 times lower hit density in the second layer: it will consist in extrapolating the track elements reconstructed in the four - much less crowded - outer layers down to the inner most layer. In case the occupancy turns out to be very high in the latter, the hits of interest can be selected by requiring them to be associated to a track element extrapolated from the other layers. This forces however the integration time to be significantly below 100 μs in the second layer (the TESLA TDR value was 250 μs). A target value of $\sim$ 50 μs was retained for this purpose.

Since the hit density in the third layer is more than 20 times lower than in the inner most layer, a read-out time of $\lesssim$ 200 μs can be considered as appropriate. The same target value was retained for the fourth and fifth layers, where the hit density is even lower.

2.3 Consequences on the radiation tolerance

The hit rate in the inner most layer translates into an upper limit of $\sim 1.8{\cdot}10^{12}$ hits/cm^2/yr near 90°. Assuming that the sensor performances should remain essentially unchanged after 3 years of operation, the radiation tolerance requirements are based on a total electron flux of $\sim 5.4{\cdot}10^{12}$ hits/cm^2.

The ionising radiation level corresponding to this integrated flux was computed assuming that the electrons deposit in average 388 eV/μm in Si. Yearly, the energy deposit would amount to $\sim 3.0{\cdot}10^{15}$ MeV/kg, i.e. $\sim$ 50 kRad. The required radiation tolerance corresponding to three years of running amounts therefore to $\sim$ 150 kRad.

The non-ionising radiation level was estimated, assuming a NIEL factor of 30 for electrons of about 10 MeV. This value is a compromise between theoretical estimates leading to values near 20 and experimental measurements favouring factors in excess of 40. The expected fluence is therefore about $6{\cdot}10^{10}$ $n_{eq}/cm^2/yr$. In 3 years of operation, the sensors should stand $\lesssim 2{\cdot}10^{11}$ n_{eq}/cm^2. This value is significantly larger than the expected fluence induced by the neutron gas circulating inside the experimental apparatus ($\lesssim 10^{10}$ $n_{eq}/cm^2/yr$ [6]).

3 R&D on signal processing architectures

The design of the signal processing micro-circuits is strongly influenced by the need to cope with the large flux of beamstrahlung $e^{\pm}$ in the inner most layer. Since this flux decreases rapidly with increasing radius, a different architecture is envisaged for the outer layers, which takes advantage of the beam time structure. The following strategies are pursued to meet the running condition requirements: a massively parallel architecture with on-chip data sparsification adapted to the inner layers; for the outer layers, on-pixel storage for $\gtrsim 5$ snapshots during a single bunch train crossing, the signal transfer and processing being postponed to the end of the train.

The design of the second of these two architectures is much less demanding than the first one; it is however unlikely to be extendable to the inner layers because of the large number of memory-cells to integrate in each pixel ($\gtrsim 40$ in the inner most layer). Most of the chip design effort over the last two years was therefore devoted to the development of a massively parallel read-out architecture adapted to the inner layers.

3.1 Present achievements

Since 2002, three different prototypes were fabricated in order to explore various charge collection and signal treatment architectures integrated in sensors adapted to fast, massively parallel, read-out. These architectures are based on the concept of pedestal subtraction inside each pixel (via correlated double-sampling) and on grouping the pixels in short columns read out in parallel, each column being equipped with a single discriminator handling the signals coming out sequentially from all pixels of the column.

The first of this series of prototypes was MIMOSA-6 [3]. Each of its pixels was equipped with charge amplification micro-circuits and allows for correlated double sampling (CDS) operation in order to subtract the pedestal associated to the average leakage current integrated by each sensing device. The chip is organised in columns grouping 128 pixels (28 μm pitch); its read-out time is close to 25 μs. A comparator is integrated at the end of each column for discrimination purposes. Tests of the prototype showed very good noise performances at the single pixel level (i.e. ~ 15 e^- ENC during the read-out phase) as well as an acceptable dispersion of the discrimination thresholds. However, substantial additionnal noise was observed, suspected to originate from cross-talks between the digital and analog circuits inside the pixels and from the dispersion of the pixel characteristics inside each column.

The next generation of fast prototypes (i.e. MIMOSA-7 and -8) were fabricated in 2003 and 2004 respectively. Both chips were tested with a ^{55}Fe source. Particularly encouraging results were obtained with MIMOSA-8 [4] (see Fig. 2). Manufactured in TSMC-0.25 μm technology, its architecture is inspired from that of MIMOSA-6: it features in-pixel amplification and CDS, and is organised in 4 sub-arrays of 32 columns read out in parallel. Each column contains 32 pixels (25 μm pitch) and is ended with a discriminator. Three sub-arrays are based on a pixel architecture with DC-coupling to the sensing diode and explore various diode sizes (from $1.2{\times}1.2$ μm^2 to $2.4{\times}2.4$

[6] This value includes a safety factor of 10 applied to the output of the Monte-Carlo simulation.

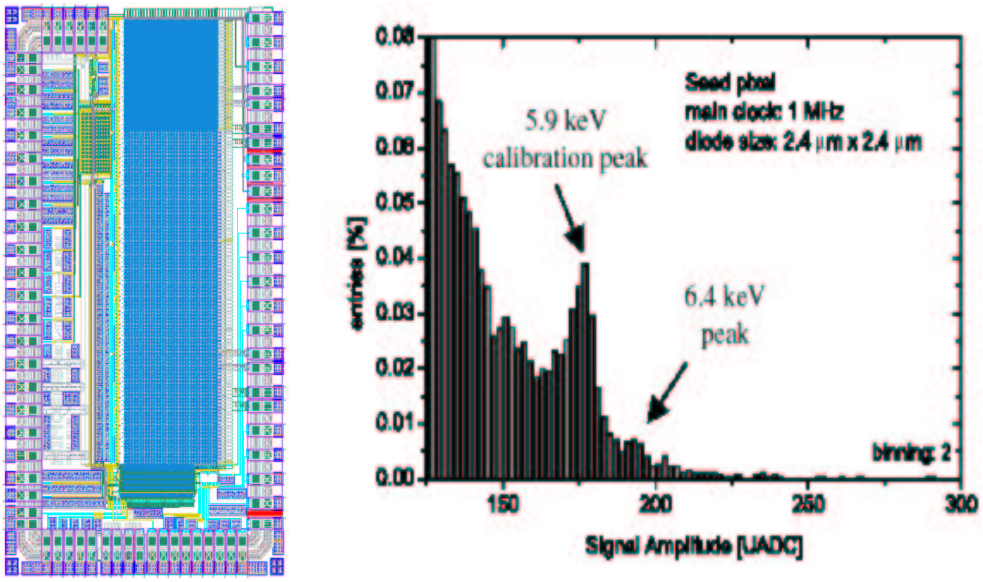


Figure 2: **Left:** layout of MIMOSA-8 showing the 32 parallel columns, out of which 24 are ended with a comparator, while the other 8 provide an analog output. **Right:** Sensor response to its illumination with an ^{55}Fe source. The peak around 180 ADC units is due to 5.9 keV X-rays impinging the sensor in the depleted volume surrounding the sensing diode, a case where the full X-ray signal charge (i.e. $\sim$ 1640 e^-) is collected by a single diode and can therefore be used for charge-to-voltage calibration purposes.

μm^2). The fourth sub-array exploits a more complicated pixel architecture (15 transistors instead of 8) with AC-coupling to the sensing diode, which allows larger charge-to-voltage conversion gain.

Tests of the chip are still under way. Preliminary results show that the noise levels are in the order of $\sim$ 13-18 e^-ENC, depending on the sub-array, and that the charge-to-voltage conversion gain is of $\sim$ 50-70 (resp. 110) $\mu V/e^-$ for the different DC-coupling (resp. AC-coupling) architectures. Moreover, the pixel-to-pixel dispersion comes out to be particularly low and matching the requirements.

The simultaneous operation of all analog and digital elements of the read-out chain remains to be tested. If successfull, a few chips may be exposed to particle beams in Autumn 2005 in order to assess their charged particle detection performances.

At this stage of the tests, one can already conclude that the architecture of MIMOSA-8 looks very promissing, and provides the path to follow in 2006 for the next R&D steps towards a fast chip. The first of these steps will allow optimising the MIMOSA-8 architecture in terms of noise, amplification, etc. Next, an ADC circuit will replace the discriminators at the column ends, followed by the design of data sparsification micro-circuits. Meanwhile, the integrated architecture allowing to store and extract the cluster information is being developped. The choice between different possible signal processing architectures will be guided by the aim of keeping the instantaneous power dissipation well below 1 W/cm^2.

Besides the effort devoted to the design of the sensors adapted to the inner layers, a prototype (called MIMOSA-12) adapted to the outer layers was designed and sent for fabrication by the end of March 2005. It features 4 capacitors inside each pixel. The latter have a pitch of 35 μm. The

sensor includes 6 different sub-arrays exploring various MOS capacitors (50, 100 and 200 fF).

A major issue of the design consists in finding the smallest possible capacitors in order to integrate the largest possible number of them in each pixel. This trend may lead to the possibility of reaching integration times as short as those needed for the second layer, thus allowing to equip the latter with multi-memory cell sensors instead of the fast, column parallel, read-out architecture foreseen at present. MOS capacitors are mandatory for this goal, since they are typically 4-5 times more compact than poly-based capacitors. On the other hand, their time constant is much shorter. Making them small enhances the corresponding dispersion of characteristics, a default which worsens moreover with their reduced surface. These weak points may introduce an unaffordable loss of precision as one goes for the smallest possible capacitors. Compromise possibilities between a small size and a satisfactory precision are expected to come out from the tests of MIMOSA-12.

The optimisation of the sensor performances will also depend on features specific to each fabrication process available (see section 5). The fabrication process exploration will therefore be conducted in parallel and in accordance with the development of the sensor architectures.

4 Assessment of the radiation tolerance

Radiation tolerance studies were initiated in 2002-2003, mainly based on the first two MIMOSA prototypes, which provided preliminary estimates of the raw technology potential. Important steps were achieved in 2004-2005 with more recent chips, in particular with low energy electrons, which allowed to make substantial progress both in the understanding of the origin of certain damages as well as in the way to improve the sensor tolerance.

The sensors were irradiated with various types of particles in order to check that the neutron gas and the beamstrahlung electron doses expected at the ILC are affordable. The chips were in particular exposed to $\sim$ 1 MeV neutrons, 10 keV X-Rays and 9.4 MeV electrons.

4.1 Tolerance to 1 MeV neutrons

The effect of bulk damage [5] was first investigated a few years ago, by exposing small prototypes (MIMOSA-1 and -2) to fluences ranging from $10^{11}\mathrm{n}_{eq}\cdot\mathrm{cm}^{-2}$ to $10^{13}\mathrm{n}_{eq}\cdot\mathrm{cm}^{-2}$. A decrease of the charge collected was observed, which started to have significant consequences on the detection efficiency for fluences near $10^{12}\mathrm{n}_{eq}\cdot\mathrm{cm}^{-2}$.

Similar neutron irradiations were repeated in 2004 with more recent prototypes: the reticle size sensor MIMOSA-5 and the prototype MIMOSA-9 designed to explore a new type of fabrication process (described in section 5). The sensors were exposed to fluences ranging from $1\cdot10^{11}\mathrm{n}_{eq}/\mathrm{cm}^2$ to $1\cdot10^{12}\mathrm{n}_{eq}/\mathrm{cm}^2$. Their performances were assessed by exposing them to a $\sim$ 6 GeV e^- beam at DESY in April 2005. A preliminary analysis of the data collected with the MIMOSA-9 chip exposed to a fluence of $1\cdot10^{12}\mathrm{n}_{eq}/\mathrm{cm}^2$ shows that the detection efficiency remains unaffected, staying around 99.5 % at an operating temperature of -20°C. This observed tolerance is much superior to the performance required for the ILC ($\lesssim \cdot10^{10}\mathrm{n}_{eq}/\mathrm{cm}^2/\mathrm{yr}$).

4.2 Tolerance to 10 keV X-Rays

The first estimates of the sensor tolerance to ionising radiation were achieved with MIMOSA-2, showing that the sensors were not affected until the integrated dose exceeded $\sim$ 200 kRad (i.e. $\sim$ 4 times the maximal dose expected yearly at the ILC).

Further studies were performed in 2004, with integrated doses of up to 1 MRad [6]. They rely on tests of MIMOSA-2 and of another chip (called SUCCESSOR-1), borrowed from the SUCIMA collaboration [7], which designed it for imaging purposes. Both sensors were manufactured with

the same fabrication process, but feature different reset transistor designs: while the source of this (enclosed) transistor was in its center and the drain at its periphery in each MIMOSA-2 pixel, drain and source had swapped positions in SUCCESSOR-1, a feature expected to improve the chip tolerance to ionising radiation.

The effect of ionising irradiation was tested by illuminating MIMOSA-2 and SUCCESSOR-1 chips, exposed to integrated doses of 400 kRad and 1 MRad respectively, with an ^{55}Fe source. The response of the irradiated chips to the 5.9 keV X-rays emitted by the source is compared to that of non-irradiated chips on Fig. 3. The latter displays the distribution of part of the cluster charges in ADC units. While the distributions of the irradiated and non-irradiated SUCCESSOR-1 chips almost overlap, those of MIMOSA-2 do not. The shift of the large peak observed for this sensor expresses a substantial charge loss due to radiation damage, which is not at all visible for the irradiated SUCCESSOR-1 chip, despite the 2.5 times larger dose it was exposed to. Though it is not yet fully established that the improved radiation tolerance is not due to some undocumented change in the fabrication process, there is strong support for the hypothesis that the source and drain swap is at its origin.

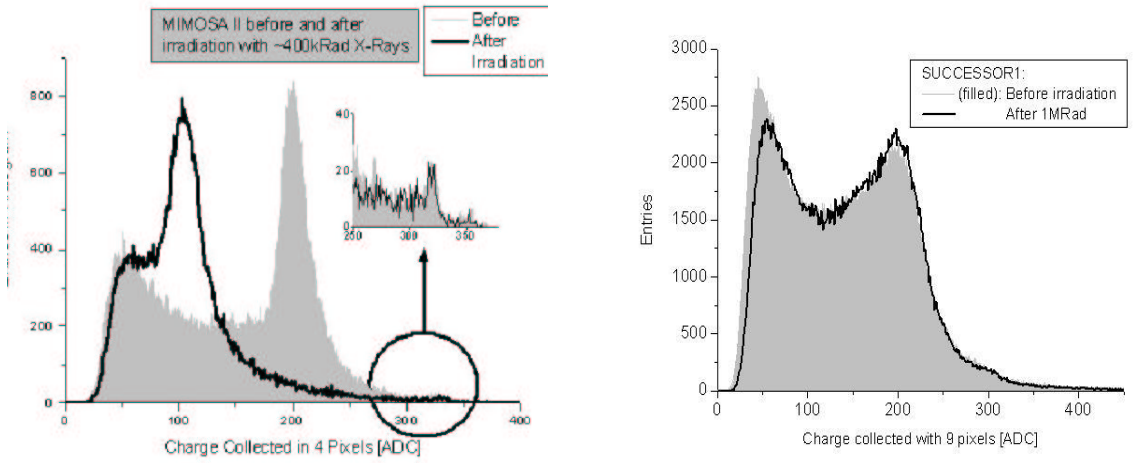


Figure 3: Effect of 400 kRad exposure on MIMOSA-2 (left) and of 1 MRad exposure on SUCCESSOR-1 (right). The response of non-irradiated (shaded histogrammes) and irradiated (black line) sensors is shown, when illuminated with an ^{55}Fe source.

The radiation hardness of SUCCESSOR-1 was observed to be limited by the raise of the sensing diode leakage current, translating into a hampering noise level at +20°C. Cooling the sensor to -15°C and shortening its integration time from 1 ms to 0.25 ms was found to be sufficient to dim this noise to a tolerable value for integrated doses of up to 1 MRad. These observations give a strong indication that the design of 1 MRad resistant CMOS sensors is under control. Moreover, they suggest that integrated doses well above 1 MRad may be tolerable (i.e. $\gtrsim$ 20 times the yearly upper limit expected at the ILC).

The importance of the fabrication process and of the operating temperature was also observed with tests of MIMOSA-9 sensors irradiated with 240 kRad of 10 keV X-Rays. A sub-array, equipped with 20 μm pitch and 3.4x4.3 μm^2 diodes, exhibited a residual noise of $\sim$ 45 e$^-$ENC at a temperature of +20°C. This was 5 times more than before irradiation. The noise 'increase translated into a S/N

value $\lesssim 5$ (MPV), which makes the detection efficiency drop to 65–85 %, depending on the cluster reconstruction criteria.

The situation changes dramatically when operating the irradiated chip at -20°C. The noise decreases below 15 e^-ENC, and the S/N value increases accordingly to ~ 18 (it was ~ 28 before irradiation). The detection efficiency rises to 99.8 $\pm$ 0.1 % (instead of 99.93 $\pm$ 0.03 % before irradiation), demonstrating that a modest cooling of the sensors allows to bring them back very close to the top of their performances[7].

4.3 Tolerance to 9.4 MeV electrons

Access has been found, in Spring 2005, to a low energy (9.4 MeV) electron beam, where the chips could be irradiated when being operated. These studies are particularly relevant for the understanding of the influence of beamstrahlung electrons, whose energies concentrate in the 9-10 MeV range.

MIMOSA-9 and -5 sensors were exposed to this electron beam. The chips received integrated doses of $3{\cdot}10^{12}e^-{\cdot}cm^{-2}$ and $1{\cdot}10^{13}e^-{\cdot}cm^{-2}$. The latter value corresponds to the maximal dose expected in the inner most layer after more than 5 years of operation. The data collected are still being analysed; preliminary test results of the MIMOSA-9 chip (20 μm pitch, 3.4x4.3 μm^2 diode) exposed to an integrated flux of $1{\cdot}10^{13}e^-{\cdot}cm^{-2}$, show that (at a temperature of -20°C), the S/N value is still high (~ 23 instead of ~ 28 before irradiation), and that the detection efficiency, which amounts still to 99.3 $\pm$ 0.1 %, exhibits only a marginal change.

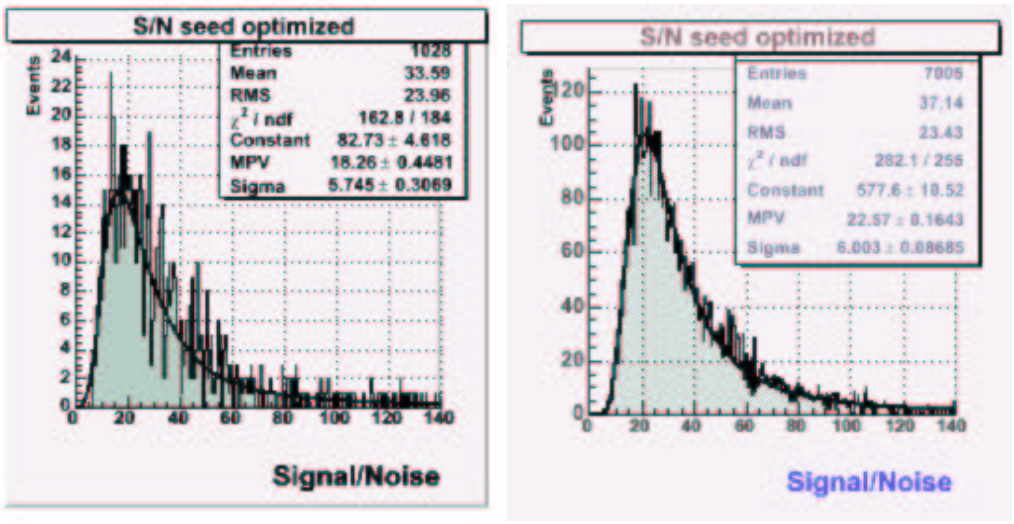


Figure 4: Signal-to-noise distributions of MIMOSA-9 sensors (20 μm pitch, 3.4x4.3 μm^2 diodes) irradiated with $\sim$ 1 MeV neutrons (left) and with 9.4 MeV electrons (right). The distributions were measured at an operating temperature of -20°. The left figure shows the chip response for a fluence of $1{\cdot}10^{12}n_{eq}/cm^2$; the right figure displays the response of a sensor exposed to $1{\cdot}10^{13}e^-/cm^2$.

[7] The sensivity to hard X-Rays (from a ^{60}Co source) has started recently with a prototype fabricated in 2004, and found to be significant (see section 5.2). More studies are needed before any conclusions can be drawn.

4.4 Summary on the radiation tolerance

The radiation tolerance studies performed in the last two years have established quite reliably that CMOS sensors can stand the ionising and non-ionising radiation doses to which the vertex detector is going to be exposed at the ILC, even if these doses come out to be much higher than the present Monte-Carlo predictions. This statement is however only fully valid if the sensors are operated at negative temperatures, typically $\lesssim$ -10°C (see for instance the signal-to-noise ratio of irradiated MIMOSA-9 sensors displayed on Fig. 4).

The sensitivity of the sensors may strongly depend on details of the the fabrication process. Each of them needs therefore to be carefuly evaluated in terms of tolerance to bulk damage and ionising radiation effects. It is also of interest to continue investigating the role of temperature (and time) in recovery procedures.

5 Exploration of fabrication processes

5.1 Motivation and major issues

The capability of developing radiation tolerant and fast sensors depends on basic fabrication parameters such as the epitaxial layer, the feature size, the number of metal layers, the leakage current, the doping and depth of the n- and p-wells, the oxide thickness, a.s.o., which may vary substantially from one fabrication process to another. Finding well adapted fabrication processes, which allow integrating the necessary signal conditionning micro-circuits in the sensor, with low pixel noise and pixel-to-pixel dispersion, is therefore a must.

Several manufacturing processes have been explored up to now:

- AMS-0.6 μm: MIMOSA-1, MIMOSA-5
- AMS-0.35 μm without epitaxial layer: MIMOSA-4, MIMOSA-12, MIMOSA-13
- AMS-0.35 μm OPTO with epitaxial layer: MIMOSA-9, MIMOSA-11
- MIETEC-0.35 μm (which became AMI-0.35 μm recently): MIMOSA-2, MIMOSA-6
- TSMC-0.25 μm: MIMOSA-8, MIMOSA-10
- IBM-0.25 μm: MIMOSA-3

Except of the IBM process (which featured a too thin epitaxial layer, presumably $\lesssim$ 2 μm), all these processes allowed to realise prototypes with good to excellent detection performances. These very satisfactory results were obtained because the noise of the pixels could be kept near 10 e^- ENC, a direct consequence of the simple pixel architecture, free of signal treatment micro-circuits such as those necessary for fast parallel read-out. These micro-circuits are expected to increase the total noise value by a factor of 2 to 3 (see section 3.1), restricting the choice of the manufacturing process to those exhibiting an epitaxial layer thickness $\gtrsim$ 8-10 μm.

Some processes, relying on a lightly doped substrate but exhibiting no epitaxial layer, allow to circumvent this handicap, the substrate acting as an effective thick (i.e. several tens of microns) sensitive volume. This was demonstrated with two prototypes (called MIMOSA-4 and SUCCESSOR-2) studied in 2003. Their tests demonstrated an outstanding detection efficiency of up to 99.9 %, and a single point resolution of about 2.5 μm [8]. However, the cluster size happens to be rather large, especially at low operating temperature, a feature which reduces the double hit resolution of the sensor. Moreover, the absence of side effects when thinning the sensors to $\sim$ 50 μm needs to be demonstrated. This type of manufacturing process is therefore not considered as the baseline for the ILC vertex detector R&D.

Another concern is the number of metal layers, which is quite often equal to 3 or 4 only in standard processes. It deserves much attention once signal treatment micro-circuits are to be

integrated in the sensor, imposing to chose processes offering at least 4 metal layers. Fortunately, present commercial processes based on features sizes below 0.25 μm rely on $\geq$ 6 metal layers.

5.2 Recent achievements

The manufacturer AMS announced a new fabrication process at the end of 2003, with 0.35 μm feature size and about 20 μm epitaxial layer. This process was supposed to be optimised for CMOS imaging applications, meaning that special care was taken of sources of leakage current in order to minimise the latter. MIMOSA-9 was designed and fabricated to explore this process. It is made of several sub-arrays, each exhibiting a different sensing diode or pitch size. The diode dimensions are either 3.4×4.3, 5×5 or 6×6 μm^2. The pitch is either 20, 30 or 40 μm in both directions.

Several prototypes were exposed to a $\sim$ 120 GeV/c pion beam at the CERN SPS. Excellent performances were observed [9], as illustrated by Fig. 5. The signal-to-noise most probable value ranges from $\sim$ 15 to $\sim$ 30, depending on the diode size, pixel pitch and operating temperature. This rather confortable magnitude translates into a detection efficiency exceeding 99.5 %, even in the case of a pitch as large as 40 μm, where charge collection is expected to eventually exhibit inefficiencies due to the sizeable path achieved by some charge carriers until the sensing diode. The single point resolution was also found to be excellent: $\sim$ 1.5 μm for a 20 μm pitch and $\sim$ 5 μm for a 40 μm pitch. These results allow to foresee a variable pitch for the vertex detector, ranging from 20 μm for the inner most layer to $\sim$ 40 μm for the outer layer, which translates into a reduced data flow and power dissipation.

Overall, these results make this fabrication process most attractive. There are however two features which weaken this statement. One of them concerns the total cluster charge, which was found to be $\sim$ 800-900 e^-ENC. This amount corresponds to an epitaxial layer of $\sim$ 10-11 μm, a thickness which was confirmed by visual check with a microscope, thus infirming the 20 μm announced by the founder. The second source of concern is related to the leakage current. The latter was indeed measured to be about one order of magnitude below the typical values of previous chips, but it increased by almost two orders of magnitude after 20 kRad irradiation with a hard ($\sim$ 1 MeV) ^{60}Co X-Ray source. This increase, which raised the noise by more than a factor 2, was however not observed for all sub-structures integrated in the chip, hinting to the possibility of containing the current increase.

In order to improve the radiation tolerance, a modified layout of the charge collection diode was designed in the fabrication process, and consecutively sent for fabrication. This new prototype, called MIMOSA-11, came back from fabrication in April 2005. Its design features various strategies of avoiding or minimising thick field oxide (bird's beak) near the junction, at the expense of a somewhat larger capacitance noise. Preliminary test results of some sub-arrays show that the dark current increases by only 50 % (instead of almost two orders of magnitude previously) after an exposure of 20 kRad, confirming that the sensitivity to hard X-Rays can most likely be circumvented.

In summary, the exploration of the AMS-0.35 μm OPTO manufacturing process is not yet completed, but one can already claim that it suits rather well to the sensor R&D for the ILC. It will therefore presumably be the baseline process for the fabrication of a substantial fraction of the next MIMOSA prototypes.

Given the evolution of the CMOS industry, it is excluded that the AMS-0.35 process will remain available until the production starts for the ultimate sensor ready to equip a vertex detector at the ILC. The R&D goals of the next years will therefore include testing fabrication processes offering a feature size below 0.25 μm, representative of the trend of the CMOS industry. Processes envisaged encompass IBM-0.13 μm, UMC-0.18 μm (eventually with triple well option) and AMS-0.18 μm (with low leakage current option).

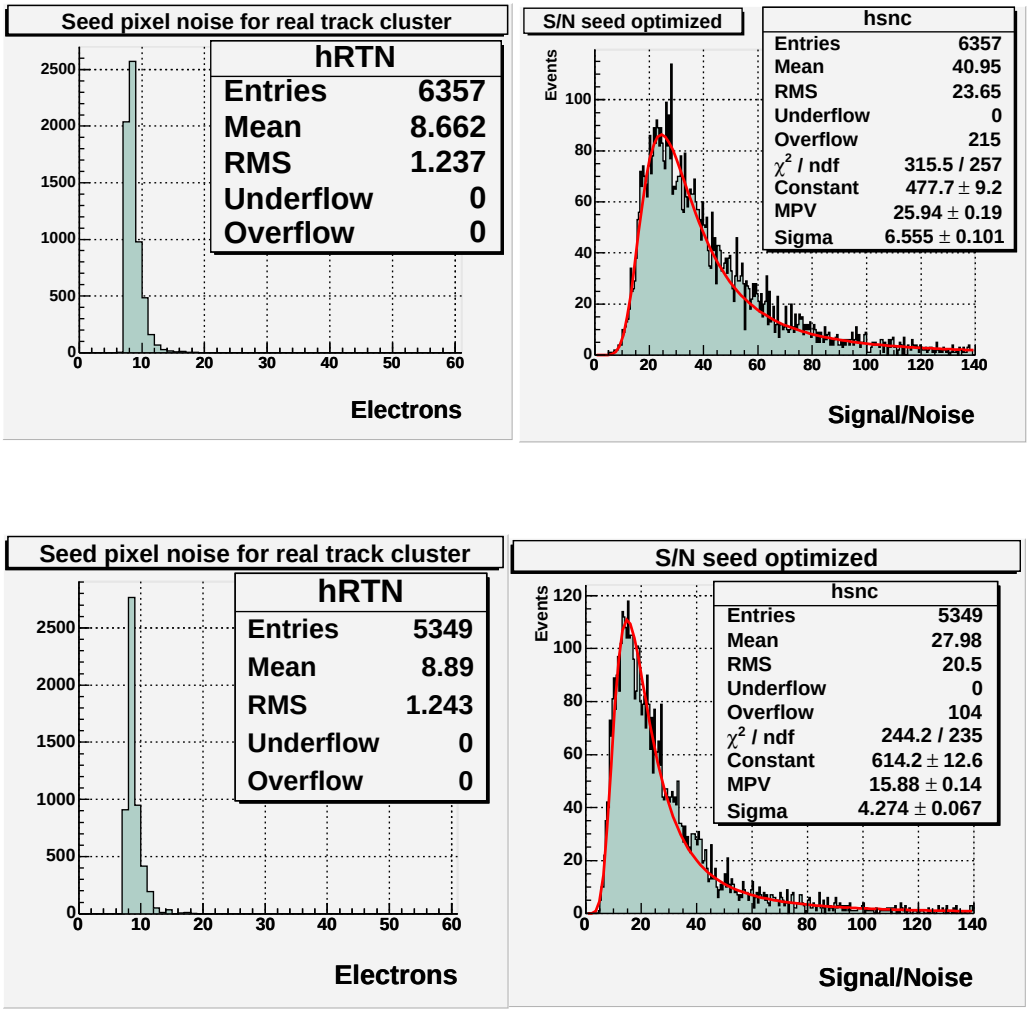


Figure 5: MIMOSA-9 beam tests results at 0°C for pixels of 20 μm (top) and 40 μm (bottom) pitch, equipped with a 3.4x4.3 μm^2 diode. The distributions shown are the residual noise after CDS (left) and the signal-to-noise ratio (right).

6 Thinning

6.1 General remarks

The question of thinning was not much addressed in the first years of the sensor R&D as it was not an issue of prime importance at that time. Ultimately, it will however become so, since the single point resolution offered by the sensors sets a severe constraint on the material budget if one aims to avoid swamping the resolution with multiple scattering.

The thickness ambitionned is $\sim 50\ \mu m$ and, if possible, twice less. While thinning sensors to $\sim 50\ \mu m$ is not expected to be particularly difficult or suspected to affect the sensor performances, a thickness of about 20 μm is considered as a challenge. The ability of industry to achieve it with a satisfactory yield needs to be assessed. Moreover, internal mechanical stress may occur, translating into wrinkling of the chip. The answer to this side effect may consist in glueing the chip on a thin carbon foam, diamond or beryllium support, which would ensure the necessary rigidity. A dedicated research effort has started, which oughts to encompass bonding issues, to investigate such possibilities. It profits from similar studies performed for the STAR upgrade and - eventualy - for the CBM experiment at GSI.

6.2 Achieved thickness

It is now established since a few years that reticle size chips (i.e. MIMOSA-5) can be thinned down by industry to 120-130 μm, without any noticeable side effect. This is still 2.5 times too much for the resolution ambitioned on the track origin. Attempts were made in 2003 and 2004 to thin MIMOSA-5 sensors down to $\sim 50\ \mu m$ or even much less.

The most agressive thinning trials were performed for imaging purposes within the SUCIMA project (E.U. 5th Framework Programme). The substrate was totally removed with a non-standard method, leaving the epitaxial layer protected by a $\sim$ 0.1–0.2 μm thin passivation film. This procedure, which resulted in a $\sim 15\ \mu m$ thin sensor, allowed to make it sensitive to electrons of a few keV only, as demanded for beta-imaging purposes. These sensors were exposed to $\sim$ 120 GeV pion beams at the CERN-SPS in order to investigate their minimum ionising particle detection performances. The detection efficiency was observed to amount only to $\sim$ 85 %, due to a substantial drop of the charge collected. Several reasons may explain this observation, hinting to possible improvements. This thinning method is thus not (yet) adapted to minimum ionising particle detection but its evolution towards better performances is not precluded.

Another, less agressive, thinning attempt was made, guided by the development for the STAR vertex detector upgrade. MIMOSA-5 wafers were thinned down to $\sim 50\ \mu m$ via STAR collaborators from LBNL with rather conventional industrial means. The first wafer thinned in this way (Autumn 2004) exhibited cracks shortly after thinning, of which the origin is still being investigated. Meanwhile, the procedure was repeated with individual sensors after their dicing. The thinned sensors were bonded to a prototype ladder using a 50 μm thin film adhesive at LBNL. Up to 9 chips were mounted on a single ladder. Preliminary test results show that the bonding technique is efficient and that the sensor functionalities tested are all preserved.

More recently, another company, located in Europe, was contacted and has accepted to thin MIMOSA-5 chips to $50 \pm 5\ \mu m$. The thinning of the first wafers is currently under way.

In conclusion, the procedure allowing to thin down the sensors to $\sim 50\ \mu m$ is still not fully established, but seems in good shape. Moreover, a more agressive goal, such as 20-25 μm, may be accessible on the mid-term.

7 Detector design studies

The detector concept taking best advantage of the CMOS sensor peculiarities in order to provide the required performances, is likely to rely on a geometry similar to the one described in the TESLA TDR (based on CCDs). It consists of 5 cylindrical layers with radii ranging from 15 to 60 mm. Depending on the layer, the polar angle coverage extends to $|\cos\theta| \sim 0.90 - 0.95$.

7.1 Geometry and read-out considerations

Some of the prominent characteristics of the detector are summarised in Table 1.

Layer	**Radius**	**Pitch**	$\mathbf{t}_{r.o.}$	$\mathbf{W}_{lad}$	$\mathbf{N}_{lad}$	$\mathbf{N}_{pix}$	$\mathbf{P}^{inst}_{diss}$	$\mathbf{P}^{mean}_{diss}$
L0	15 mm	20 μm	25 μs	7 mm	20	25 M	<100 W	<5 W
L1	25 mm	25 μm	50 μs	15 mm	26	65 M	<130 W	<7 W
L2	37 mm	30 μm	$<$ 200 μs	24 mm	24	75 M	<100 W	<5 W
L3	48 mm	35 μm	$<$ 200 μs	24 mm	32	70 M	<110 W	<6 W
L4	60 mm	40 μm	$<$ 200 μs	24 mm	40	70 M	<125 W	<6 W
Total					142	305 M	<565 W	<29 W

Table 1: Prominent features of the detector concept based on CMOS sensors. For each layer, the table indicates the layer radius, the pixel pitch, the read-out time ($t_{r.o.}$), the ladder width (W_{lad}) and number (N_{lad}), the number of pixels (N_{pix}), as well as the instantaneous (P^{inst}_{diss}) and average (P^{mean}_{diss}) power dissipations. The average dissipation is based on a detector duty cycle of 5 %. The usually assumed duty cycle of 1/200 would lead to a 10 times smaller value.

An overview of the detector geometry is shown in Fig. 7.1. Sketch views including or perpendicular to the beam axes are shown in Fig. 7.

Some main differences with the TESLA TDR geometry are:

- a faster read-out (and thus a larger number of ladders equipping the inner layers),
- a variable pixel pitch (and therefore a smaller total number of pixels: 300 millions instead of 800 millions), translating into a reduced data flux and power dissipation,
- less material at small polar angle,
- the absence of a cryostat.

The number of ladders in the 2 inner layers follows from the ambitionned read-out speed and granularity (i.e. pixel pitch), the ladder width being dictated by the number of pixels per column. This is illustrated on Fig. 8, which displays a sketch view of a ladder from the inner most layer.

It is (at least) 100 mm long. Its width amounts to 7 mm, out of which 5 mm are equipped with 20 μm pitch pixels, while 2 mm are reserved for the mixed and digital parts of the signal processing micro-circuits. The pixels are grouped in columns of 256 units, oriented perpendicular to the beam lines and read out in parallel at an effective clock frequency of $\sim$ 10 MHz, which translates into a column read-out time of $\sim$ 25 μs. While all functionalities of the signal processing chain up to the CDS are integrated in the pixels, the analog-to-digital conversion, data sparsification and signal transfer electronics are integrated in the 2 mm wide side band.

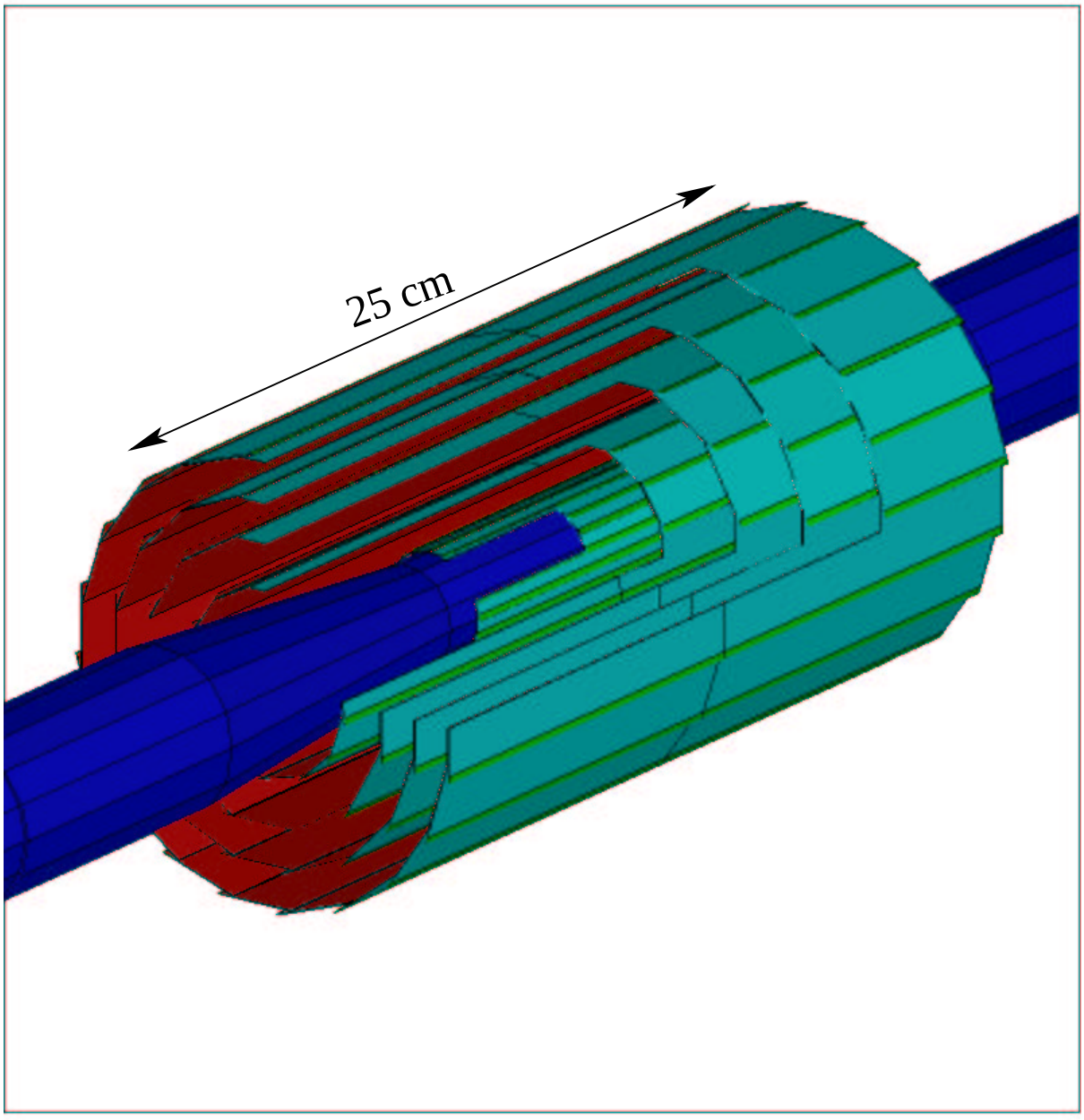


Figure 6: Overview of the detector geometry.

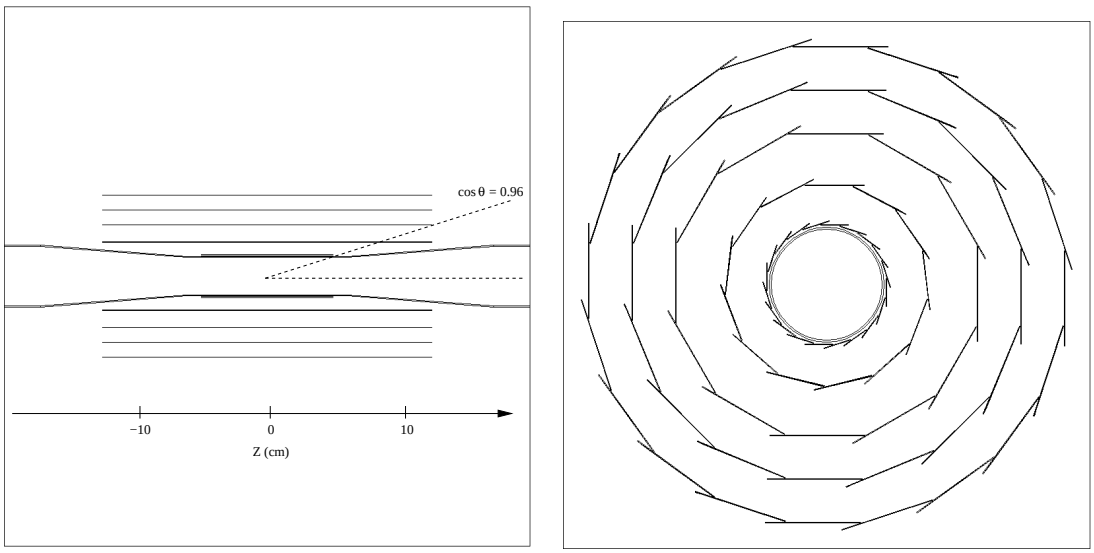


Figure 7: Side views of the detector geometry including the beam axes (left) and transverse to them (right).

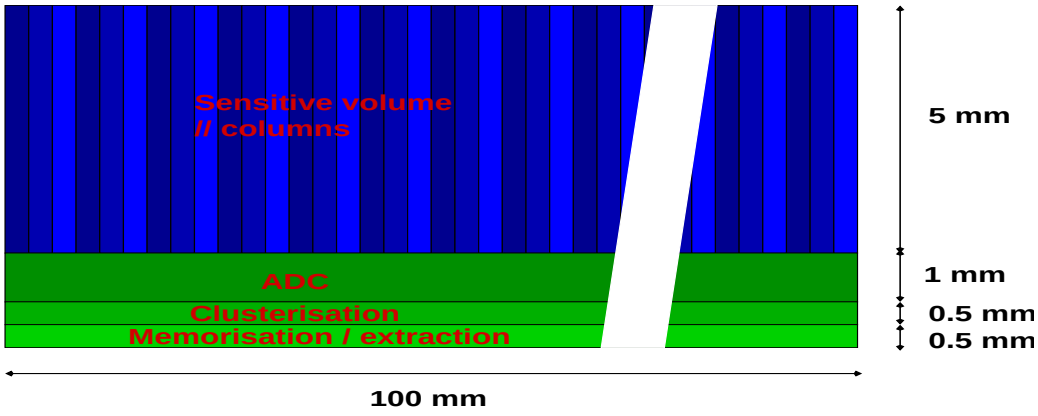
The second layer is equipped with pairs of 125 mm long ladders, stitched near the vertical to the interaction point. The ladder width amounts to 15 mm, shared between $\sim$ 13 mm long columns, perpendicular to the beam lines, and a 2 mm wide side band hosting the mixed and digital electronics. The columns are made of 512 pixels of 25 μm pitch. They are read out in parallel with an effective pixel read-out frequency of $\sim$ 10 MHz, which translates into a ladder read-out time close to 50 μs.

The 3 other layers are also composed of pairs of 125 mm long ladders. They are $\sim$ 24 mm wide ($\sim$ reticle width). Each pixel is equipped with $\geq$ 5 memory cells, read out after the end of each bunch train. Each memory cell collects a charge integrated over $<$ 200 μs. The pixel pitch is 30, 35 or 40 μm, depending on the layer.

Overall, the total surface of the detector is $\sim$ 3000 cm^2, covered by a total number of pixels of $\sim$ 300 millions (like the SLD vertex detector).

7.2 Comments on power dissipation

The total instantaneous power dissipated by each column is estimated to $\lesssim$ 1 mW, based on the fast sensor prototypes already fabricated. The sensor design is therefore optimised for a minimal number of columns in order to keep the power dissipated as low as possible. This pleads for the largest possible pixel pitch and for the longest possible columns (with the largest possible number of pixels per column). Increasing the pitch deteriorates the single point resolution and increasing the number of pixels per column slows down the read-out speed. The design studies show that an acceptable compromise can be found, which table 1 summarises in its present, still preliminary, version.



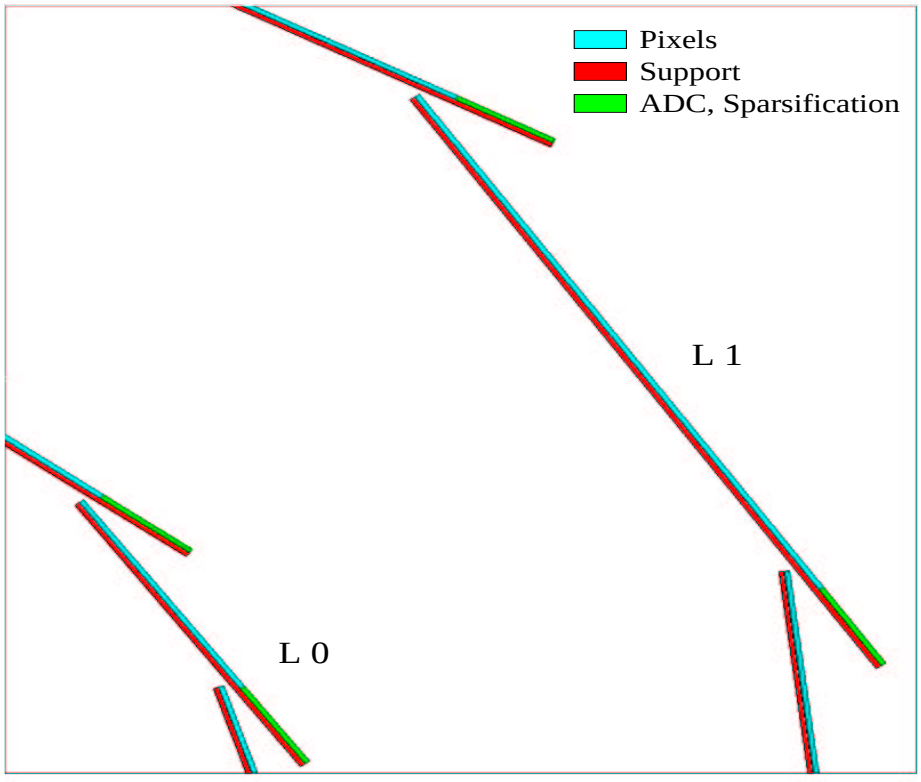


Figure 8: Top: Sketch view of a ladder equipping the inner most layer. Bottom: zoom on a section of the two inner layers, distinguishing the support (red), the part of the sensors made of pixels (blue) and the side band reserved to mixed and digital electronics (green).

For the whole detector, the expected instantaneous power dissipation would amount to $\lesssim 550$ W, a value which would still require substantial cooling. As for any of the technologies envisaged for the vertex detector, the crucial question arises on how well the beam time structure can be exploited to switch off (most of) the detector inbetween trains, or nearly so. It is usually assumed that the ILC duty cycle (expected to be close to the 1/200 proportion of the TESLA design) can be fully exploited. In this extreme case, the total average power dissipated would amount to $\lesssim 3$ W. This possibility remains however to be proven (see section 8). Moreover, the final beam time structure of the ILC, which doesn't need to be identical to the TESLA project one, is still to be defined. Meanwhile, a conservative approach was prefered for the present estimates, which assumes that the detector can be switched off (or nearly so) for at least 95 % of the time, an hypothesis which translates into an average dissipation of $\lesssim 30$ W. This value is still considered as being compatible with a light cooling system.

7.3 Material budget versus occupancy

The fact that the columns are oriented perpendicular to the beam lines allows to make them short enough to garantee a swift read-out of the layers most exposed to the beamstrahlung electrons, even if their rate happens to be significantly higher than predicted by present simulations. Since all signal processing functionalities cannot be integrated inside the pixels, the drawback is a narrow side band hosting integrated mixed and digital micro-circuits. This band, which is expected to be ~ 2 mm wide, adds material inside the fiducial volume of the detector (see Fig. 8).

This situation is particular to the CMOS sensor based vertex detector. The alternative technological solutions (e.g. CCD, DEPFET) rely on columns parallel to the beam axes, making it however more difficult to achieve read-out times $\lesssim 50\ \mu s$. Moreover, the read-out electronics is concentrated at the ladder edges, where its material affects the very forward tracking in a narrow angular range.

The consequence of the material budget excess due to the 2 mm side band, specific to the design presented here, was estimated. The loss in resolution on the impact parameter derived from the study is modest: overall, the parameter b, entering the canonical expression of the impact parameter resolution ($\sigma_{IP} = a \oplus b/p \cdot sin^{3/2}\theta$), increases by $\sim$ 5-10 %, depending on assumptions made on the thickness of the sensors and of the mechanical support and cooling system. The effect is mild essentially because of two reasons: i) the material of the beam pipe (500 μm of beryllium, i.e. 0.14 % of the radiation length) governs the multiple scattering parameter b, ii) b grows essentially like the square root of the fraction of radiation length.

In comparison, the benefit in read-out time is rather significant. It can be illustrated by comparing the radii of the inner most layer which provide the same occupancy for two different read-out times: 50 and 25 μs. This study was performed and showed that shortening the read-out time from 50 of 25 μs allows to reduce the radius of the inner most layer by $\sim$ 15-20 %. Since b is proportional to this radius, it decreases by the same amount.

7.4 Operating temperature

Several different sensor prototypes were operated at room temperature, and have provided excellent detection performances. It is however desirable to run the detector at a slightly negative temperature in order to reduce the sensitivty of the sensors to unexpected radiation effects, such as the rise of the electronic noise (see section 4.2).

Tests performed with various prototypes show indeed that a slightly negative temperature, i.e. -10 or -20°C, reduces already substantially several noise components, especially those related to the leakage current. Such an operating temperature is already achievable with a rather light cooling system, having mild consequences on the material budget. It does not require a cryostat.

More studies are still needed to refine the outcome of the present ones, aiming to find an optimal temperature which accounts for all basic parameters of the sensors. It would in particular be interesting to study the behaviour of the sensors (with and without epitaxy) at temperatures much below 0°C (e.g. liquid nitrogen temperature).

8 Cooling studies

An evaporative cooling system is being tested[10] for the cooling of the ladders. Compressed gas of a cooling agent, here R134a, expands through an expansion valve to a fluid close to the boiling point. This fluid flows through a thin pipe of 0.6 mm diameter and 0.05 mm wall thickness along the ladder underneath the area where the readout electronics is situated. The pipe is in thermal contact with the ladder. Heat transfer from the ladder into the pipes leads to evaporation of the fluid at constant temperature increasing the gas content of the cooling agent to about 80%-90%. The cooling agent is recompressed and recirculated.

The ladder is simulated by a glass plate of 0.03 mm thickness. The readout electronics, which produces most of the heat on the ladder, is replaced by 2 strips of very thin aluminum evaporated onto the glas. These strips have an electrical resistance of about 10 Ω. With a voltage around 10 V a heat source of around 10 W can be simulated.

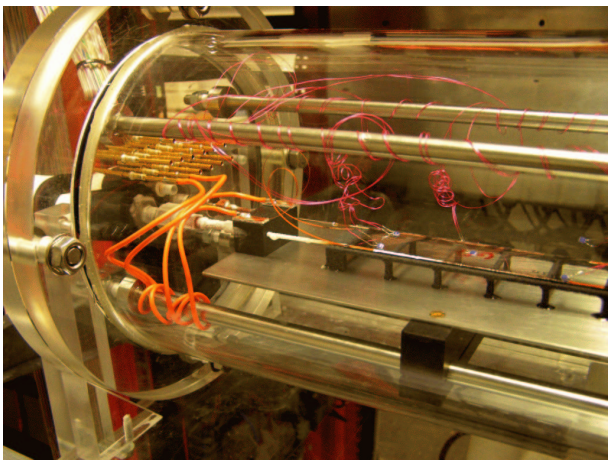
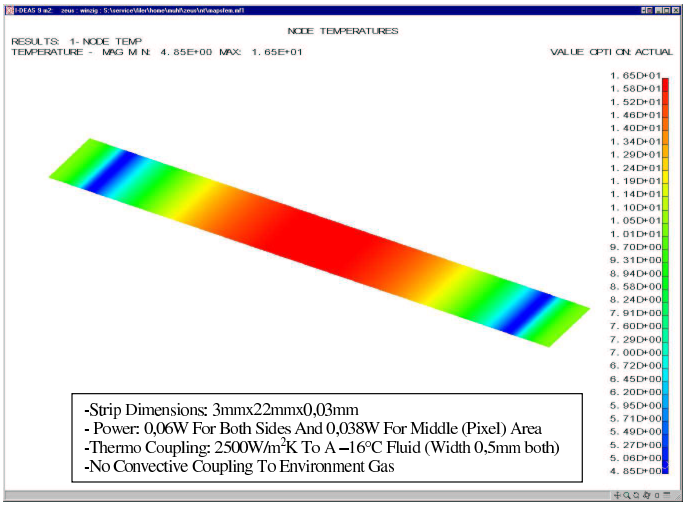


Figure 9: View of the Lucite cylinder with test ladder for power dissipation and cooling studies.

Figure 9 shows a view of the Lucite cylinder with the test ladder connected to a carrier of carbon-silicon foam, into which the cooling pipes are integrated, together with the electrical connections and thermal sensors which are read out at the front face of the cylinder. Temperatures of down to -12°C have been achieved. However, the long term stability of the whole system is not yet satisfactory. Presently the cooling rack hosting the system is being equipped with additional electrically controlled valves to regulate the temperature of the expanded cooling agent and improve the stability.

The temperature profile on the ladder has been calculated with a finite element program under the assumption that the areas under the cooling pipes are kept at a fixed temperature. A calculated temperature profile across the ladder is shown in Fig. 10.



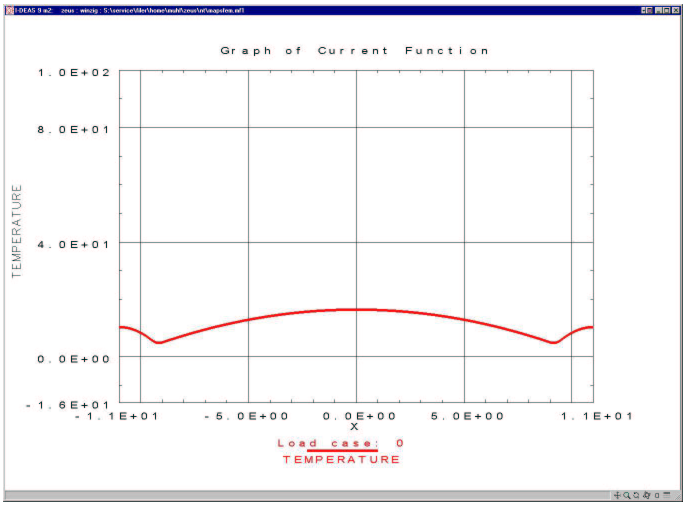


Figure 10: Simulated temperature profile across one ladder.

9 Mechanical support studies

The STAR collaboration at RHIC is currently preparing un upgrade of the apparatus, in order to fully exploit the planned increase of the machine luminosity. This increase is accompanied by a reduction of the beam pipe radius. The space freed by this reduction is expected to host 2 layers of CMOS sensors of the MIMOSA series developed at IReS-Strasbourg.

3 mechanical support prototypes have been designed at LBNL and fabricated, on which MIMOSA-5 sensors, thinned down to 50 μm, were mounted [11]. Up to 9 sensors are mounted contiguously on the ladders. When designing the ladder, special attention was given to sources of multiple scattering. The supports are therefore particularly light, their lightest version featuring only ~ 0.25 % of radiation length. Tests are going on, and provide very satisfactory results up to now.

10 Outlook

The two coming years will allow to finalise on-going studies, and to address some issues which were not yet top priorities. An overview of the different topics is provided hereafter.

10.1 Read-out architectures

The first objective is to finish testing MIMOSA-8 in the laboratory (combined analog and digital parts) and make it work on a test beam. Its radiation tolerance needs also to be assessed. Based on the results of all these tests, a modified (improved) design should come out by the end of 2005 or early in 2006. This new prototype (designed by Saclay and IReS in TSMC-0.25 technology) may come back from the foundry in April-May 2006.

In addition to the usual signal sensing and read-out chain, the chip will also host test structures exploring the ADC design foreseen to replace ultimately the comparators at the column's ends. Major constraints on the ADC are its allowed surface (and aspect ratio) and consumption (during train collisions and inbetween consecutive trains). Tests of the chip will be carried on through most of 2006.

The design of the first prototype with digital output should come out from these tests, and eventualy be fabricated by the end of 2006 or early in 2007. If successful, this architecture will be the basis of the first fast large scale prototype with digital output, eventualy available by the end of 2007.

Besides the R&D in the TSMC-0.25 μm technology exploiting the MIMOSA-8 architectures, ADC designs will be explored with the AMS-0.35 μm technology. Several test structures and pixel based prototypes may be fabricated in 2006. This R&D line as well may lead to a macroscopic prototype design in 2007.

These developments address first of all the fast sensors supposed to equip the first two layers of the vertex detector. The architecture based on memory-cells integrated inside the pixels will be developed separately. The tests of MIMOSA-12, which should start in June 2005 and take several months, will allow to figure out how compact accurate capacitors can be, and thus how many of them can be integrated in a pixel of given pitch. The delayed output architecture of the pixel matrix will also be tested.

The next prototype exploiting this sensor design will focus on rather elaborated pixel designs and still exploratory mixed micro-circuits. It will take advantage of the ADC development mentioned above. Its design (at IReS) should be completed early in 2006, allowing the chip to be fabricated (in AMS-0.35 technology) by Spring 2006. Most of 2006 will be devoted to its tests.

The third generation of this sensor architecture may include a signal processing chain including a 4/5-bit ADC, and may be fabricated (in the same technology) in the first half of 2007.

First attempts will also be made to design micro-circuits achieving sparsification. The retained algorithm may be implemented in a FPGA in order to first test and tune it with real digitised sensor signals. Test structures exploring micro-circuit designs may start being fabricated in 2007.

Besides these design evolutions, technologies offering a feature size below 0.25 μm will be explored. The first step, which may occur by the end of 2005, will consist in designing some basic test structures in technologies such as IBM-0.13 μm of UMC-0.18 μm. The aim is to prepare for a translation of the sensors designed from 2005 to 2007 in AMS-0.35 and TSMC-0.25 technologies, to these deeper sub-micron technologies around 2007-2008. This R&D will be performed at IReS in collaboration with several institutes in Europe and North-America (Saclay, IN2P3 laboratories, LBNL, etc.).

Finally, most of the designs foreseen in the coming years should progressively include the possibility to run the sensor in a pulsed power mode. In order to do so, the designs will foresee a splitted powering of some transistors, where the most intense of both power lines will be switched

off between trains, the weakest power line remaining switched on in order to prevent the transistor from changing polarity untimely.

10.2 Radiation Tolerance

At first order, the adequacy of CMOS sensors to the ILC radiation conditions is rather well established. Substantial work is however still needed in order to better understand the vulnerability of the sensors, its dependence on temperature, on fabrication process details, a.s.o. The on-going studies at IReS and DESY-Univ. Hamburg will therefore continue, based on irradiations with 9.4 MeV electrons in Darmstadt and with $\sim$ 1MeV neutrons in Dubna. The influence of the temperature needs also to be studied more extensively.

Moreover, each new sensor prototype (see previous subsection) will be characterised w.r.t. the ILC radiation dose requirements (e.g. neutrons and electrons). This remark applies in particular to each new fabrication technology explored. The R&D on the sensor radiation tolerance will therefore still be of central importance and will still necessitate substantial efforts at IReS and DESY.

10.3 Thinning - Mechanical support

The objective is to achieve a reliable industrial procedure within the coming two years, which allows to thin down the sensors at $\lesssim$ 50 μm with a high yield. The tuning of the procedure will use a stock of MIMOSA-5 wafers available at IReS.

So far, three directions exist to approach this goal: the on-going development at LBNL for the STAR upgrade, which relies on a 50 μm thinning performed in the US; a thinning procedure being set-up by a French company for IReS, aiming for 50 μm; a thinning procedure allowing to remove completely the substrate, proposed by another French company, in contact with IReS.

These three possibilities will be exploited in parallel. Reliable test results of MIMOSA-5 sensors thinned to 50 μm will be already available in 2005. Depending on the results, trials will be made, to thin the sensors down to 25 μm. First results on the reliability of such an extreme thinning should come out in 2006.

The procedure used to remove the substrate from the sensor for imaging purposes is not yet adapted to provide a m.i.p. detection efficiency in excess of 99 %. Contacts will however be established by IReS with the relevant company to investigate how its procedure could be modified to achieve such a goal.

Manufacturing processes offering no epitaxial layer but a low doping substrate instead, may provide very attractive performances once the sensors are thinned down to about 20 μm. Finding a procedure to achieve this goal would thus be a breakthrough. Attempts will be made to find a company able to set-up such a procedure. To really make the necessary trials, one would however need to manufacture reticle size sensors based on the design of MIMOSA-9 fabricated in the relevant AMS-0.35 technology, an operation costing at least 150 keuros.

The issue of thinning deserves looking for still other companies susceptible of offering highly agressive thinning possibilities. DESY will investigate if possibilites exist in Germany or neighbour countries. Contacts are being set up by IReS with H.E.P. institutes in Japan having thinned CCDs, which may be ready to make similar trials with MIMOSA-5 wafers.

Efforts invested in finding adequate thinning procedures need to be backed-up by similar efforts aiming for very light mechanical supports. This issue, which was not yet much addressed within the ILC CMOS sensor community, will become an important activity in the coming two years. It may build up on the current R&D effort going on at LBNL for STAR, and is very likely to end-up with a prototype ladder hosting several MIMOSA-5 sensors in 2006-2007.

10.4 Sensor operating conditions

Optimised operating conditions of the sensors are still to establish. They concern the operating temperature, as well as the pulsed powering of the sensors needed to achieve a low average power dissipation.

Exploring the response and the performances of the sensors as a function of temperature is still a quite widely open field. Up to now, the sensors were always operated at temperatures exceeding -40°C. It may however be of interest to test their behaviour at very low temperatures, such as that of liquid nitrogen.

Cooling studies performed at DESY will be carried on, together with pulsed powering of the chips. A major outcome expected from the trials to pulse MIMOSA-5 is the demonstration that the sensors can indeed be pulsed in a way where the duty cycle of the collider is exploited with high efficiency. This duty cycle being in the order of 1/100, the aim is to reduce the fraction of time during which the sensors are on to a similar magnitude. A duty cycle of the sensors in the order of 1/20 would in principle already be quite satisfactory. The two coming years should shed light on this crucial issue.

10.5 Detector geometry studies

The cylindrical detector geometry assumed in this report needs still to be refined w.r.t. basic issues, such the length of the inner most layer, the radius of the second layer, the connexion with the tracking devices next to the vertex detector, the optimal pixel pitch for each layer, a.s.o.

The studies carried at IReS will thus continue, guided by physics studies based on the detector design presented in this report, which will be implemented in the standard ILC simulation programmes.

11 Summary and Conclusion

The R&D on CMOS sensors for the ILC vertex detector has made substantial progress during the last two years, making it more and more plausible that the detector performance requirements can indeed be met with such sensors.

The main outcome of these two years of R&D are summarised below:

- the detector requirements dictated by the rate of beamstrahlung electrons have been estimated with improved accuracy w.r.t. previous computations (i.e. TESLA TDR). The constraints on the read-out speed and radiation tolerance take the spatial distribution of the electrons into account and include a safety factor reflecting some major uncertainties affecting the rate predictions. They are therefore more severe than previous estimates;
- detector design features specific to the use of CMOS sensors were investigated, leading to a detector concept which exhibits some significant differences with the TESLA TDR baseline. One of the most substantial differences is the read-out time of the two inner layers: 25 μs and 50 μs instead of 50 μs and 250 μs respectively. An other difference concerns the material budget: a side band of the sensors is entirely devoted to integrated signal processing micro-circuits, and is therefore not participating to the detection. The effect of the additional material introduced on the path of the particles detected has been estimated and found close to marginal;
- the R&D on a sensor integrating fast, column parallel, signal processing micro-circuits adapted to the two inner layers has made substantial progress. It has come to an architecture, which includes CDS inside each pixel and a comparator at the end of each column, exhibiting low

noise (i.e. < 20 e$^-$ENC) and pixel-to-pixel dispersion. Though its tests are not yet completed, it looks like a breakthrough, and indicates the path to follow towards the next steps of the signal processing chain, which encompass the design of a fast ADC and of data sparsification micro-circuits;

- the design of the sensor architecture adapted to the three outer layers, which is less demanding, is also progressing: the first dedicated chip is expected back from fabrication in June 2005. It explores the possibility of storing the charge integrated in 4 time slots of < 200 μs in 4 capacitors integrated in each pixel, and of processing the signal after a 1 ms delay;
- an attractive manufacturing process has been found, which provides high signal-to-noise ratios. It allowed to explore quite systematically the sensor response as a function of pixel pitch, diode size and temperature. The possibility to equip the different vertex detector layers with sensors featuring a pitch being larger for the outer layers than for the inner ones was validated. This allows to reduce the data flux and the total number of columns, which alleviates the total power dissipated. The mean value of the latter has been estimated to $\lesssim 3 - 30$ W, depending on the assumption made on the detector duty cycle;
- the radiation tolerance of several different chips has been assessed with various types of irradiations. One of the most innovative study was performed with sensors irradiated with 9.4 MeV electrons representative of the beamstrahlung flux expected at the ILC. Overall, the test results provide evidence that the sensors will stand all sorts of expected beam backgrounds, even if their rates are substantially higher than predicted by present Monte-Carlo simulations;
- the possibility to thin the sensors down to ~ 50 μm or less was also addressed. Reticle size sensors (MIMOSA-5) were successfully thinned to 50 μm. They were consecutively mounted on prototype ladders developed for the STAR vertex detector upgrade, and are currently being read-out for extensive test purposes.

The next two years should allow to consolidate the detector concept, the thinning procedure (trying a thickness close to 20-25 μm) and the possibility to keep the average power consumption low (by switching the detector off during most of the time inbetween trains).

The design of the sensor architectures foreseen for the inner and the outer layers should progress substantially. One of the most important outcomes should be a fast ADC (of typically 4 bits) which will be integrated in the side band at the end of each column of a cm^2 wide sensor. Another important result is expected, which governs the potential of the architecture adapted to the outer layers: the maximal number of memory-cells which can be integrated in a pixel of given pitch will be known. Progresses on the design of sparsification architectures are also foreseen.

Finally, the characterisation of some fabrication processes providing a feature size below 0.25 μm will have started. This exploration of new fabrication processes will be carried on in parallel with on-going investigations of the sensor radiation tolerance, to ~ 10 MeV electrons in particular.

It is worth noticing that this R&D programme on high precision, swift, slim and low power CMOS sensors addresses a large panel of applications, which encompasses other future vertex detector projects and extends to particle imaging for bio-medical applications as well as for nano-sciences. It benefits therefore from the synergy with scientific communities far from the ILC topics. A major outcome of this tendancy is that a detector made of CMOS sensors is likely to be operational for one these other applications before the ILC starts.

References

[1] R. Turchetta et al., *Nucl. Inst. Meth.* **A458**, 677 (2001).

[2] M.Winter et al., *Proc. of the 8th ICATPP*, Como (Italy), October 2003.

[3] G.Deptuch et al., *Proc. of the IEEE Nuclear Science Symposium*, Portland (Oregon), September 2003; *to be printed in IEEE Trans. Nucl. Sci.* (2004).

[4] Y.Degerli, G.Deptuch et al., *Proc. of the IEEE Nuclear Science Symposium*, Roma (Italy), Octobre 2004; *to be printed in IEEE Trans. Nucl. Sci.* (2005).

[5] M. Deveaux et al., *Nucl. Inst. Meth.* **A512**, 71 (2003).

[6] M.Deveaux et al., *proc. of 5th Int. Conf. on Radiation Effects on Semiconductor Materials, Detectors and Devices,* Firenze (Italy), Octobre 2004; *to be printed in Nucl. Inst. Meth.* **A**, (2005).

[7] http://sucima.dipscfm.uninsubria.it/

[8] W.Dulinski et al., *Proc. of the IEEE Nuclear Science Symposium*, Portland (Oregon), September 2003; *to be printed in IEEE Trans. Nucl. Sci.* (2004).

[9] W.Dulinski et al., *Proc. of the IEEE Nuclear Science Symposium*, Roma (Italy), Octobre 2004; *to be printed in IEEE Trans. Nucl. Sci.* (2005).

[10] details can be found in the note accessible on the following Web page: http://www-zeus.desy.de/~ gregork/MAPS/summary_prc.pdf

[11] details can be found on a web page written by Leo Greiner: http://www.lbnl.leog.org/2005_04_06_ladder_status.htm

[12] http://ireswww.in2p3.fr/ires/recherche/capteurs/index.html