PRC PROPOSAL PROGRESS REPORT

DEVELOPMENT OF CMOS SENSORS FOR A LINEAR COLLIDER VERTEX DETECTOR

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Abstract

CMOS pixel sensors are developed by the IReS-LEPSI collaboration since 1999 for future vertex detectors needing very high granularity and minimal material budget. The first prototypes, made of small arrays of a few thousands of pixels, demonstrated the viability of the technology and its high tracking performances, and were at the origin of the PRC proposal made in October 2001.

Substantial progress was achieved since: The tracking performances of the first prototypes were further investigated; A real size prototype was designed, fabricated, and tested; The radiation tolerance of the sensors was investigated; The performances of a new fabrication process, relying on a low doping substrate, were assessed; The first sensor with signal processing micro-circuits integrated on its substrate was designed and tested. The note summarises these achievments and provides an outlook on the coming steps of the R&D, which include major system integration issues.

1 Introduction

The development of Monolithic Active Pixel Sensors (MAPS) for charged particle tracking was initiated by the IReS-LEPSI (Strasbourg) collaboration in 1999. This new class of pixel detector, manufactured in standard CMOS technology, allows to integrate signal processing (amplification, noise subtraction, discrimination, digitisation, etc.) on the detector substrate, which may be thinned down to a few tens of μm. The key element of this new tracking technique is the use of an n-well/p-epi diode to collect, through thermal diffusion, the charge generated by the impinging particle in the thin epitaxial layer underneath the read-out electronics [1].

The ability of these sensors, called MIMOSA[2], to provide charge particle tracking is now well established [2]. This report summarises the latest results on their tracking performances and radiation tolerance, and introduces the major next R&D steps.

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[2]standing for Minimum Ionizing MOS Active pixel sensor.

2 The situation in October 2001

The first prototypes (MIMOSA-1 and -2), made of small arrays of a few thousands of pixels, were exposed to 120 GeV/c π^- beams at the CERN-SPS in order to assess the viability of the technology and its tracking performances. A detection efficiency exceeding 99 % and a single point resolution of $\sim 1.5\mu m$ were observed [3]. Overall, MIMOSA-1 exhibited better performances than MIMOSA-2, its thicker epitaxial layer ($\sim 14\ \mu m$ against $4\ \mu m$) originating larger signal charges.

Some results obtained at the SPS are illustrated on Figure 1 and 2.

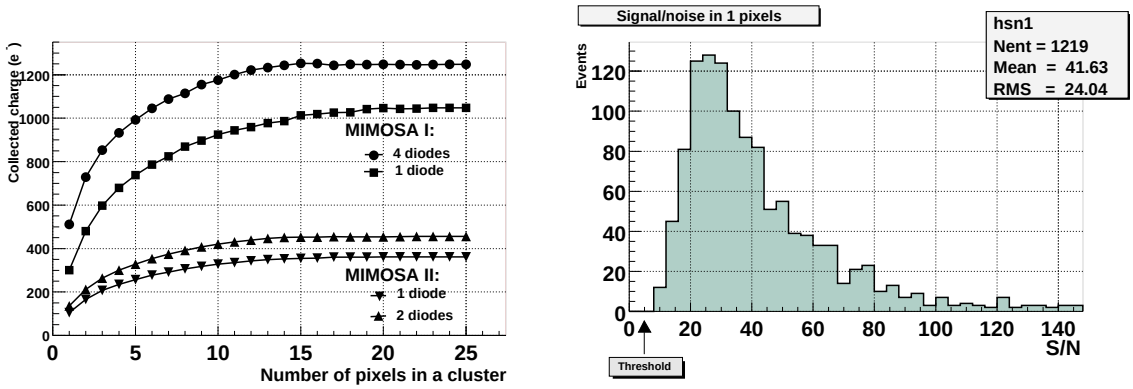

Figure 1: Left: Signal charge collected versus cluster multiplicity. Data collected with MIMOSA-1 are shown for two prototype structures differing by the number of diodes per pixel (1 and 4). Data collected with MIMOSA-2 are shown for structures with 1 or 2 diodes per pixel – Right: Signal-to-noise ratio observed with MIMOSA-1 in the seed pixel of each cluster (1 diode per pixel).

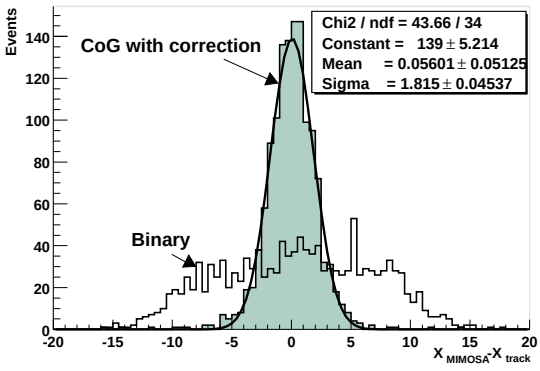

Figure 2: Residues between extrapolated and reconstructed track impacts in MIMOSA-1. The shaded distribution (annotated "CoG with correction") results from a centroid algorithm using the charge deposited in several pixels of the cluster, while the empty histogram (annotated "Binary") was obtained with the cluster seed pixel alone.

3 Recent studies of tracking performances

More recently, these data were used to estimate the double hit resolution by artificially moving, step-by-step, a signal cluster of one frame towards the signal cluster of another frame. Applying this procedure to a few thousands of cluster pairs, the probability to distinguish two neighbour clusters was computed as a function of the distance between the two cluster centers (Figure 3-left). Due to the sizeable cluster multiplicity and to the rather comfortable signal-to-noise ratio ($\sim$ 25-30 for MIMOSA-1), excellent cluster separation is observed down to distances below $30\mu m$.

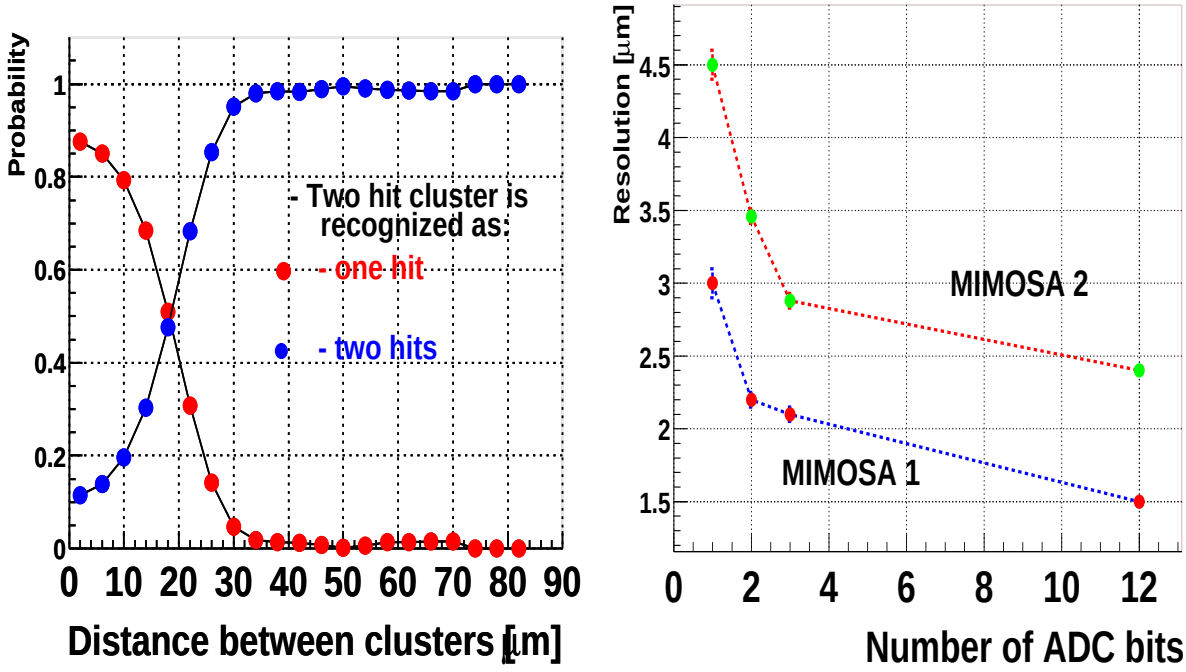

Figure 3: **Left:** Double hit resolution versus distance between clusters — **Right:** Single point resolution as a function of the number of ADC bits for MIMOSA-1 and -2.

The test data were also used to estimate the loss in single point resolution once the signal charge is digitised on a restricted number of ADC-bits. The charge measured with MIMOSA-1 and -2, originally recorded on 12 bits, was converted off-line into a 3-, 2- or 1-bit information (Figure 3-right). The analysis shows that a 3-bit encoding would still allow a single point resolution close to $2\mu m$ (in case of MIMOSA-1), and that the extreme case of only 1-bit may still provide $\sim 3\mu m$ resolution, a value twice better than the digital resolution ($5.8\mu m$) associated to the pixel pitch ($20\mu m$).

The necessity to operate the sensors at high read-out speed translates into a very high data flow (up to $\sim$ 500 Gbits/s/cm^2), making it mandatory to implement very efficient sparsification micro-circuits on the sensor substrate. These signal processing architectures need to be designed with great care in order to minimise the noise they introduce, thus degrading the signal-to-noise ratio (S/N).

The question was addressed, for which value of the average S/N the detection efficiency and/or the single point resolution would become to poor. The data collected with MIMOSA-1, -2 and -5 (see section 6) were used for this purpose. Figure 4 shows how the single point resolution of MIMOSA-1, -2 and -5 is related to their average S/N. The measured noise of MIMOSA-1 was then scaled off-line by factors of 2, 3, 4 and 5 and the cluster reconstruction was consecutively repeated. The result is illustrated by the single point resolution and detection efficiency curves (and dots) annotated "simulation" on Figure 4.

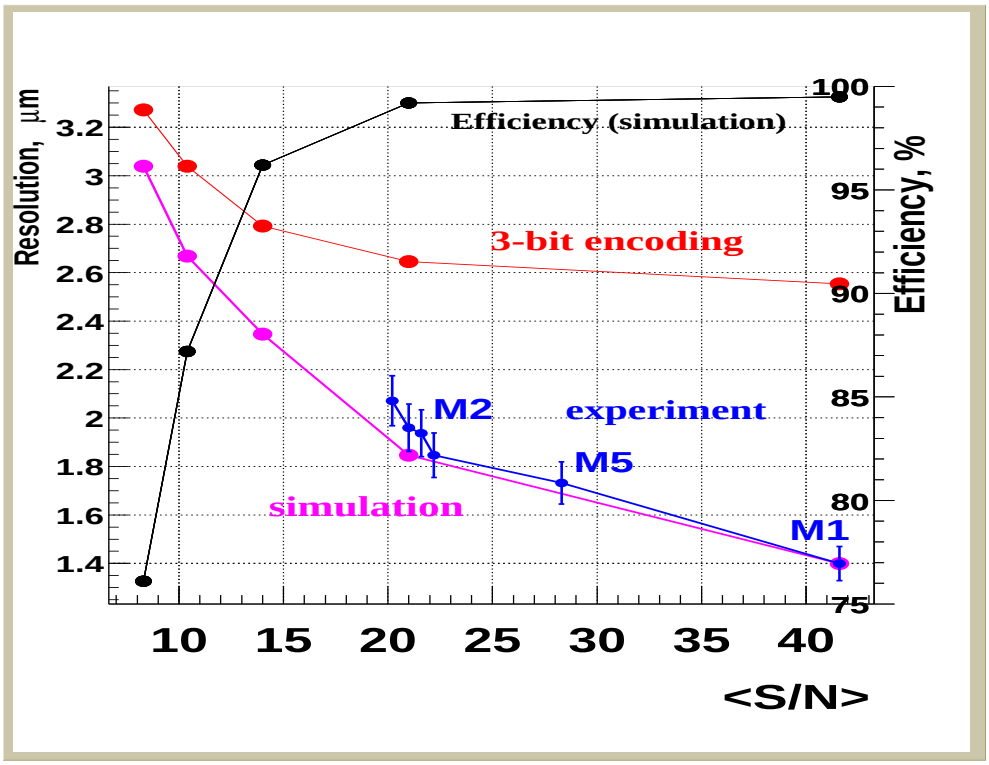

Figure 4: Variation of the single point resolution (scale on left side) and of the detection efficiency (scale on right side) as a function of the average value of the signal-to-noise ratio. The points with uncertainties stand for measurements performed with a MIMOSA-1, a MIMOSA-5 and 4 different MIMOSA-2 sensors. The curves annotated "simulation" show how the MIMOSA-1 single point resolution and detection efficiency degrade when increasing the measured noise by factors of 2, 3, 4 and 5. The variation of the single point resolution is also shown after encoding the MIMOSA-1 signal charge on 3 bits.

One observes that the values measured with MIMOSA-2 and -5 are well reproduced, a fact which pleads for the predictivity of this "simulation". The latter shows that an increased noise would first degrade the detection efficiency to an unacceptable value (e.g. 96 % when the average S/N is about 14), while the resolution remains better than 3 μm for very low values of the average S/N. Once the charge is encoded on 3 bits, no significant resolution loss is observed as long as the average S/N remains above 10 or so. The main outcome of this study is that for a LC vertex detector, the detection efficiency is by far the parameter most exposed to potential electronic noise consecutive to the implementation of signal processing micro-circuits, and that the development of future sensor prototypes integrating sparsification should satisfy the constraint that the average S/N remains well above 15.

4 Performances of a prototype without epitaxial layer

A prototype (MIMOSA-4) was fabricated in a 0.35 μm process without epitaxial layer and based on a low doping substrate ($\sim 10^{14}$ atoms/cm^3). Its tests at the CERN-SPS exhibited a detection efficiency close to 100% and a single point resolution of $\sim 4\mu m$ (see Figure 5).

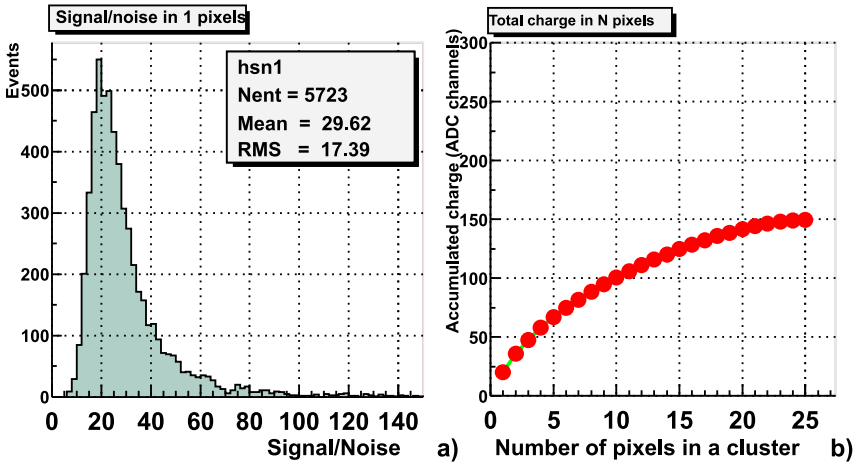

Figure 5: MIMOSA-4 seed pixel S/N (left) and charge versus cluster multiplicity (right).

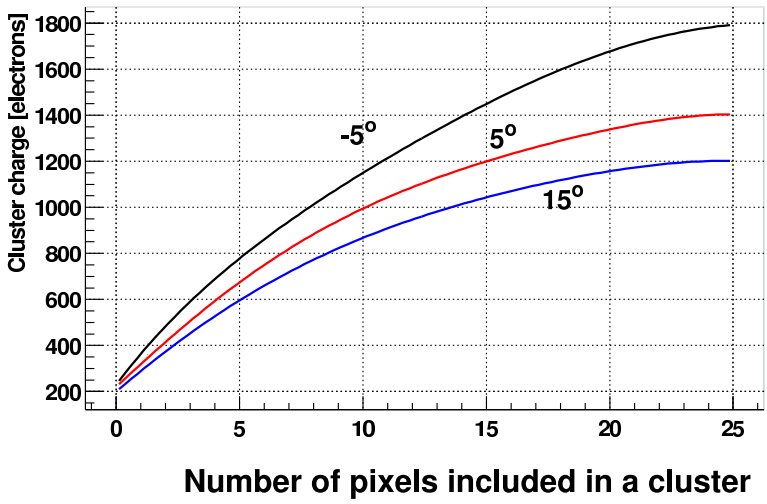

Figure 6: MIMOSA-4 test data: variation of the signal charge with the cluster multiplicity for 3 different values of the operating temperature.

The chip characteristics were also studied as a function of temperature. Figure 6 displays the cluster average signal charge measured at various temperatures as a function of cluster multiplicity. One observes that the charge increases substantially when decreasing the temperature, a fact expressing the temperature dependence of the charge carrier mobility.

In summary, the tests of MIMOSA-4 demonstrate that a particularly high S/N can be ob-

tained with this technology, especially for low operating temperature. This advantage allows to design signal processing architectures which are less constrained to low noise. On the other hand, the cluster size and single point resolution are slightly less favourable than those obtained with sensors including an epitaxial layer. More refined studies are still needed to conclude on the adequacy of this manufacturing process for a LC vertex detector.

5 Tolerance to high neutron doses

The radiation tolerance w.r.t. bulk damage [4] was investigated by exposing MIMOSA-1 and -2 sensors to neutron doses of up to $10^{13}\mathrm{n}_{eq}\cdot\mathrm{cm}^{-2}$. As the fluence approaches $10^{12}\mathrm{n}_{eq}\cdot\mathrm{cm}^{-2}$, charge losses occur (see Figure 7). The noise was observed to increase only moderately and the gain remained unchanged. All together, these variations translate into a decrease of the detection efficiency starting to be significant near $10^{12}\mathrm{n}_{eq}\cdot\mathrm{cm}^{-2}$, a value several orders of magnitude above the rate expected at a LC, which is in the range of 10^{9}-$10^{10}\mathrm{n}_{eq}\cdot\mathrm{cm}^{-2}$ per year [5].

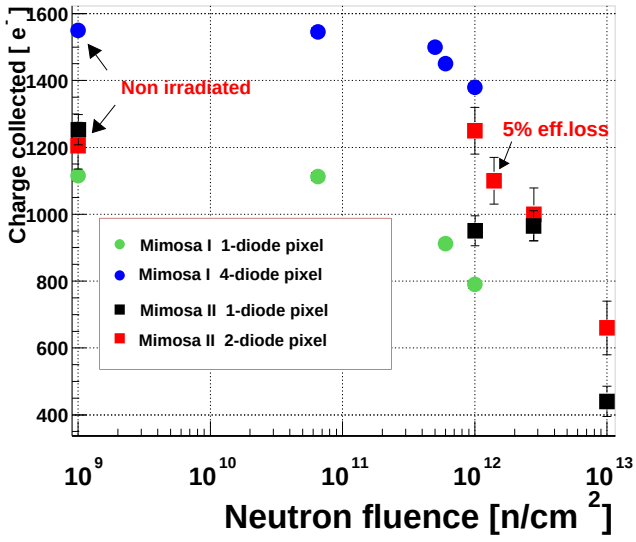

Figure 7: Variation of the signal charge collected with MIMOSA-1 (for 1 and 4 diodes per pixel) and -2 (for 1 and 2 diodes per pixel) as a function of the fluence. One of the MIMOSA-2 sensors exposed to $\sim 10^{12}\mathrm{n}_{eq}\cdot\mathrm{cm}^{-2}$ was tested at the CERN-SPS, where it exhibited ~ 5 % loss in detection efficiency.

6 First real scale prototype

The first real scale sensor (MIMOSA-5) was fabricated in 2001. Made of 10^6 pixels (17x17 μm^2 wide), it was thinned down to 120 μm. Tests performed at the CERN-SPS showed that the sensor reproduces the tracking performances of the small prototypes rather well (e.g. > 99 % detection efficiency, single point resolution of ~ 1.7 μm). Moreover, the average gain dispersion over the sensor surface was of the order of a few per-mill only. The results are summarised on figure 8, where they are compared to those obtained with MIMOSA-1, which was manufactured with the same fabrication process. One observes that despite the twice larger noise of MIMOSA-5 (a direct consequence of the large number of pixels read out serially), the tracking performances of both sensors are similar.

These achievements provide strong support to the feasibility of a light and very granular LC vertex detector with CMOS sensors.

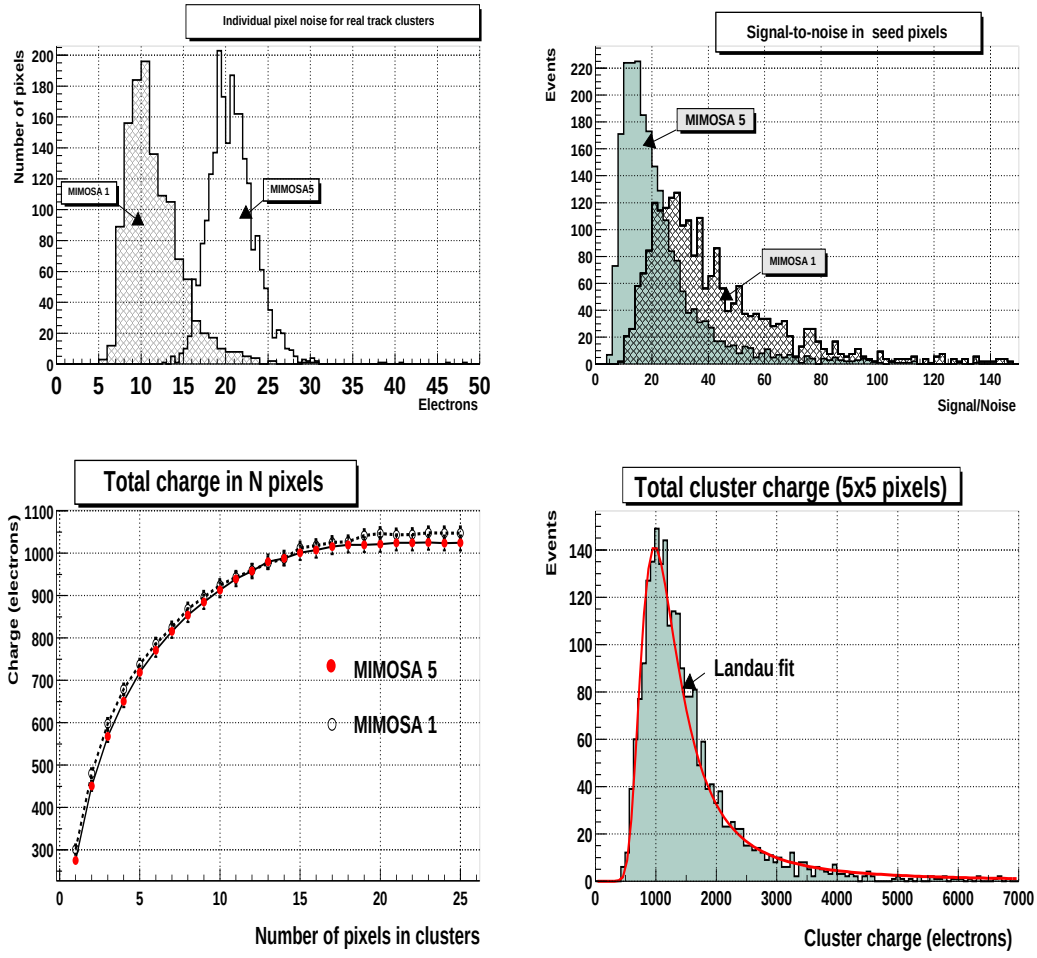

Figure 8: MIMOSA-5 test results, compared those of MIMOSA-1. The top figures show the pixel noise (left) and the seed pixel signal-to-noise ratio (right). The bottom figures display the signal charge as a function of the cluster multiplicity (left) and the cluster total charge distribution (right).

7 First prototype with integrated data processing and column parallel read-out

The fast read-out of several hundred million pixels constituting a LC vertex detector requires grouping the pixels in columns read out in parallel, with data sparsification integrated on the sensor substrate. The recently fabricated MIMOSA-6 chip was designed (in collaboration with DAPNIA-Saclay) in this perspective. It features 30 columns of 128 pixels ($28\mu m$ pitch) read out in parallel. Each pixel includes charge amplification and delivers a signal expressing the difference between the charges collected in two consecutive frames [6]. The charge difference is discriminated in a micro-circuit integrated at the end of each column (see Figure 9).

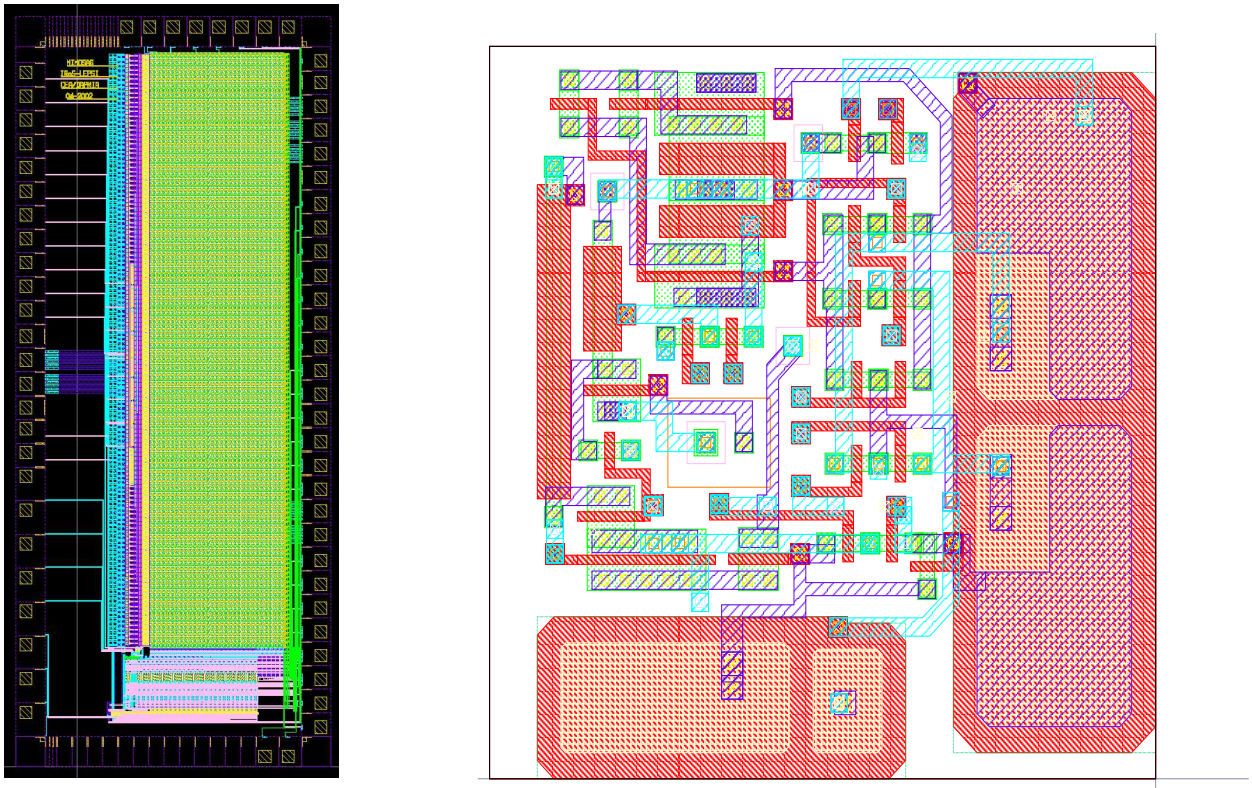

Figure 9: MIMOSA-6 global design (left) and individual pixel layout (right). The latter exhibits close to 30 transistors and two 90 fF capacitors (on the right pixel edge) where the signal charge of two consecutive frames is stored before being sent to the column exit for subtraction and discrimination.

Tests are under way. A preliminary study of the analog and digital parts, each isolated from the rest of the micro-circuits, shows that they work as expected. More studies are needed to conclude on the complete operation performances of the sensor.

8 Achievment summary

Six consecutive CMOS sensor prototypes were fabricated since the start of the development (see Table 1). In a first stage of the R&D, the viability of the detection technique was assessed, comforting the perspective of realising a vertex detector of a future Linear Collider based on this new technology.

prototype	year	fab. process	epi. thickness	pitch	nb(metal lay.)	peculiarity
MIMOSA1	1999	AMS $0.6\mu m$	$14\mu m$	$20\mu m$	3M	thick epitaxy
MIMOSA2	2000	MIETEC $0.35\mu m$	$4.2\mu m$	$20\mu m$	5M	thin epitaxy
MIMOSA3	2001	IBM $0.25\mu m$	$2\mu m$	$8\mu m$	3M	deep sub-μm
MIMOSA4	2001	AMS $0.35\mu m$	0 !	$20\mu m$	3M	low dop. substrate
MIMOSA5	2001	AMS $0.6\mu m$	$14\mu m$	$17\mu m$	3M	real scale
MIMOSA6	2002	MIETEC $0.35\mu m$	$4.2\mu m$	$28\mu m$	5M	column // r.o. & integ. spars.

Since Autumn 2001, further important steps were achieved: i) excellent tracking performances were obtained with a manufacturing process without epitaxial layer; ii) the tracking performances observed with small prototypes were reproduced with real scale, 10^6 pixel large, prototypes, thinned down to 120 μm; iii) the sensor tolerance to neutron irradiation was found to fullfil comfortably the LC requirements; iv) the first chip with data sparsification integrated on the sensor in a column parallel architecture aiming to meet the LC read-out speed requirements was fabricated and is being tested.

9 Outlook

The main goal of the next series of sensor prototypes is to achieve a read-out speed adapted to the expected occupancy induced by beamstrahlung $e^{\pm}$. Taking into account various uncertainties affecting the estimates of the background magnitude, a read-out time of $\lesssim 25$ μs is a valuable goal for layer 1, while layer 2 can be safely read out in 100 μs, and layer 3-5 can easily be read out in 200 μs.

Besides designing fast signal processing micro-circuits integrated on the sensor, the R&D of the coming years will also address important system integration issues, such as data acquisition system, sensor thinning, mechanical support and cooling. Finally, the tolerance to ionising radiation will be further investigated, though not crucial for the LC application.

Development guide lines for some of these issues are listed hereafter.

9.1 signal processing architectures *(at IReS-LEPSI, DAPNIA)*

The rather wide range of frame read-out speeds to achieve (i.e. typically from $\lesssim 25\mu s$ to $\gtrsim$ 200 μs), depending on the detector layer concerned, spontaneously pleads for two alternative ways of treating the signal. For the outer layers, the signal may be read-out $\gtrsim 6$ times per train (i.e. every $\sim$ 150 μs) and stored in 6 capacitors inside each pixel. The pixel read-out would then occur during the 200 ms separating consecutive beam trains. Sensors adapted to this read-out structure are being designed and will be sent for fabrication by the end of June. For the inner most layer, and perhaps for the second layer as well, another approach is being considered, allowing signal sparsification within the train duration. This architecture follows the strategy implemented in the MIMOSA-6 prototype (see section 7).

The designs include power dissipation and material budget considerations, the latter coming from the width of the side band of the sensors necessary for hosting part of the integrated electronics (e.g. ADC, memories).

Based on the design and fabrication of 2 to 3 sensors per year, the goal is to produce a first real scale prototype (i.e. $\gtrsim 1$ cm^2 array), made of $\lesssim 1$ million pixels and read out in 100-200 μs, by year 2005.

9.2 power dissipation *(at DESY, Hamburg University, NIKHEF)*

The VFE being integrated inside, or nearby, the pixels, substantial power dissipation is expected inside the active volume of the vertex detector. Based on the power consumption of the MIMOSA-6 prototype, a total dissipation of the order of 500 W is expected from the complete detector. This questions the need of active cooling.

In order to minimise the cooling system influence in terms of material budget, pulsed powering is envisaged, taking advantage of the time structure of the beams: $\sim$ 1 ms long trains separated by 200 ms. The duty cycle of the collider (1/200) is however unlikely to be fully usable[3], due to the time needed by the pulses to slow down once they are switched off, and to the stabilisation period required once the circuits are switched on (besides possible pick-up noise problems). It is nevertheless likely that power dissipation will only be substantial during a few ms inbetween trains, making a reduction factor of 20-50 w.r.t. the instantaneous power dissipation plausible. The average power dissipation would therefore only amount to a few tens of watts. This magnitude should not require a cooling system introducing significant material in the active volume of the detector.

Pulsed powering is still to be proven. It will be investigated with the MIMOSA-5 prototype. In parallel, the amount of cooling needed for each detector layer will be simulated and light cooling systems will be designed. Among the latter, the possibility to introduce capillary (i.e. warm) cooling inside the silicon substrate is particularly appealing, though very challenging.

9.3 mechanical support *(at DESY, Hamburg University, NIKHEF)*

In order to exploit the high granularity provided by the sensors, a major effort is needed to keep the material budget of each detector layer at a very modest level. The goal is to keep each

[3] independently of the detection technique considered

of them below 0.1 % radiation length. Physics simulation are, and will be, done in order to quantify the consequence of a given material budget and the sensitivity to physics processes.

Studies of elementary ladder structures have started. A first milestone would consist of a ladder prototype equivalent to $\gtrsim$ 0.25 % radiation length, allowing to spot the intrinsic difficulties of this sort of design. The foreseen time scale needed to achieve such a prototype, grouping 5 individual sensors, each made of 1 million pixels, on a single ladder, is 2-3 years.

9.4 sensor thinning *(via IReS-LEPSI, ...)*

The goal is to thin the sensors down to 50 μm or less. Up to now, 3 MIMOSA-5 wafers were thinned down to 120 μm and consecutively diced in industry. The chip performances are very satisfactory, as summarised in section 6.

A procedure based on chemical etching is being studied at the National Center of Microelectronics (University of Barcelona, Spain), which should allow to achieve thicknesses below 50 μm on most of the sensor surface. Alternative techniques, where the full wafer is being thinned to the ultimate thickness, are also being considered (as for the STAR vertex detector upgrade at RHIC).

9.5 sensor stitching *(at IReS-LEPSI, DAPNIA, ...)*

The perspective of ladders made of stitched, reticle size wide, sensors is definitely appealing since it minimises the sensor material budget. Since recently, industry offers such stitching possibilities, where neighbour sensors are separated by a <1 μm wide band. However, stitching will only be adequate if the sensor componant yield is good enough. This would, for instance, not be the case with MIMOSA-5, where the sensor yield was about 30 %, and the largest fully operational ladder was made of 3 consecutive sensors. Mechanical supports are therefore to be studied, with and without stitched sensor arrays, until the production yield is better understood.

9.6 radiation tolerance *(at IReS-LEPSI, ...)*

A few MIMOSA-1, -2, -4 prototypes were exposed to intense ionising radiation sources (e.g. 10 keV X-Ray source at CERN). First test results exhibit charge losses for a few 100 kRad exposure. Though this result indicates that the sensors would stand several years of running at a Linear Collider, the origin of the phenomenon will be investigated.

These studies include measurements inside the sensor structure (i.e. SIMS after depassivation), design and fabrication of isolated elementary structures suspected to change characteristics after ionising irradiation, 3D simulations of the irradiation effect on the sensor, studies of the influence of temperature and time on irradiated sensors, etc.

10 Conclusion

Since the start od the development, major requirements in terms of spatial resolution and radiation tolerance for a LC experiment were met with CMOS sensors: detection efficiency > 99 %, single point resolution ~ 1.5 μm, double hit resolution ~ 30 μm, neutron radiation tolerance $\lesssim 10^{12} \mathrm{n}_{eq} \cdot \mathrm{cm}^{-2}$ and ionising radiation tolerance > 100 kRad.

The most important remaining issues, such as frame read-out speed and system integration aspects related to data flow and material budget (i.e. DAS, mechanical support, power dissipation, operating temperature) are being adressed and are subject of a provisional ladder prototype expected to be realised within 2-3 years.

The best compromise between spatial resolution, power dissipation and read-out speed will be guided by detailed physics simulations addressing several fundamental processes where the vertex detector performances should play a central role (e.g. $e^+e^- \rightarrow t\bar{t}, t\bar{t}H, ZH, WW$).

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