Henri Videau
Hamburg Sept

Status of the W-Si calorimeter hardware design (since Obernai)

To optimize the hardware design needs a lot of software development and optimization.

In Obernai we had presented:

- a clear geometry for mechanical structure read out.
- a quite clear design of the mechanical structure
- ideas on the way to get the signals out ***
- concepts on the front end electronics **
- nothing on the acquisition *

- Review of the geometry — modules — # of layers — read out

cooling < 300 W in calorimeter bulk
< 12 kW in 1 barrel stave electronics
(if not pulsed - calibration)

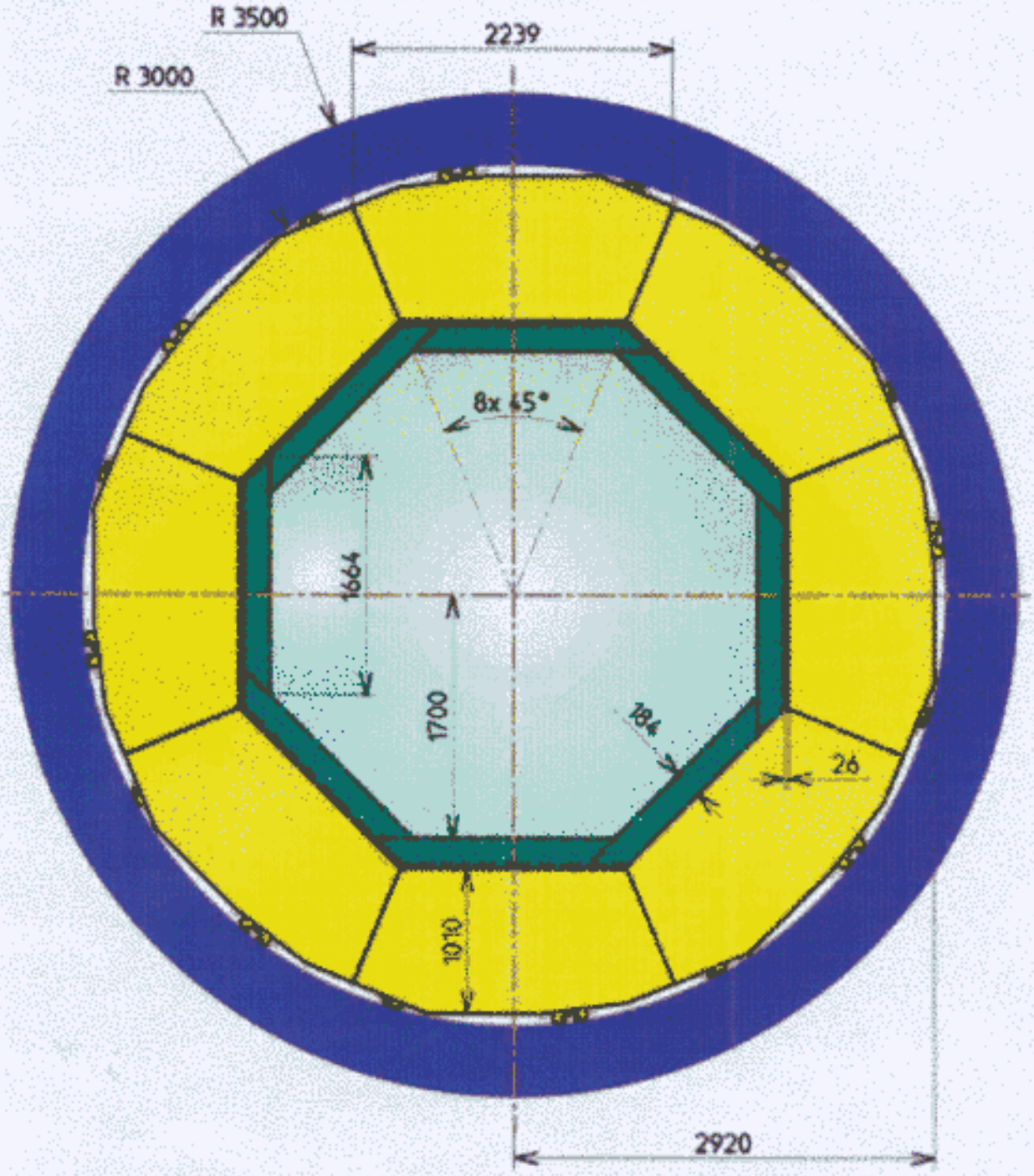
the installation.
View of the cables path.

- modification in the structural design.
1 tungsten layer out of 2 supports the silicon

- the structure of the detector slab -
the silicon wafers
the "S10" interface — prototype being realised
the flat cable
the front end board

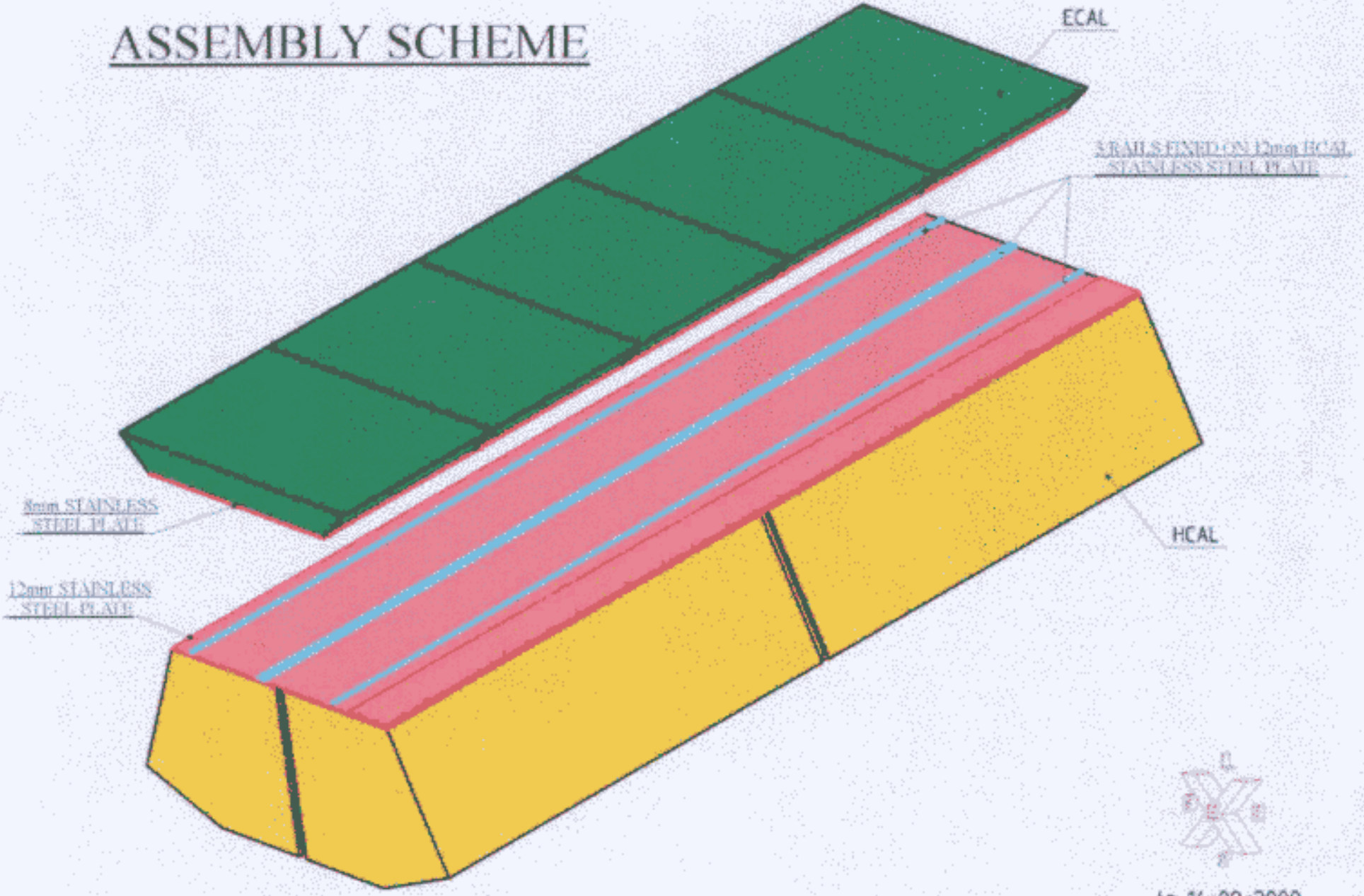
- the front end electronics — prototype chip
similar to Opera
$\frac{\text{noise}}{\text{MIP}} \sim \frac{1}{10}$ cross talk OK
number of chips / slab ~ 8 local threshold
analogic buffer
a pile (40) of slabs for 1 ADC 40 × 8 × 140 channels
Example of solution considered : "token ring" 700 ADC's
few cables -

8 MODULES VERSION 00



le 16-11-1999

ASSEMBLY SCHEME



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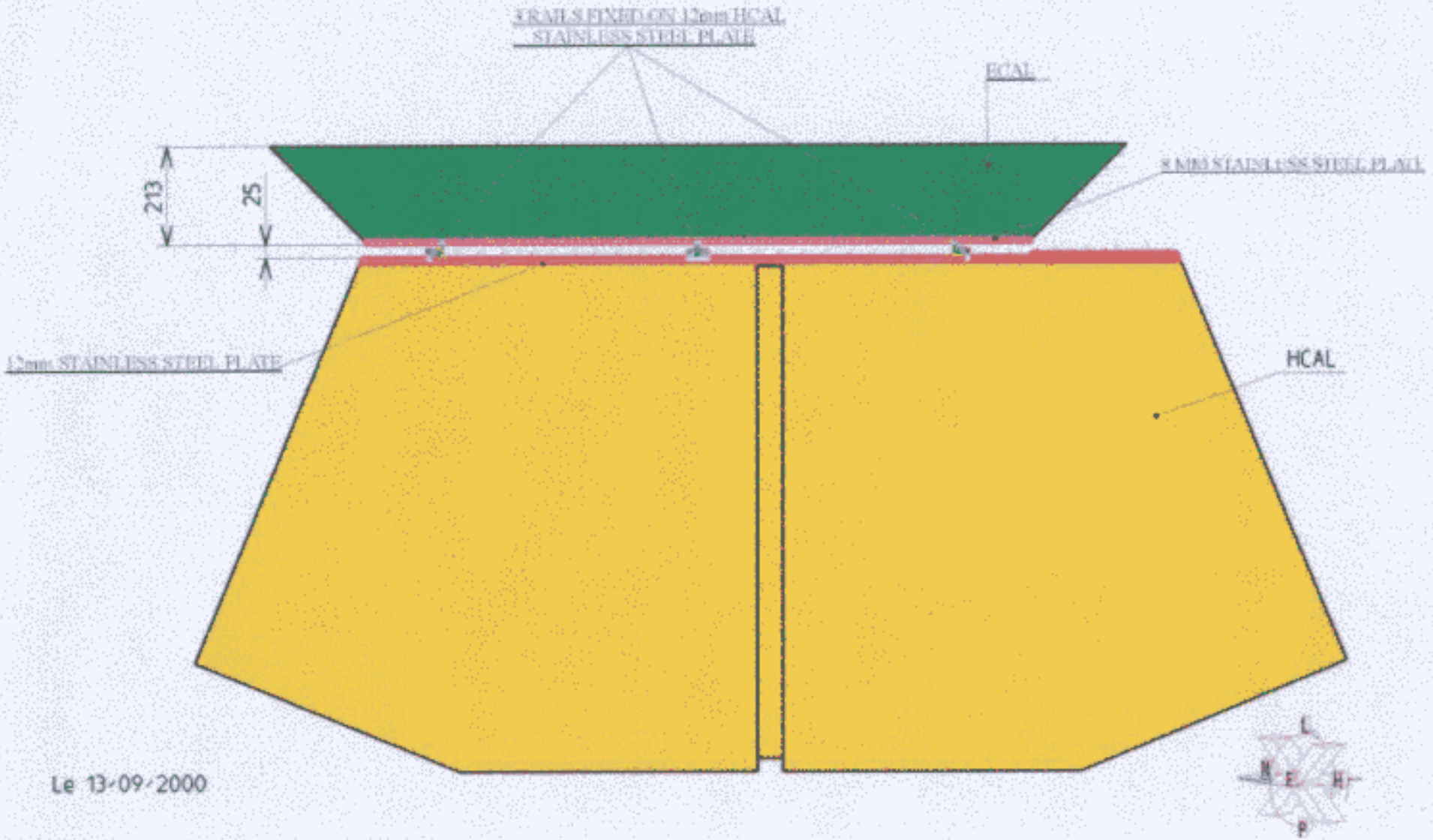

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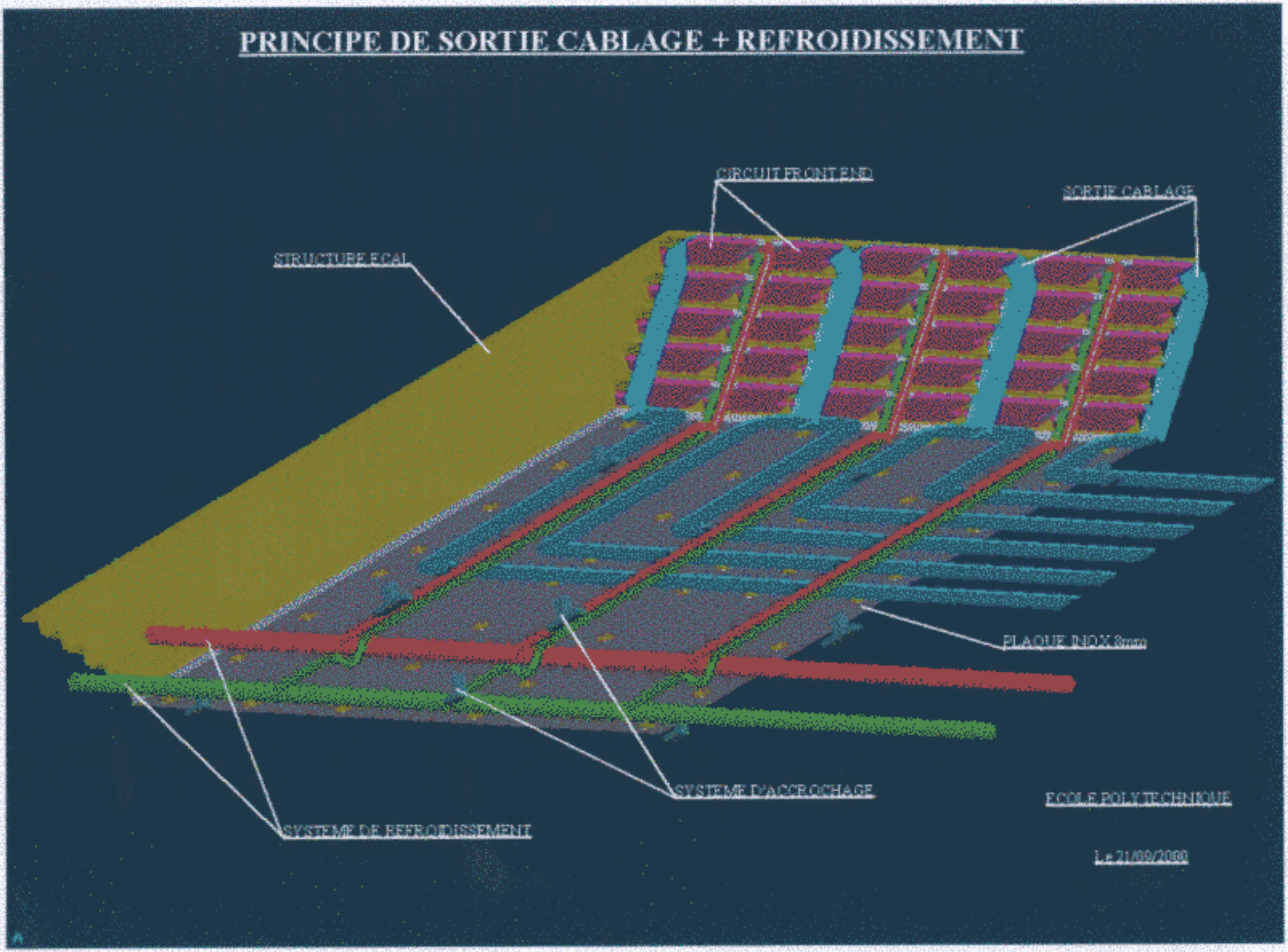
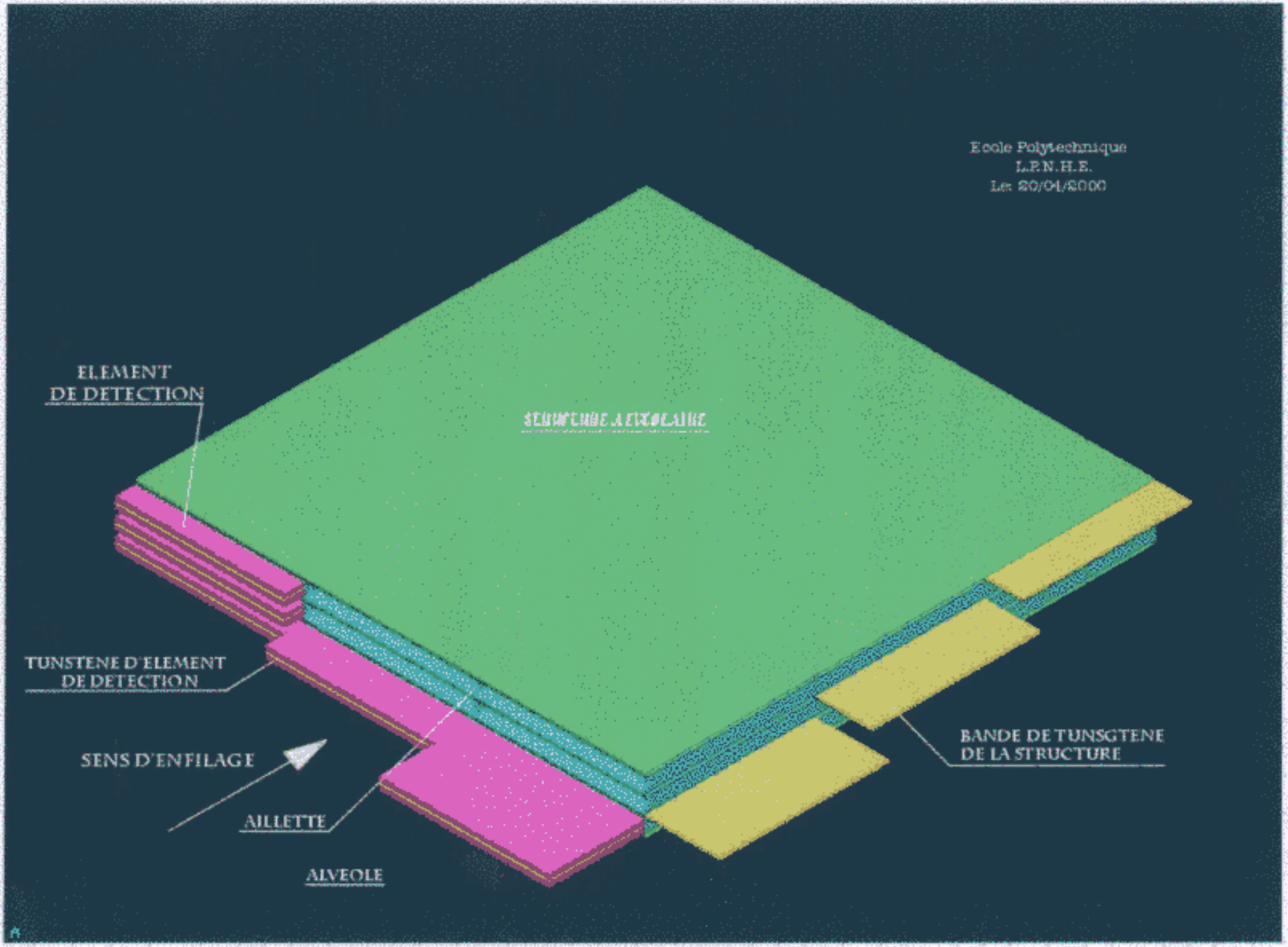
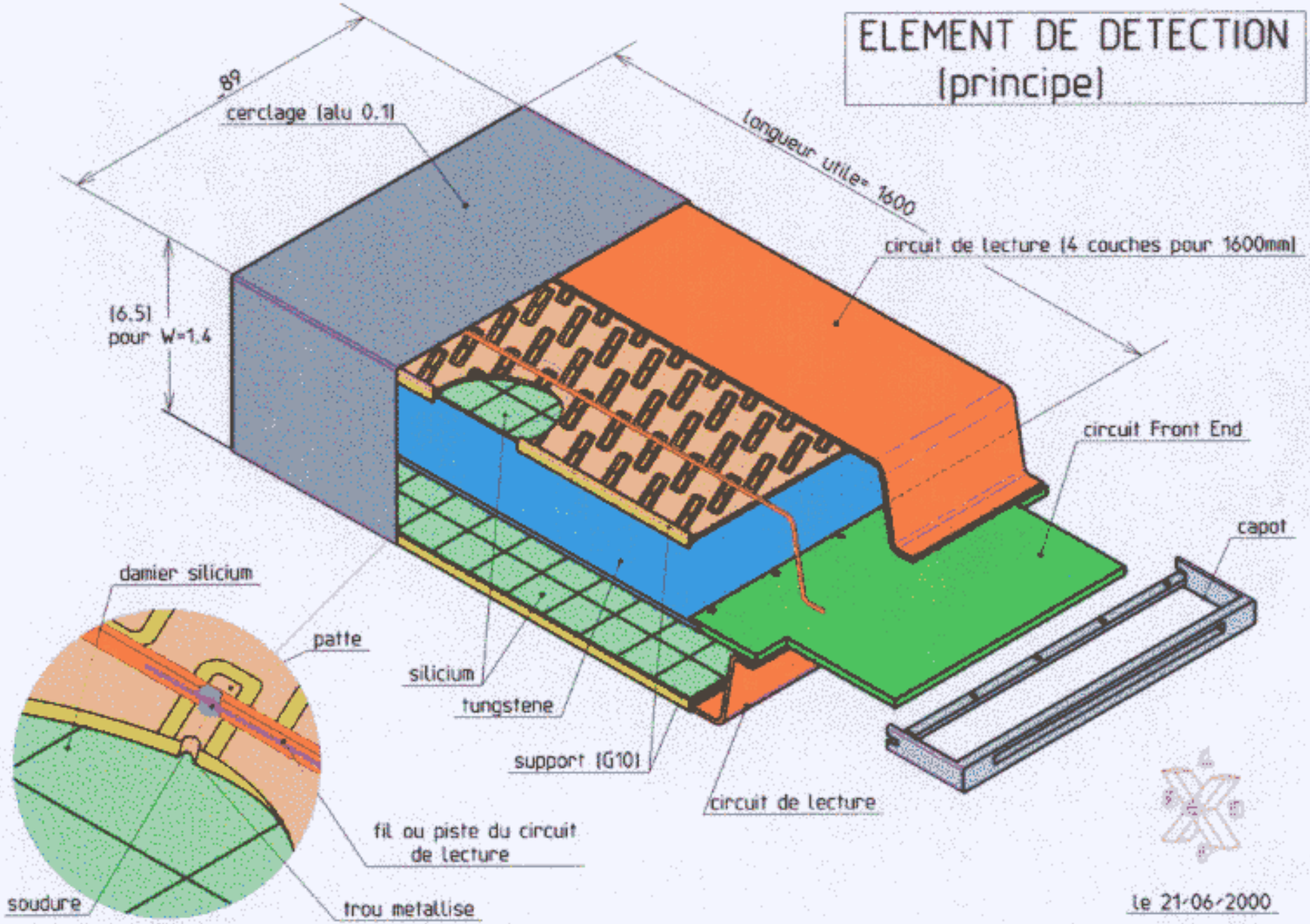
PRINCIPE DE SORTIE CABLAGE + REFROIDISSEMENT




Ecole Polytechnique
L.P.N.H.E.
Le: 20/04/2000
ELEMENT
DE DETECTION
TUNSTENE D'ELEMENT
DE DETECTION
SENS D'ENFILAGE
AILLETTE
ALVEOLE
BANDE DE TUNSGTENE
DE LA STRUCTURE

ELEMENT DE DETECTION (principe)



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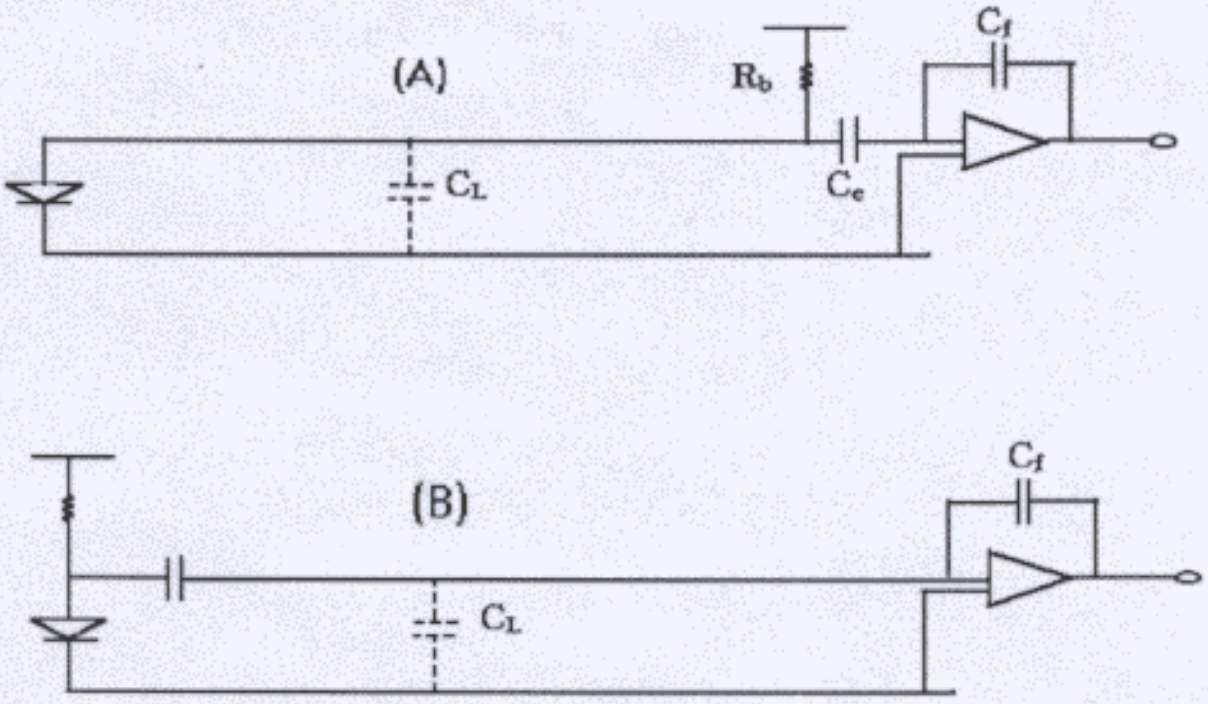
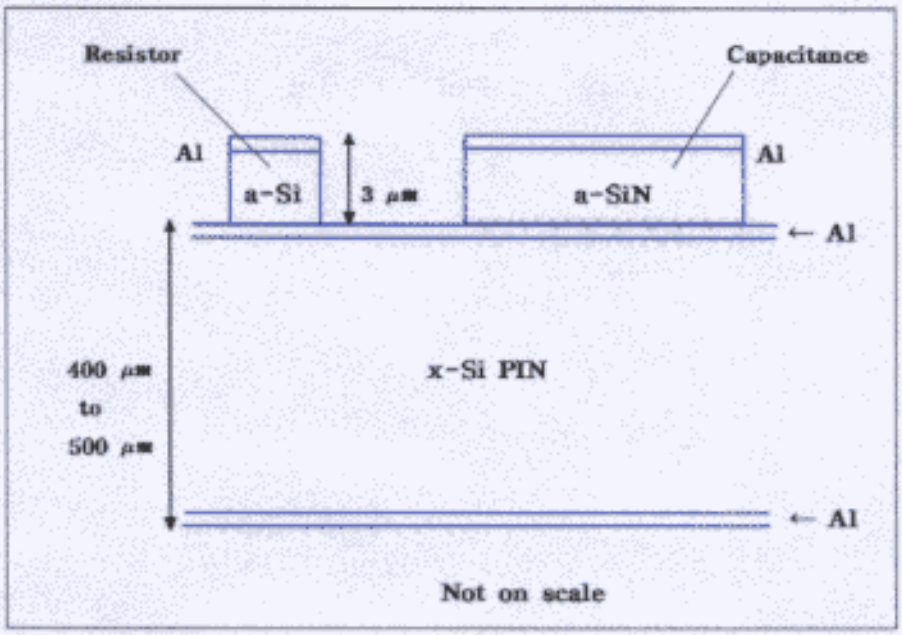
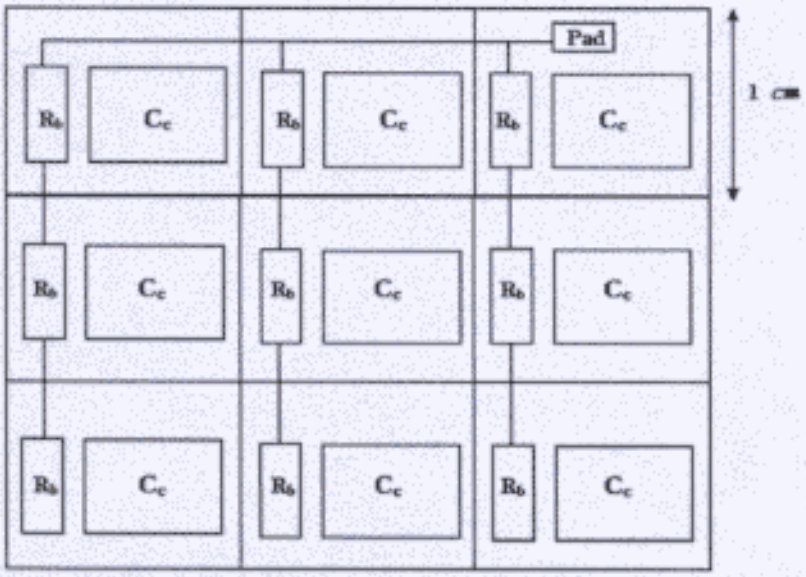


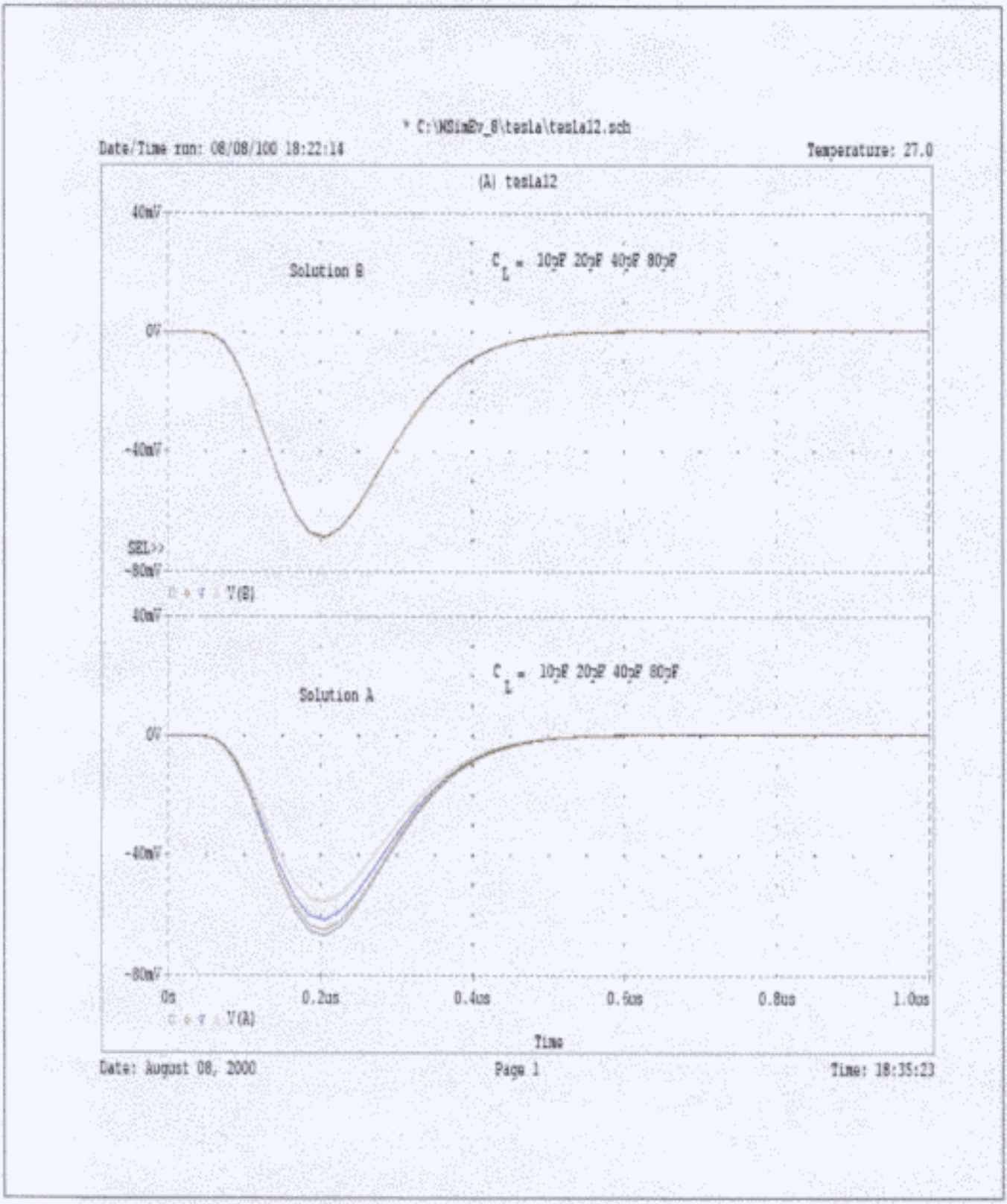
The two possibles solutions for the coupling capacitance and resistance.



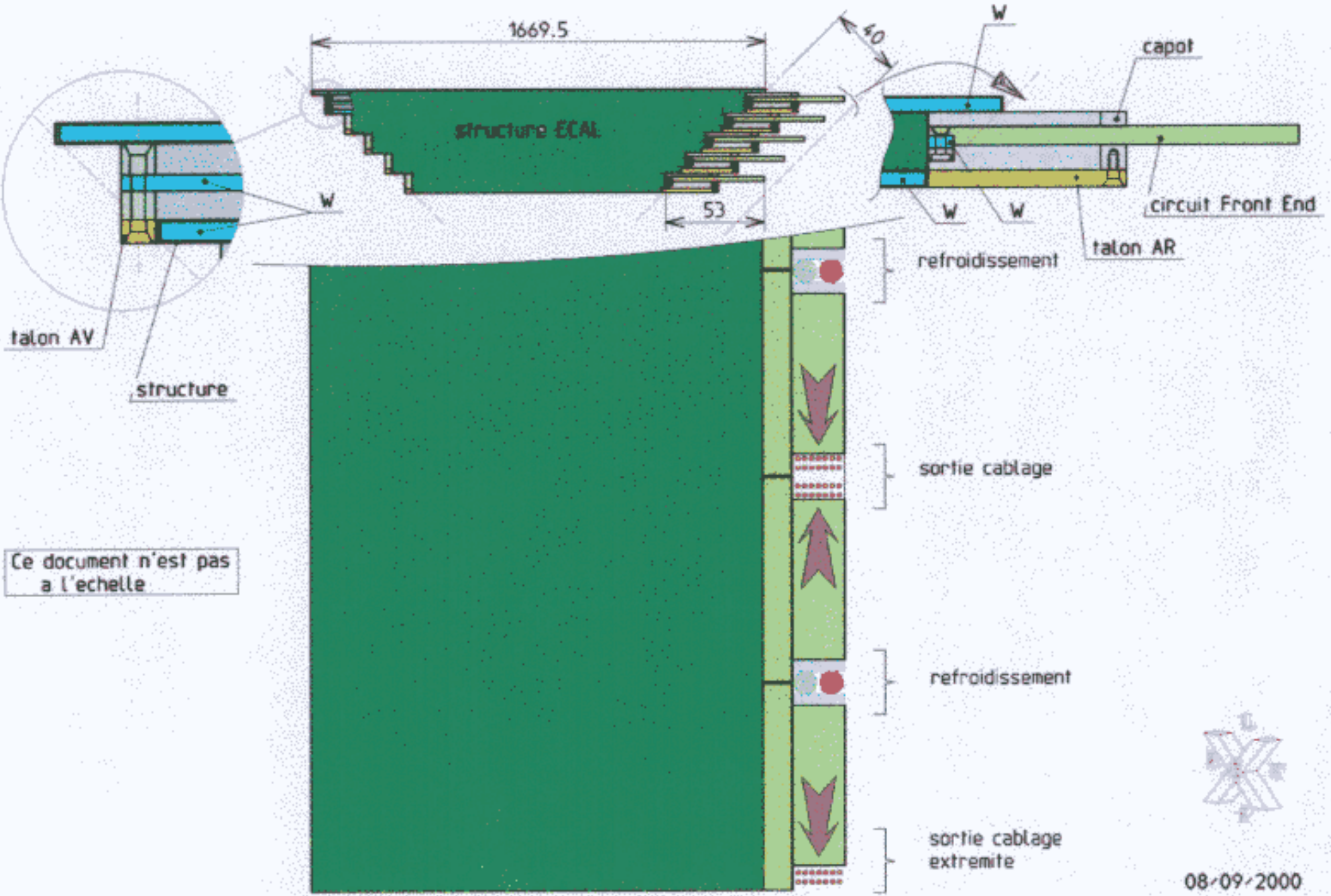
Schematic view of the PIN diode with the amorphous silicon deposited.



The arrangement of the Silicon wafer, for the example of 3x3 diode wafer.



Results of the SPICE simulation.



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a l'echelle

08/09/2000