1.2 VERTEX DETECTOR SYSTEM

- VALUABLE INPUT FROM M. BATTAGLIA, M. CACCIA, R. HAWKINGS M. WINTER, S. XELLA, ...

1.2.1 INTRODUCTION

PHYSICS MOTIVATION

PERFORMANCE GOALS

MACHINE-RELATED ISSUES

DETECTOR FEATURES

1.2.2 TECHNOLOGY OPTIONS

CCD & CMOS PIXELS

HYBRID PIXELS

1.2.3 DETECTOR PERFORMANCE

GENERIC PERFORMANCE [VTX + TRK]

COMBINED PERFORMANCE [JET SELECTION / ENERGY MEASUREMENT ...]

PHYSICS EXAMPLES [REFS]

1.2.4 R & D

CCD
CMOS PIXELS
HYBRID PIXELS

1.2.5 COST ESTIMATE

CCD
CMOS PIXELS
HYBRID PIXELS

} TABLE IN DETECTOR SECTION

+ DESY 123 NOTES:

1 FOR EACH OPTION
GENERIC PERFORMANCE (EVOLVED FROM

Chapter 1

Tracking System

1.2 VTX vertex detector system

1.2.1 Introduction

LEP, SLC and the Tevatron have established the importance of vertex detectors in understanding the physics accessible at high energy colliders. At TESLA, both precision measurements and particle searches set stringent requirements on the efficiency and purity of the flavour identification of hadronic jets since final states including short-lived b and c-quarks and τ leptons are expected to be the main signatures. High accuracy in the reconstruction of the charged particle trajectories close to their production point must be provided by the tracking detectors, in particular by the Vertex Tracker located closest to the interaction point, in order to perform the reconstruction of the topology of secondary vertices in the decay chain of short-lived heavy flavour particles in a complex environment. Low efficiency would be unacceptable due to the small event samples, and low purity would generally be unacceptable due to backgrounds.

Experience at LEP and SLD shows the way forward. Jet flavour identification can based primarily on the topological vertex structure in the jet, since this in principle allows most of B and D decay modes to be detected. By aiming for good sensitivity down to decay times short compared with the mean lifetimes, high efficiencies may be realised. Distinguishing clearly between b and c jets requires additional information. This comes from the secondary and tertiary vertex topology, the charged decay multiplicity and the vertex mass, after applying corrections for missing neutrals.

As well as tagging b and c jets, the vertex charge (if non-zero) can distinguish b from $\bar{b}$, c from $\bar{c}$. This again requires sufficient precision to distinguish between all the decay tracks and those coming from the primary vertex.

Cases where leptons (and hence neutrinos) are absent from jets are particularly valuable for precise jet energy measurement. Due to the prevalence of converted γs in jets, it is important to track detected electrons in through the layers of the vertex detector to establish if they were really produced in semileptonic B or D decays. For such decays, the jet energy measurement may be improved substantially by extending the procedure used for the p_T-corrected mass, allowing a correction for the transverse

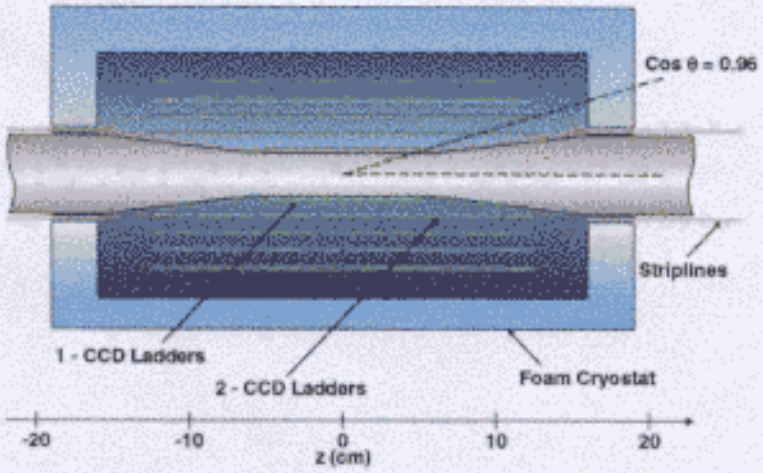


Figure 1.1.1: Cross-section of CCD-based vertex detector

pipe complemented by forward crowns and disks extending the polar acceptance to small angles following a solution successfully adopted in the DELPHI Silicon Tracker. The three barrel layers have a polar acceptance down to $|\cos\theta| = 0.82$. At lower angles, additional space points are obtained by extending the barrel section by a forward crown and two disks of detectors providing three hits down to $|\cos\theta| = 0.995$. The transition from the barrel cylindrical to the forward conical and planar geometries optimises the angle of incidence of the particles onto the detector modules in terms of the achievable single point resolution and the multiple scattering contribution. Overlaps of neighbouring detector modules provide an useful mean of veryfing the relative detector alignment using particle tracks from dedicated calibration runs taken at Z^0 centre-of-mass energy.

The vertex detector will be one of the most high-tech parts of the TESLA detector. Along with other elements of the inner detector system (everything inside the TPC inner radius) it will potentially need periodic maintenance and upgrades. For this reason, there needs to be a clear plan for carrying out such operations without a major impact on other delicate equipment such as the final focus magnet system. A procedure for avoiding such interference has been devised, and is based on a strategy of rolling the TPC along the beamline by about 5 m, to provide access to the inner detector. This is discussed fully in Chapter ??.

1.2.2 Technology options and conceptual designs

1.2.2.1 CCD and CMOS pixels

Both these options rely on a charge-collection region of thickness ~ 20 μm, which is partly depleted and in part of which the charge is collected by diffusion, as indicated

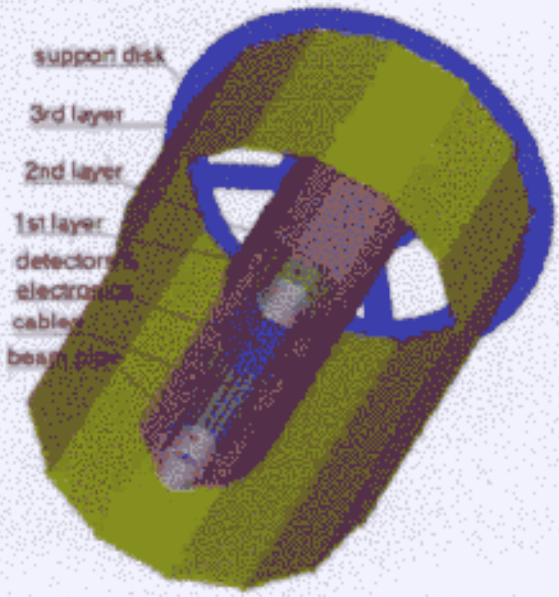


Figure 1.1.2: General layout of the hybrid pixel-based Vertex Tracker

in Fig 1.2.1. These features lead to coordinate measurements which are precise and robust (relatively free of effects of δ electrons and fluctuations in charge deposition) in both the $r\phi$ and z components down to small polar angles. Use of small pixels ($\sim$ 20 μm square) permits coordinate measurements with precision $\sim$ 3 μm by interpolation.

The essential difference between these two options is the method of sensing the signal after collection. The CCD design shown in Fig 1.2.2 restricts the material within the fiducial volume to the thin silicon alone, patterned by the IC processing which firstly creates the potential wells which define the pixel matrix, and secondly permits the stored charges to be shifted along the columns in the z direction to the readout ICs. The CCDs are attached to 'ladder blocks' and tensioned so as to achieve the required mechanical stability (stability on the sagitta of $< 5\mu$m). These devices with their inactive pixels dissipate very little power in the fiducial volume, and can be cooled by a gentle flow of nitrogen gas. Outside this volume, as well as the mounting blocks, each ladder carries a driver IC and a readout IC (see Fig 1.2.3). The driver chip generates the waveforms which shift the stored signals row by row down the device. The readout chip receives the analogue signals from all columns in parallel as they are shifted out of the active area to buffer amplifiers. This chip incorporates analogue-to-digital conversion, correlated double sampling, data sparsification by a sequence of pixel- followed by cluster-comparators, and data storage.

Some of the key parameters associated with this detector design are listed in Table 1.2.2.1. The material budget for this option is shown in Fig 1.2.4. Processed data are stored in the readout ICs during the bunch train. As events are found by the trigger processors during the inter-train periods of 200 ms, the associated vertex detector data are read out via optical fibres (just one fibre at each end of the detector).

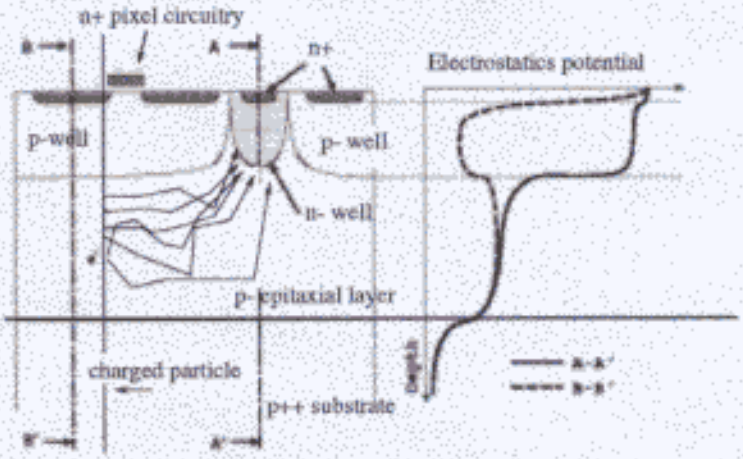


Figure 1.2.1: Charge collection within a CMOS pixel

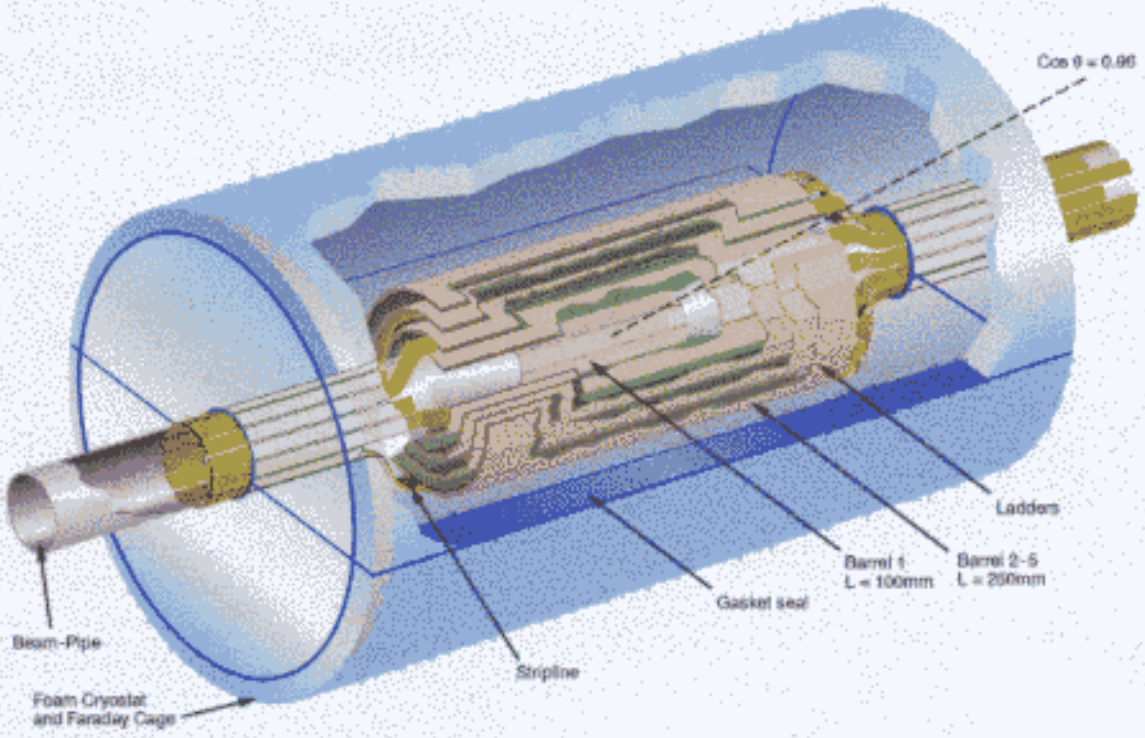


Figure 1.2.2: General layout of CCD-based vertex detector

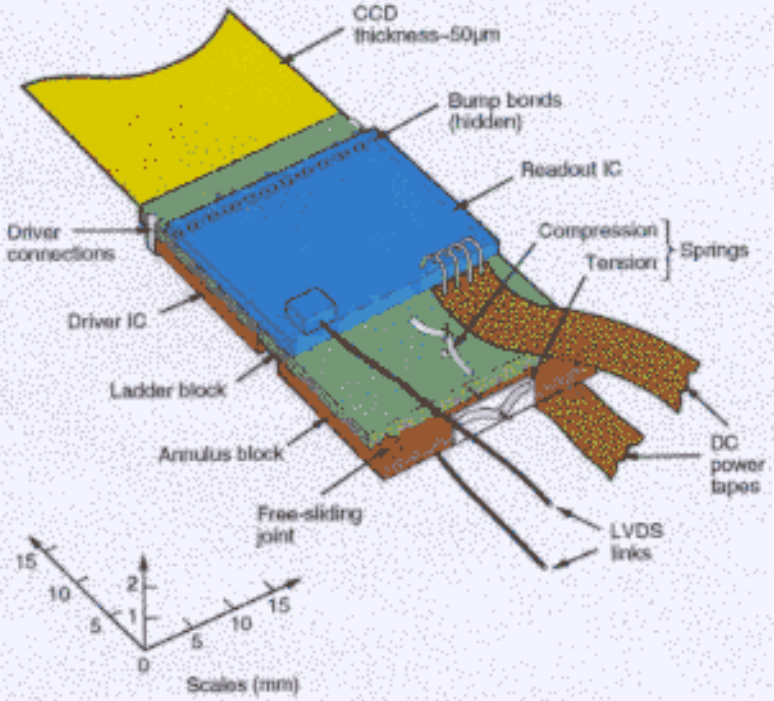


Figure 1.2.3: Layout of components at end of ladder in CCD-based detector - stretched silicon option

Figure 1.2.4: Material budget for CCD-based detector, as function of polar angle *to come soon!*

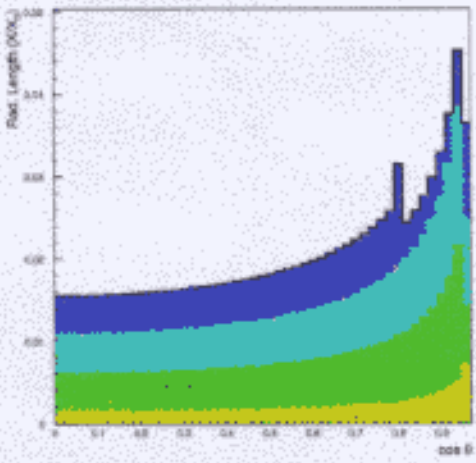


Figure 1.2.5: Material budget for Hybrid Pixel-based detector, as function of polar angle

stamping (25 ns) and sparse data scan read-out, and the operability of hybrid pixel detectors exposed to neutron fluxes well beyond those expected at the linear collider.

The detector resolution requirement can be accomplished by sampling the diffusion of the charge carriers generated along the particle path and by interpolating the signals of neighbouring cells using analog read-out. This requires a sampling pitch of not more than 25 μ that can be achieved by exploiting the capacitive coupling of neighbouring pixels and arranging a read-out pitch n times larger than the implant pitch with interleaved pixels. Recent tests on a microstrip sensor, with 200 μm read-out pitch, have achieved a 10 μm resolution with three interleaved strip layout [?]. Similar or better results are to be expected for a pixel sensor, taking into account both the lower noise because of the intrinsically smaller load capacitance and the charge sharing in two dimensions, setting the target single point resolution to ≤ 7 μm. Reducing the read-out density, without compromising the achievable space resolution, is also beneficial to limit the power dissipation and the overall costs.

The requirements in terms of material budget can be fulfilled by adopting 200 μm thick detectors and back-thinning of the read-out chip to 50 μm, corresponding to 0.3 % X_0 of a radiation length, and a light support structure. The estimated material budget corresponds to 1.6% X_0 for the full tracker. The present concept for the mechanical structure envisages the use of diamond-coated carbon fiber detector support layers acting also as heat pipes to extract the heat dissipated by the read-out electronics uniformly distributed over the whole active surface of the detector. Assuming a power dissipation of 40 μW/channel, the total heat flux is 530 W, corresponding to 1750 W/m^2, for a read-out pitch of 150 μm. Preliminary results from a finite element analysis show that pipes circulating liquid coolant must be placed every 5 cm along the longitudinal coordinate except for the innermost layer where they can be placed only at the detector ends to minimise the amount of material. Signals can be routed along

This design philosophy, while it minimises the material in the tracking volume, imposes the need for an environment in which efficient transfer of signal charge in the CCD buried channel (by as much as 12.5 cm) is established and preserved throughout the life of the detector.

In the case of the CMOS pixels, the plan is also to measure the signal charge in every pixel, on a row-by-row basis. However, the charges are now sensed where they are collected, and the rows of sensing transistors are successively switched on by means of gating lines controlled by a shift register. The analogue signals are then transmitted to the edge of the active area by means of a set of readout lines, one per column. From this point, the signal processing can proceed approximately as for the CCD option. There are additional complications associated with the reset of the sensing circuits. To achieve the required noise performance and readout rate, it may be necessary to introduce logic for correlated double sampling inside the unit cell; space for this is probably available without enlarging the pixels. Whether such devices can be constructed with the required performance in the full length needed for an unsupported-silicon detector architecture is an open question. If not, a solution (which would substantially increase the material budget) would be to tile a substrate (probably diamond) with a number of these devices, so as to make up the full ladder length. In this case, the planned cooling (by conduction along the substrate) would need to take account of the full power dissipation of the readout sections of the chip. Here there are many open issues to be investigated, including the possible use of pulsed power.

Layer	Radius	CCD L×W	CCD size	Ladders and CCDs/ldder	Row clock fcy & Readout time	Bgd * occupancy	Integrated bgd *
	mm	mm^2	Mpix			$Hits/mm^2$	Hits/Train $\times 10^{-3}$
1	15	100 × 13	3.3	8/1	50 MHz/50 μs	5.9	1165
2	26	125 × 22	6.9	8/2	25 MHz/250 μs	2.9	484
3	37	125 × 22	6.9	12/2	25 MHz/250 μs	1.1	276
4	48	125 × 22	6.9	16/2	25 MHz/250 μs	0.9	301
5	60	125 × 22	6.9	20/2	25 MHz/250 μs	0.6	251

Table 1.2.1: Key parameters of the CCD-based vertex detector design.

307 Mpix (SLD) → 799 Mpix (TESLA)

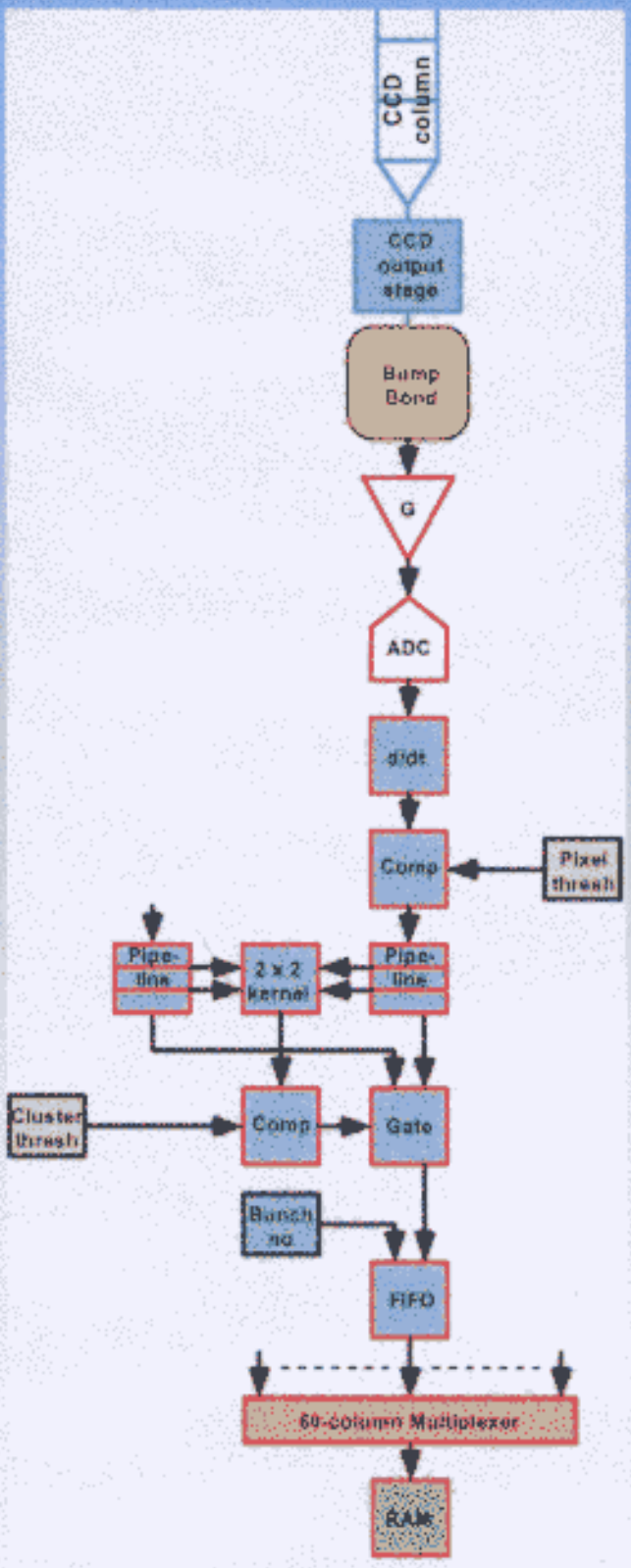
* Store ~ 15 MB / Train on detector
Between trains, each event → 2 MB via 2 optical fibres (one each end of detector)

1.2.2.2 Hybrid pixel option

Hybrid silicon pixel detectors have been developed and successfully applied to track reconstruction in high energy physics experiments in the last decade. In particular, DELPHI at LEP was the first collaboration adopting hybrid pixel sensors for a Vertex Tracker at a collider experiment [?]. Hybrid pixel sensors have been further developed for ALICE [?], ATLAS [?] and CMS [?] to meet the experimental conditions of the LHC collider. These R&D activities have demonstrated the feasibility of fast time

Column-parallel CCD signal-handling

- **Functionality of readout chip *(n.b. very preliminary ideas — more study needed)*:**



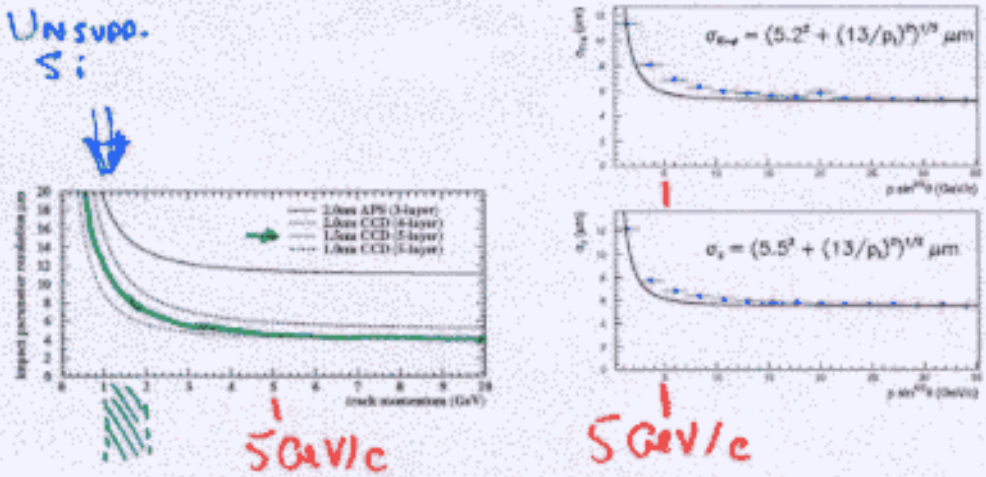


Figure 1.3.1: Track impact parameter resolution in $r\phi$ vs momentum, for $\theta_p = 90°$ (CCD (left) and hybrid pixels (right)) *(to be revised soon)*

ONE COMBINED, READABLE PLOT

1.2.3.3 Physics examples

Higgs branching ratios vs Higgs mass (text and figure from Marco)

Reconstruction of high energy events of type $e^+e^- \to W^+W^-$ with one leptonically decaying W and one to $c\bar{s}$ (Tim Barklow study).

1.2.4 Ongoing R&D programme

1.2.4.1 CCD

This detector, with 799 Mpixels is a reasonable evolution from the extremely successful SLD vertex detector of 307 Mpixels [7], which operated extremely reliably for several years in hostile background conditions. However, there are challenges which push the design well beyond the performance required for SLD.

In terms of the mechanical design, the most ambitious aspect is the move to stretched silicon, which reduces the layer thickness from 0.4% X_0 (achieved with excellent stability in SLD) to 0.06% X_0. This is the subject of an active R&D programme, the first fruits of which (obtained with a mechanical model comprised of thin glass plates instead of silicon) is shown in Fig 1.4.1. This indicates the stability achieved when the sliding ladder block was repeatedly disturbed and allowed to recover, as for example would happen in a real detector as result of temperature variations. For a modest spring tension ($\gtrsim 5$ Newtons) the stability in sagitta was around 3 μm, which would be entirely adequate. These studies are being extended to unprocessed then CCD-processed silicon, in place of the glass.

Regarding the CCDs, the active area of up to 125 × 22 mm^2 is standard for companies with at least 6 inch wafer processing. The column-parallel architecture is intrinsically simple, since the readout register is omitted. However, the layout of the

Technology Options

- If claims realized, happy situation of choosing between 3 high-performance options
- We will not burden TDR with the fine differences between these claims.
- For each, there may be decisive performance limitations or show-stoppers. [See R&D Sections]

CCDs	CMOS Pixels	Hybrid Pixels
• Neutron BGD • Readout: Column-parallel @ 50 MHz • ≤ 3 V Amplitude gates •	• 9μm, hence fst size, for fast, large area operation [If ≤ 2×12 cm², material budget for tilted Ass'y] • Pulsed power? [If not, material budget for cooling] •	• Precision with thin detector & charge interpolation • 2-bit resolution (& layer 1 radius) • Pulsed power? [If not, material budget for cooling] • . . . . .

* Material budget for adequate mech. stability?

ATLAS Vertex Detector & Silicon Trkr

10 years R&D, on verge of production

1999: "We'll tell you when we begin production"

Why care?

Vertex charge lost if 1 ambiguous low-mom trk between P.V. & (S.V./T.V.)

Photon conversions confuse category of no-lepton (hence no ν) jets

* Push sustained R&D for all options.

MARCO & I SUGGEST:
PERFORMANCE PLOTS ONLY FOR ONE OPTION (UNSUPP. Si CCD) WITH CLARIFICATION IN TEXT (p12)

R. HAWKINGS

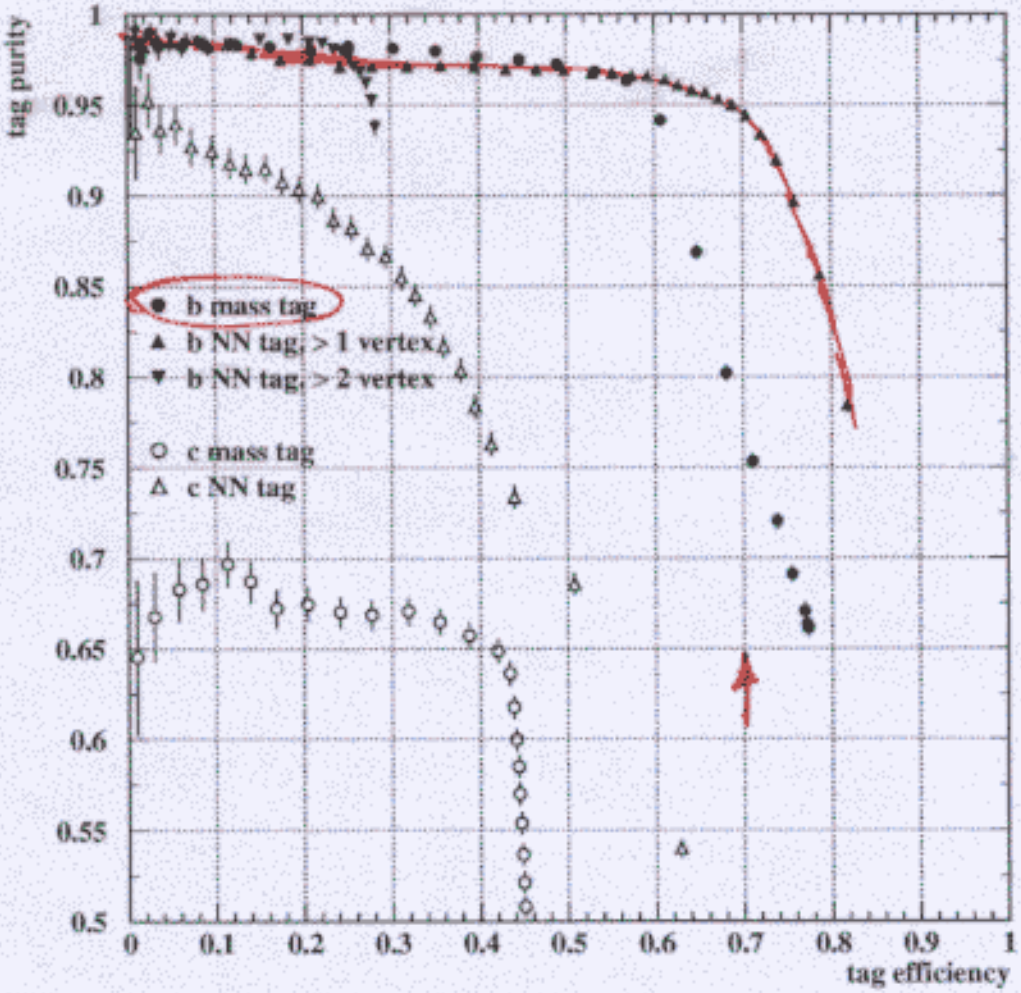


Figure 1.3.2: Efficiency and purity of b tag in Z^0 decays *(to be revised soon)*

the beam pipe and the end-cap disks to the repeater electronics installed between the Vertex Tracker and the forward mask protecting the Vertex Tracker from direct and backscattered radiation from the accelerator.

1.2.3 Detector performance for physics

1.2.3.1 Generic vertex detector performance

In this section, we discuss simulations for the CCD-based option, since this has the best-defined material budget, and also has the highest established performance in terms of precision over a wide range of incident angles, for devices of the dimensions needed for this application (tens of cm^2).

It must be emphasised that other options may eventually reach or exceed these performance figures. Furthermore, CCDs might be ruled out by unexpectedly large neutron or other hadronic backgrounds. This field remains wide open for ongoing R&D in a number of options. It is then to be hoped that the detector which is eventually installed will deliver at least the performance represented by these simulations.

The figure of merit for any pixel-based vertex detector can be expressed by the precision with which one measures the track impact parameter to the IP, separately in the $r\phi$ and rz projections. For a set of cylindrical detectors, this resolution can be expressed as

$$\sigma = \sqrt{a^2 + \left(\frac{b}{p \sin^{\frac{3}{2}} \theta}\right)^2}$$

The constant a depends on the point resolution of the detectors and b represents the resolution degradation due to multiple scattering, which varies with track momentum p and polar angle θ. For the present detector design, the values of a and b are similar for both projections, and take the values 5.0 μm and 6.5 μm respectively. An example for one projection and polar angle is plotted in Fig 1.3.1. These calculations are based on a full GEANT description of the TESLA detector, and use the BRAHMS 2.1 detector simulation program, with the 'standard' layout of VTX, ITC and TPC for the overall track fitting. The solenoid field is set to 4 Tesla.

Tracks in jets typically have momenta below a few GeV, so the low momentum region is most important for flavour tagging. In the $r\phi$ projection, the uncertainty in the measurement of the track curvature contributes significantly to the impact parameter resolution at high momentum. It should be noted that for high energy jets, the decay vertices may be far from the IP, close to or even beyond the first layer of the vertex detector. Topological vertexing has the potential to become progressively cleaner in such cases, provided the code is written with these effects in mind.

Most of the simulations have been done using $Z^0 \to q\bar{q}$ events generated at $\sqrt{s} = m_Z$ with PYTHIA 6.1, since the 45 GeV jets are typical of the energies produced in more complex multijet final states at high energies, and provide a good benchmark for comparison with current experiments. These studies have then been extended to two-jet events over a wide energy range, in order to provide a more complete overview

R. Hawkings
Oberammergau Week

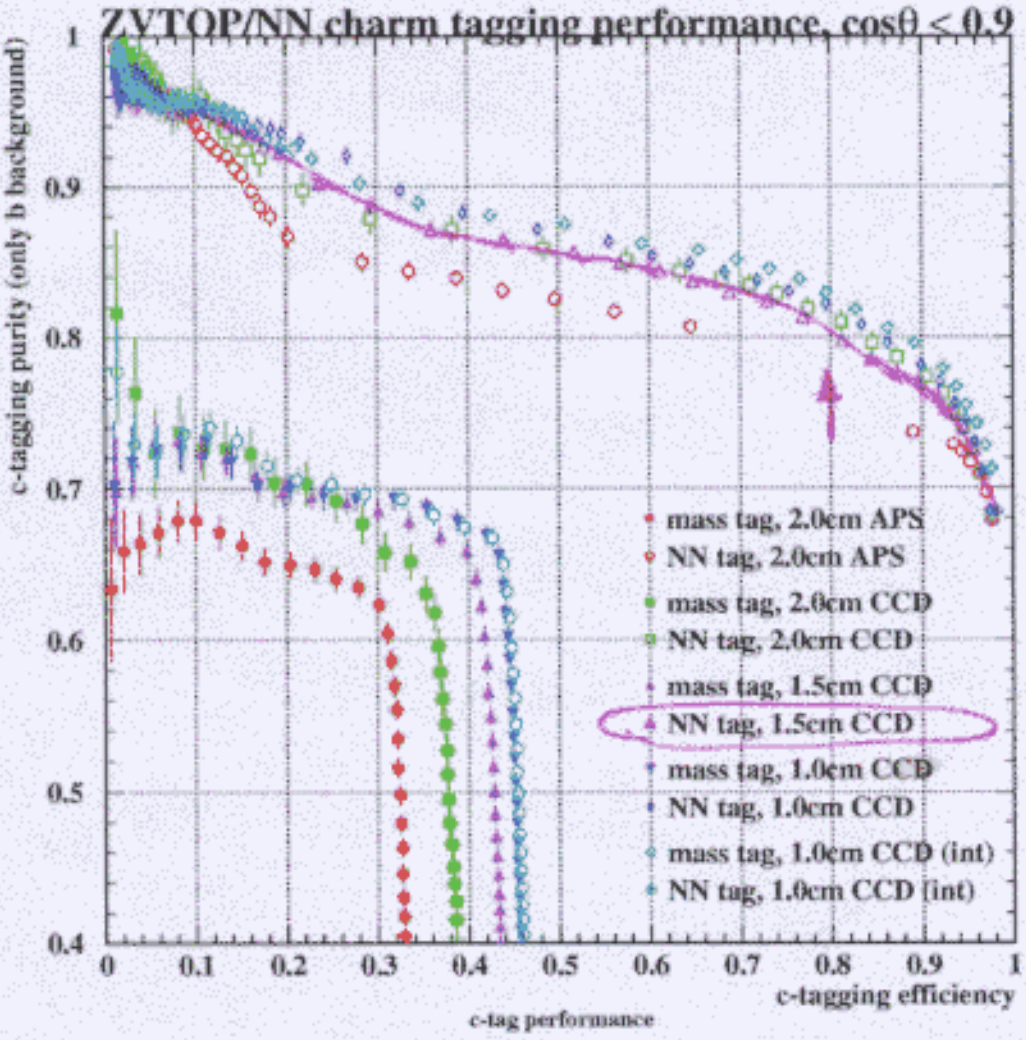


Figure 1.3.3: Efficiency and purity of c tag in Z^0 decays (including use of 1-prong c decays) *(to be revised soon)*

NB

R. Hawkings

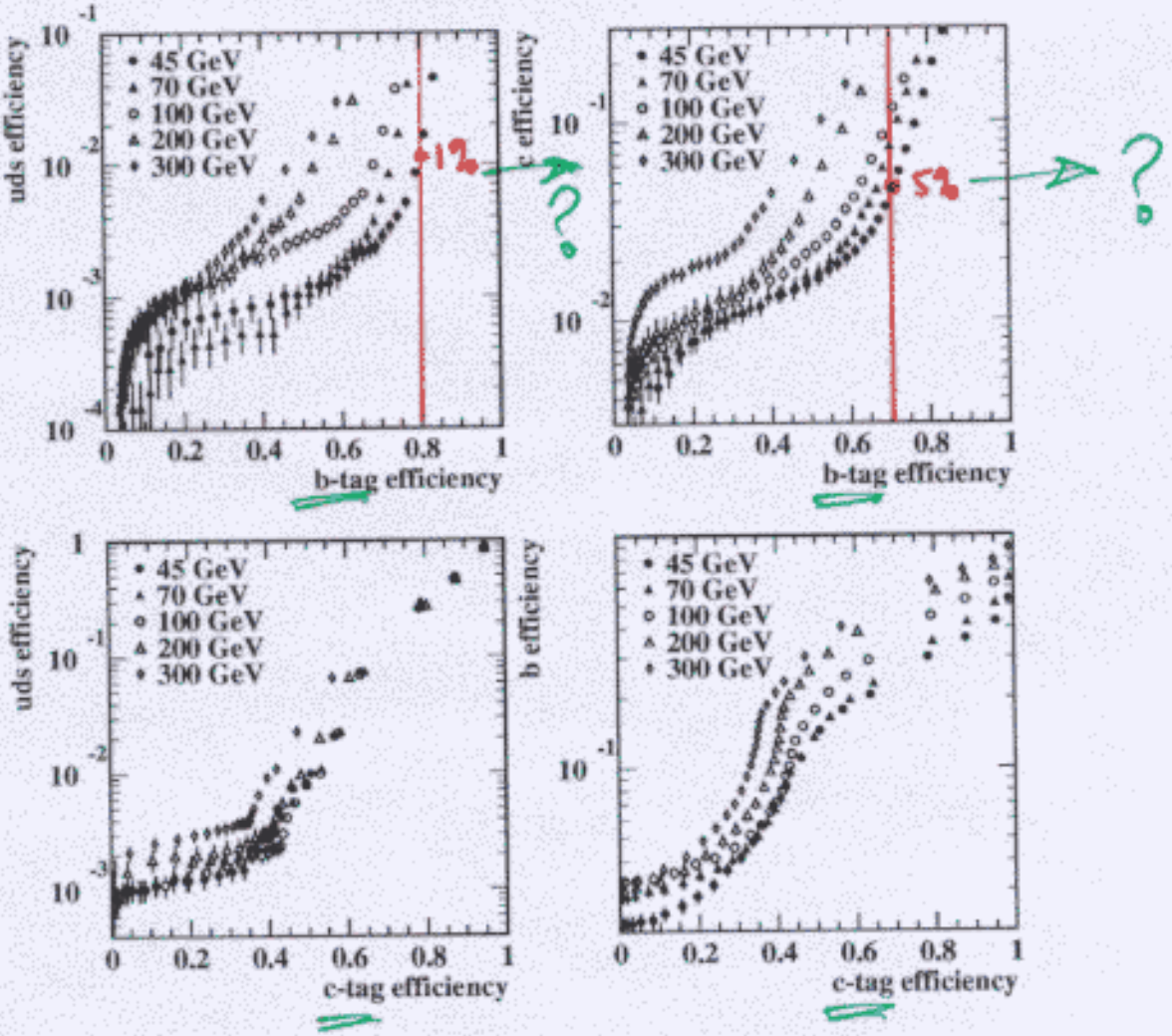
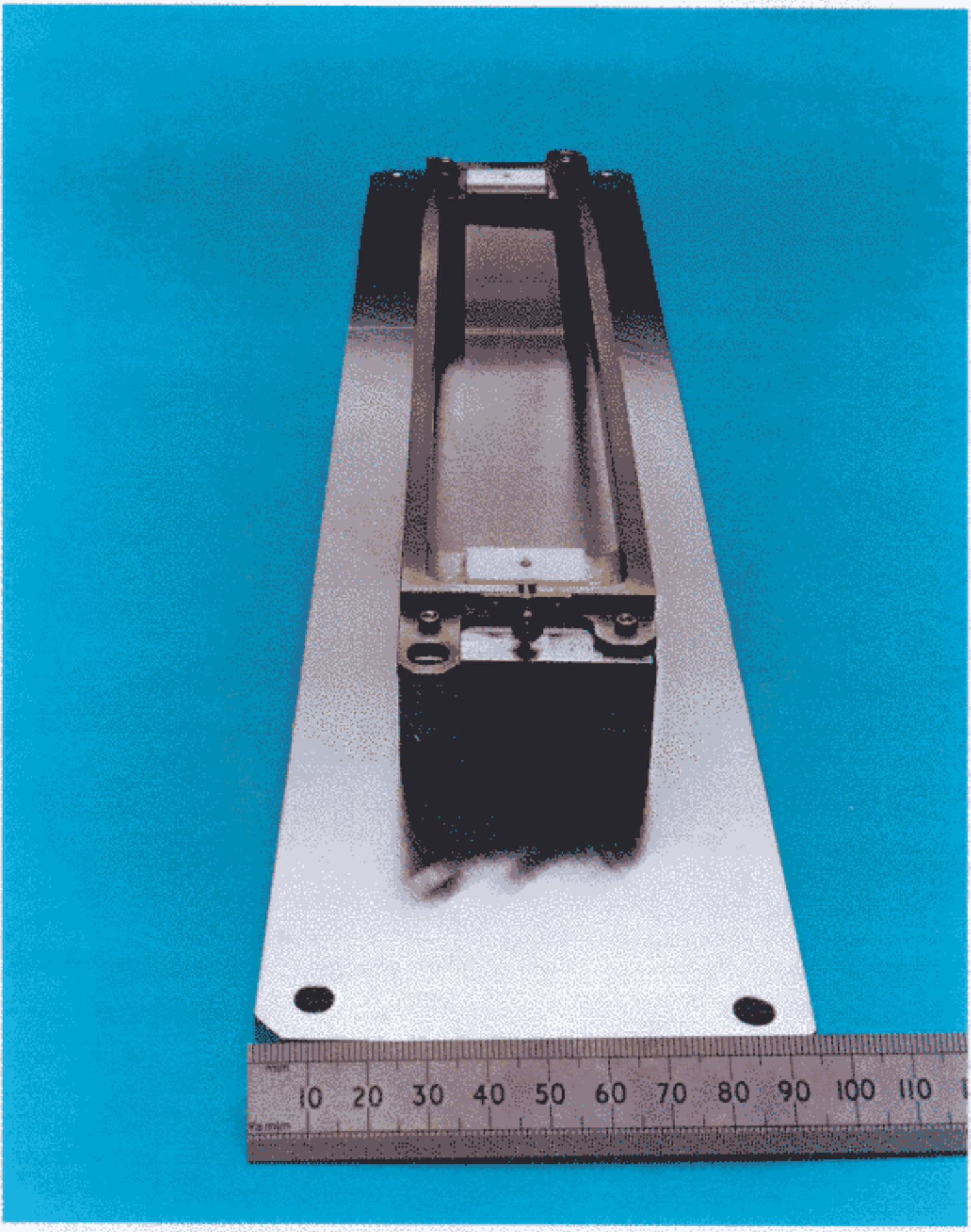
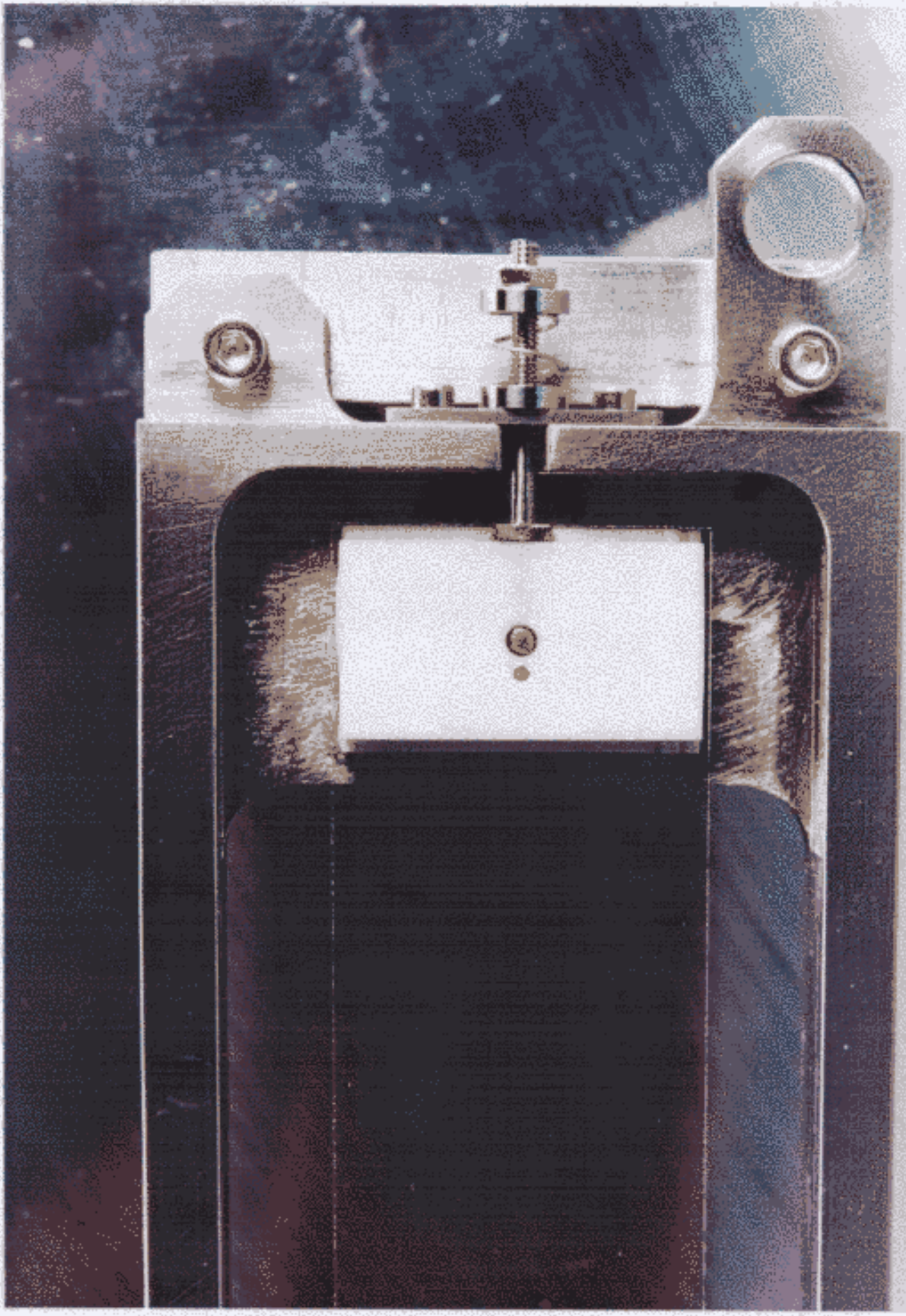


Figure 1.3.4: Tagging performance vs jet energy. *uds* and c effic vs b effic (top); *uds* and b effic vs c effic (bottom) *(to be revised soon)*

Figure 1.3.5: b and c tag performance (purity, for fixed efficiency) vs $\cos\theta_p$ in Z^0 decays*(to be calculated soon)*


10 20 30 40 50 60 70 80 90 100 110



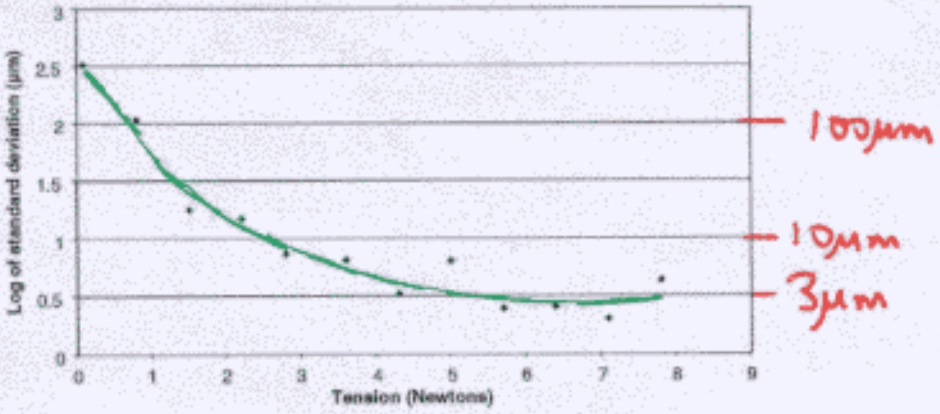


Figure 1.4.1: Stability of sagitta in mechanical model of stretched-silicon option, with respect to repeated disturbances of the geometry

Figure 1.4.2: Quality of drive pulses in the centre of a 2-phase ladder-1 CCD being clocked at 50 MHz *coming soon!*

1.2.4.2 CMOS pixel option

It will be important to establish the unit cell design appropriate for large-scale devices. A correlated double sampling circuit may be needed to reduce reset noise; there appears to be room for this within the 20 μm square pixel. The output capacitive load represented by the column line which overlays all the row lines needs to be established, and hence the requirement for the transconductance of the output FET in order to achieve the necessary signal risetime. The peripheral logic to perform the data sparsification needs to be designed; in some respects it can be similar to that of the CCD option.

Putting these pieces together will establish the scaling law for these devices (width and length) and hence the practical limit for this application. If it turns out to be feasible to work with $> 12 \times 2$ cm^2 read from only one end at the required readout frequency, then the unsupported silicon option will be equally promising for this architecture. If not, the degree of tiling necessary will be apparent. If one or more readout sections need to be situated inside the active volume of the detector, this will increase significantly the cooling requirements.

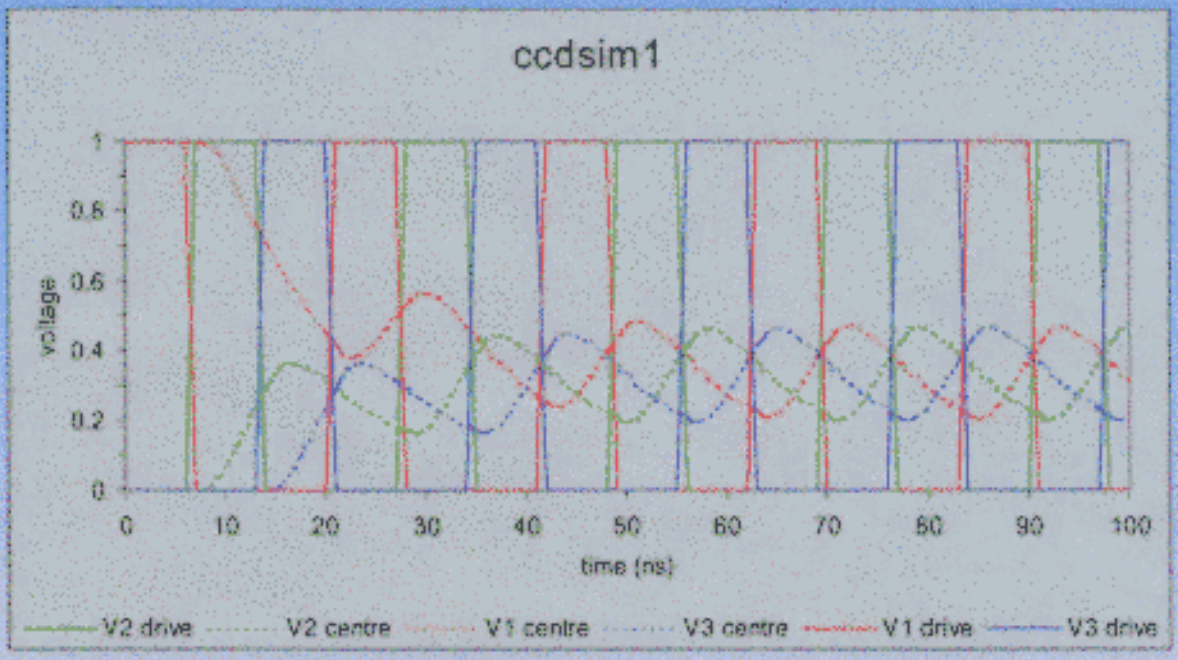
In any event, the question as to whether the APS option is amenable to pulsed power operation is of considerable interest. To some extent, circuit features such as correlated double sampling can protect against the effects of baseline drift.

1.2.4.3 Hybrid pixel option

Hybrid pixel sensors have been adopted at LEP, heavy ion experiments and at the LHC. These activities have gathered a significant know-how and addressed important issues related to reliability, radiation hardness and timing capabilities of these detectors. The

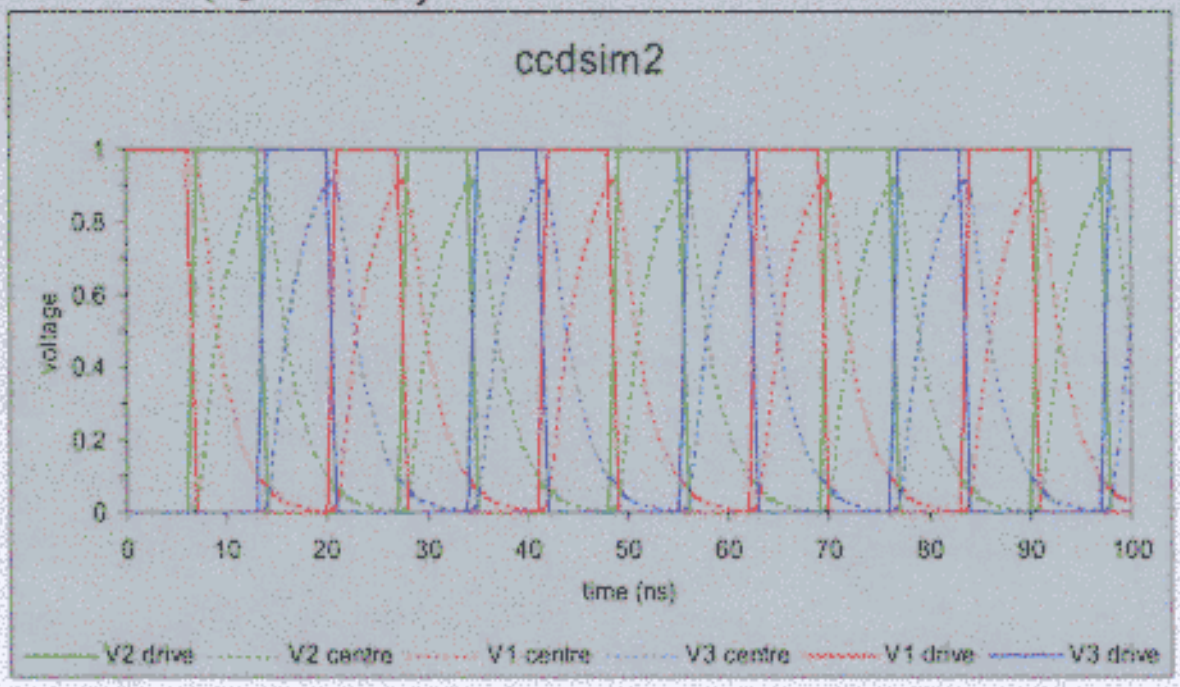
Column-parallel CCD clocking

a) Drive waveform variation across the CCD in X:



- **Add 3 μm wide Al overlay to the polysilicon gates —**

(OPAQUE)



- **Waveform amplitudes attenuated by <10% in centre *(X)***

linear collider application now defines new areas of specific R&D aimed to improve the achievable single point resolution to better than 10 μm and to reduce the sensor+VLSI thickness.

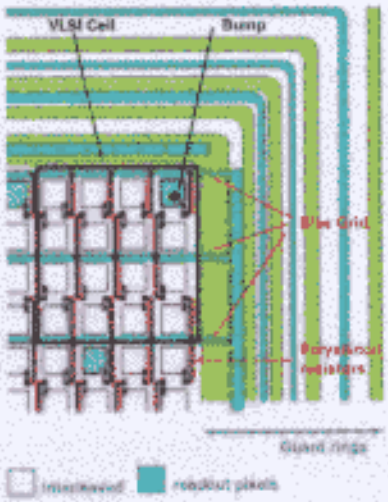


Figure 1.4.3: Layout of the upper corner of pixel detector test structure, with 50 μm implant and 200 μm read-out pitch.

In pixel devices the ultimate read-out pitch is constrained by the front-end electronics, to be integrated in a cell matching the sensor pattern. At present, the most advanced read-out electronics have a minimum cell dimension of 50×300 μm^2 not suitable for a finely segmented charge sampling. The trend of the VLSI development and recent studies [?] on intrinsic radiation hardness of deep sub-micron CMOS technology allows to envisage a sizeable reduction in the cell dimensions. However, sensor designs without such basic limitations are definitely worth being explored. A possible solution is to exploit the capacitive coupling of neighbouring pixels and to have a read-out pitch n times larger than the implant pitch [?]. The proposed sensor layout is shown in Figure 4 for n=4. In this configuration, the charge carriers created underneath an interleaved pixel will induce a signal on the capacitively coupled read-out nodes. The ratio of the signal amplitudes on the read-out nodes at both sides is correlated to the particle position and the resolution is expected to be better than (implant pitch)/$\sqrt{12}$ for an implant pitch of 25 μm or smaller. The ratio between the inter-pixel capacitance and the pixel capacitance to backplane plays here a crucial role, as it defines the signal amplitude reduction at the output nodes and therefore the maximum number of interleaved pixels. In order to verify the feasibility of this scheme a dedicated R&D program has started [?]. Prototype sets of sensors with interleaved pixels and different choices of implant and read-out pitch have been already designed, produced and characterised [?, ?].

Relevance of planned R&D to other applications (imaging, FEL,...)