TESLA

S2E Simulations on Jitter Issues for the European XFEL Project

- Layout (10AUG04 Version) with Two BC Stages -

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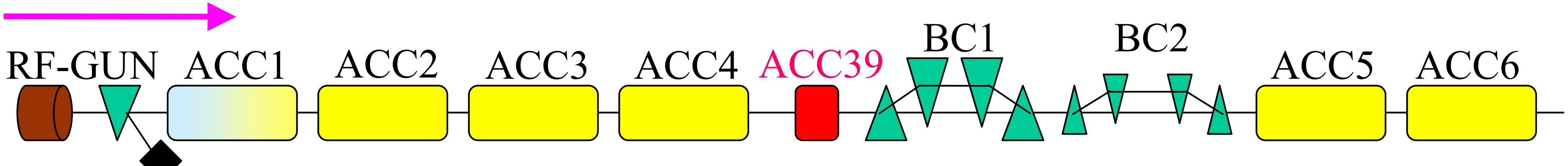
Current Layout for XFEL (13JAN04)

With Old European XFEL Injector, ε_n= 0.90 μm

Q=1.0 nC

e-beam

σ_z = 1.76 mm → 113 μm → 20.5 μm →



60 MV/m
44.0 deg

11.5 MV/m
25.0 MV/m
-18.3 deg

20.5 MV/m
-29.6 deg

34.8 MV/m
160.6 deg

E = 510 MeV
$\sigma_\delta \sim$ 1.89%
R_{56} = 87 mm
θ = 3.95 deg

E = 510 MeV
$\sigma_\delta \sim$ 1.88%
R_{56} = 4.8 mm
θ = 0.93 deg

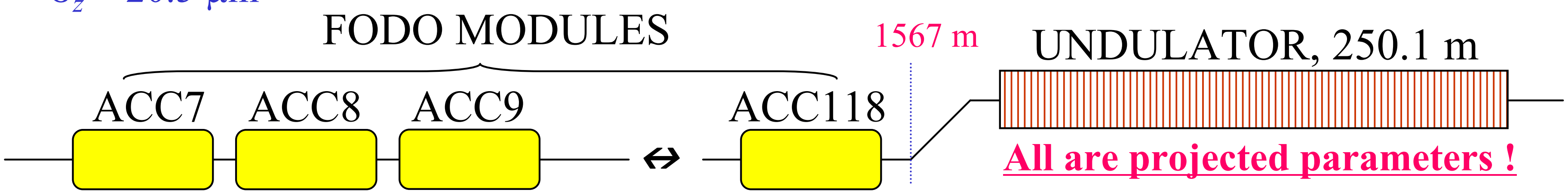
20.65 MV/m
0.0 deg

ASTRA with Space Charge

0.0 m — 12.0444 m

To the end of Linac : ELEGANT with CSR
with geometric wakefields
without space charge

σ_z = 20.5 μm →



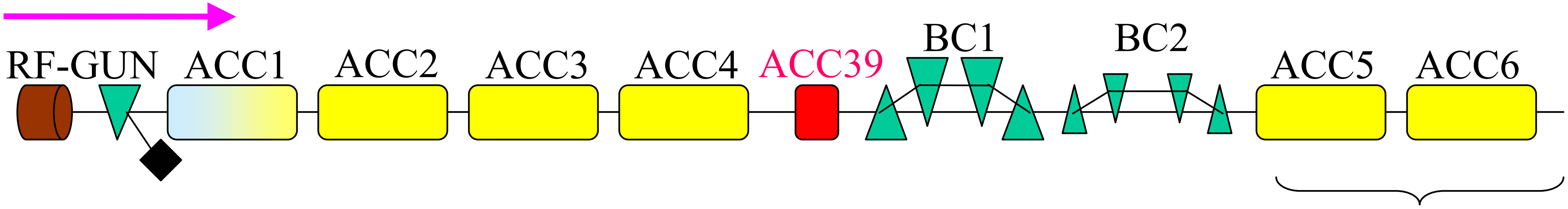
All are projected parameters !

20.65 MV/m
0.0 deg

E = 20.0 GeV
σ_δ = 0.008%
σ_x= 37.3 μm, σ_y= 31.6 μm, σ_z = 20.5 μm
ε_{nx}= 1.19 μm, ε_{ny}= 0.94 μm

Klystron Distribution of Current Layout

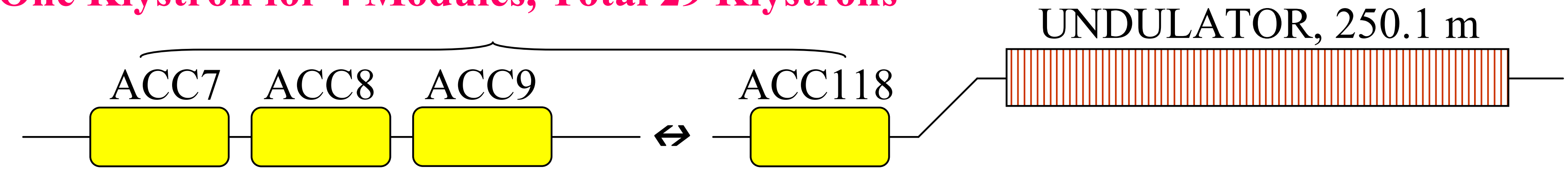
Here K.No means the number of Klystron per module !



K.No = 1 2 1 1 1 2

One Klystron for 4 MODULES

One Klystron for 4 Modules, Total 29 Klystrons



Multi-Klystron before BC2 reduces the jitter sensitivity in ACC234 and ACC39 modules

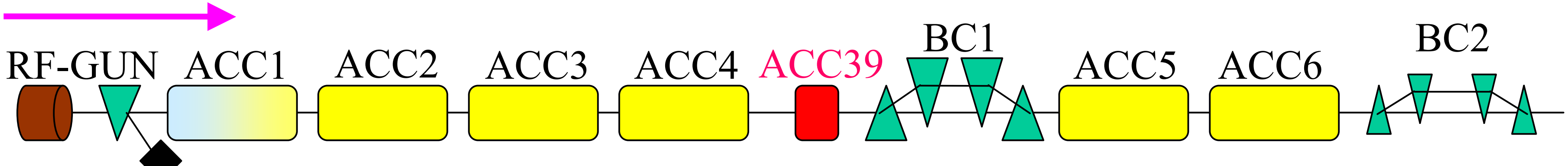
Alternative Layout for XFEL (10AUG04)

With New European XFEL Injector, ε_n= 0.88 μm

Q=1.0 nC

e-beam

σ_z = 1.72 mm → 94 μm → 21.6 μm



60 MV/m
40.0 deg

12.8 MV/m
24.84 MV/m
-25.0 deg

20.2 MV/m
-25.0 deg

34.5 MV/m
165.9 deg

E = 518 MeV
σ_δ ~ 1.87%
R_{56} = 87 mm
θ = 3.95 deg

0-20.5-35 MV/m
-44.5 deg

E = 518-760-1100 MeV
σ_δ ~ 1.87-1.33-0.9%
R_{56} ~ 5.3 mm
θ ~ 0.93 deg

ASTRA with Space Charge

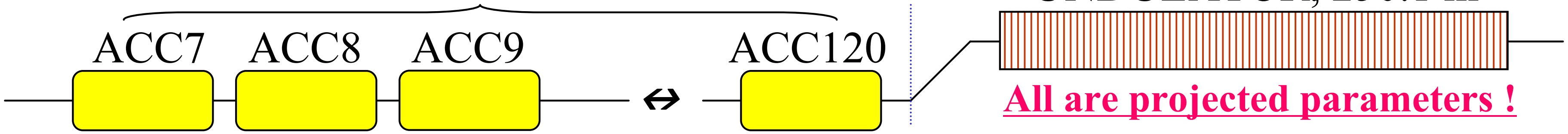
0.0 m — 12.9869 m

To the end of Linac : ELEGANT with CSR
with geometric wakefields
without space charge

σ_z = 21.6 μm →

FODO MODULES

1579 m



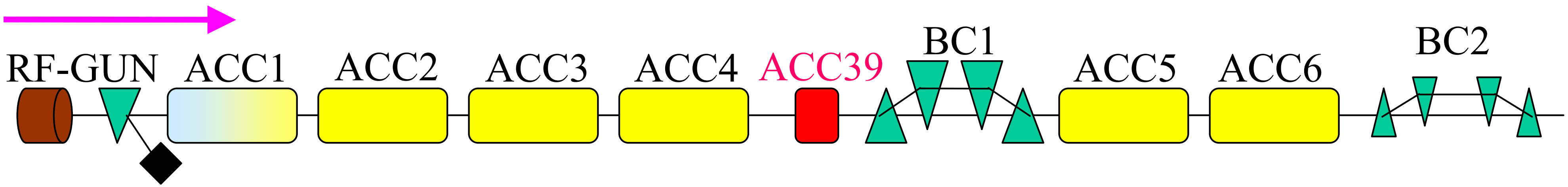
All are projected parameters !

20.38 MV/m
0.0 deg

E = 20.0 GeV
σ_δ = 0.0088%
σ_x= 34.2 μm, σ_y= 29.5 μm, σ_z = 21.6 μm
ε_{nx}= 1.044 μm, ε_{ny}= 0.896 μm

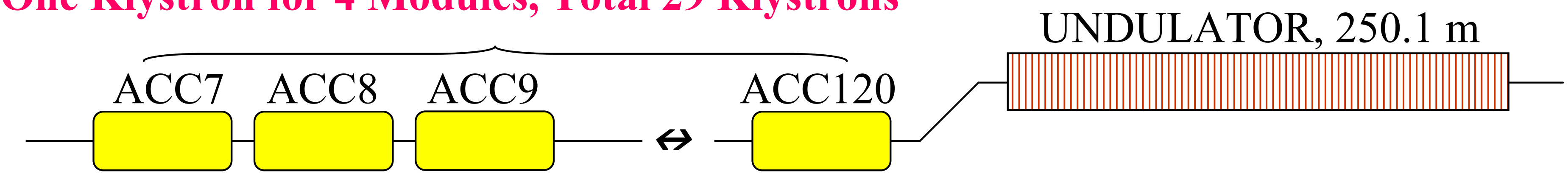
Klystron Distribution of Alternative Layout

Here K.No means the number of Klystron per module !



K.No = 1 2 1 1 1 2 1 1

One Klystron for 4 Modules, Total 29 Klystrons



Multi-Klystron before BC2 reduces the jitter sensitivity in ACC234, ACC39, and ACC56

Papers On Two Linac Layouts for XFEL

On Current Linac Layout (13JAN04 Version) with a Double Chicane

S2E simulation on Linac Optimization :
APAC2004, EPAC2004
by Yujong Kim, K. Flöttmann, T. Limberg, M. Dohlus, and D. Son

S2E Simulations on Jitter :
EPAC2004
by Yujong Kim, K. Flöttmann, and T. Limberg, and D. Son

On Alternative Linac Layout (10AUG04 Version) with Two BC Stages

S2E simulation on Linac Optimization :
LINAC2004
by Yujong Kim, K. Flöttmann, T. Limberg, and D. Son

S2E Simulations on Jitter :
Not yet reported due to limited available computer, maybe, at PAC2005

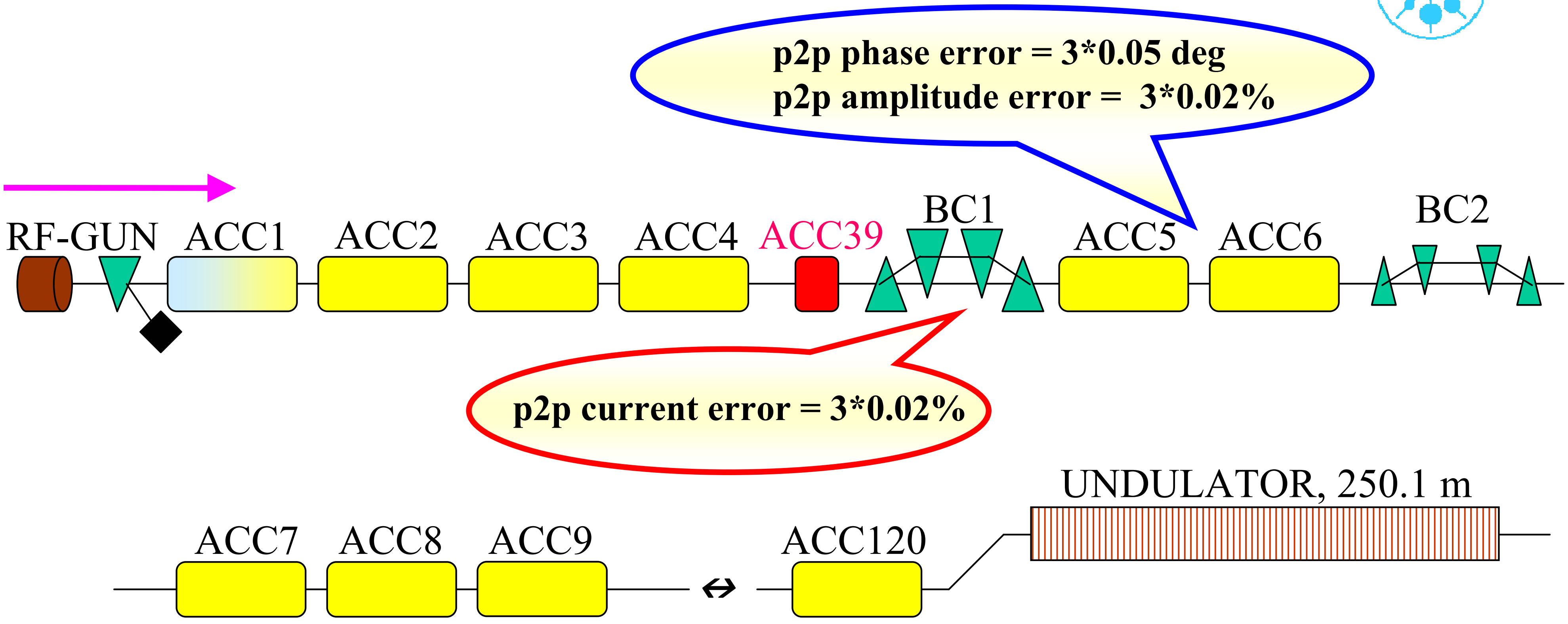
Sensitivity & Tolerance Set for Current Layout

Linac Performance Based Tolerance (refer to our EPAC2004 paper)

For each Klystron

	Sensitivity	TOL-I (rms)	TOL-II (rms)
dT	0.50 ps	0.1 ps	0.3 ps
dQ	- 6.10%	1.0%	1.5%
ACC1C1234 Phase	0.20 deg	0.05 deg	0.07 deg
ACC1C1234 dV/V	- 0.17%	0.02%	0.03%
ACC1C5678 Phase	0.10 deg	0.05 deg	0.07 deg
ACC1C5678 dV/V	-0.08%	0.02%	0.03%
ACC234 Phase	-0.056 deg	0.05 deg	0.07 deg
ACC234 dV/V	-0.06%	0.02%	0.03%
ACC39 Phase	-0.08 deg	0.05 deg	0.07 deg
ACC39 dV/V	0.19%	0.02%	0.03%
BC1 dI/I	0.02%	0.02%	0.02%
BC2 dI/I	0.31%	0.02%	0.02%
ACC5678 Phase	4.19 deg	0.05 deg	0.07 deg
ACC5678 dV/V	0.028%	0.02%	0.03%

S2E Simulations Under Same Jitter Tolerances

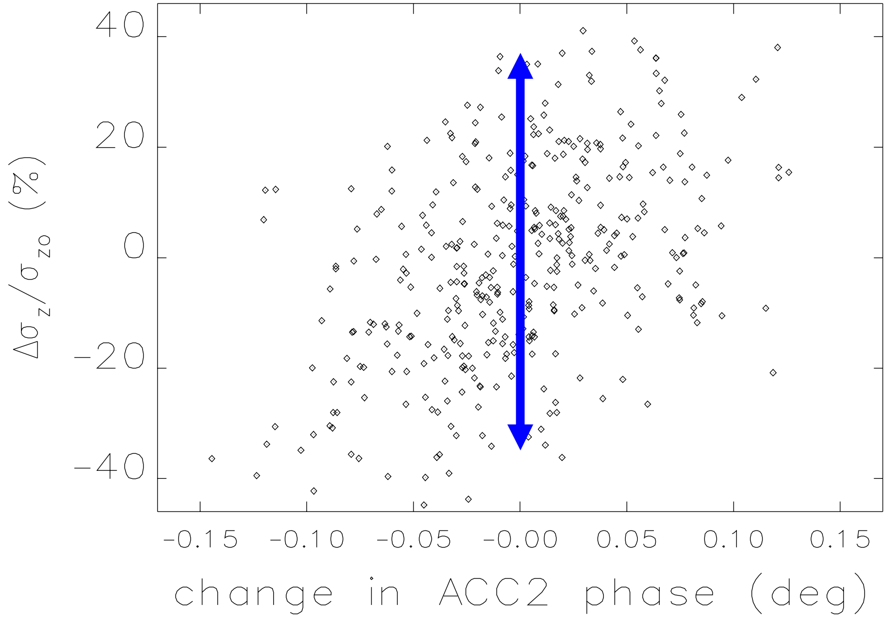


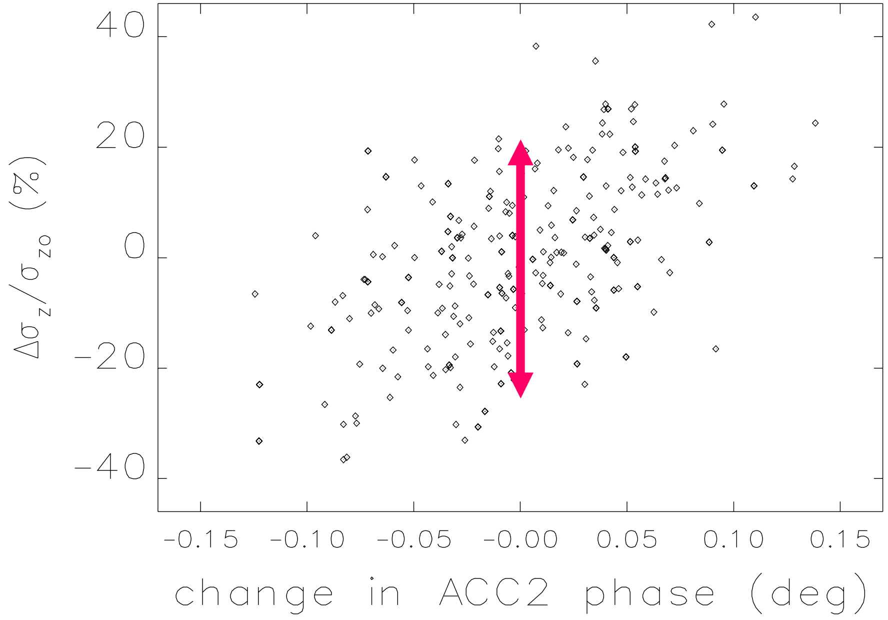
After applying random error set (p2p = 3 × tolerance) to each component, we have performed about 400 times S2E simulations from gun to the end of linac to compare two linac layouts under same jitter tolerance set (TOL-I).

Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Curent Layout **400 Times Tracking with Alternative Layout**

most sensitive jitter source on bunch length = ACC2 phase error





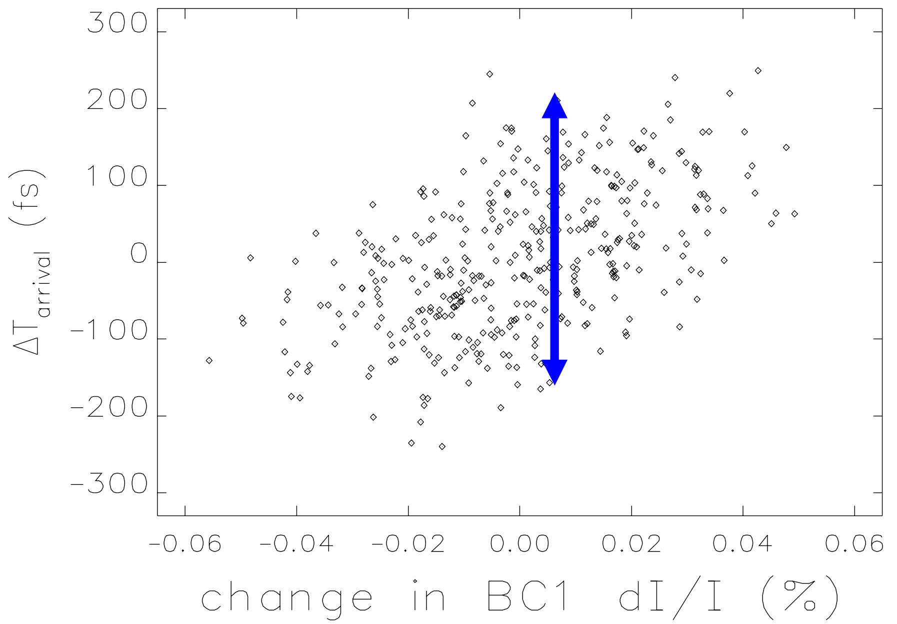
wider change in bunch length for current layout
stronger correlation with errors in other components !

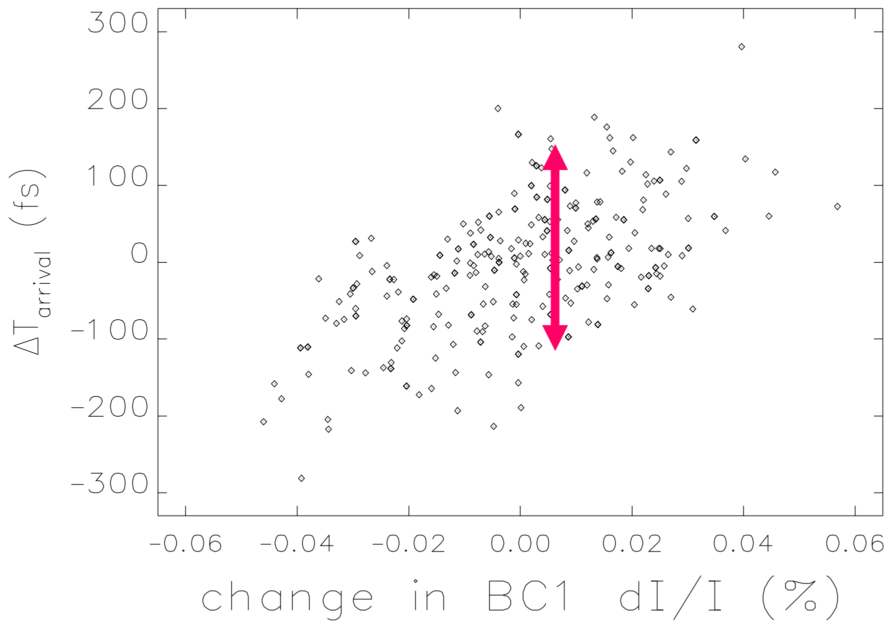
Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Curent Layout

400 Times Tracking with Alternative Layout

most sensitive jitter source on arriving time = BC1 current error





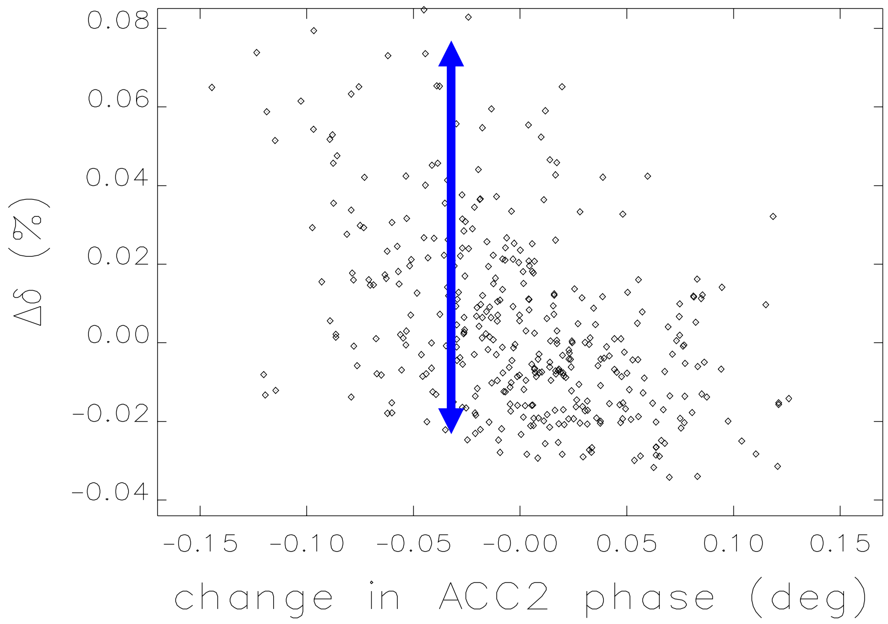
wider change in bunch arriving time for current layout
stronger correlation with errors in other components !

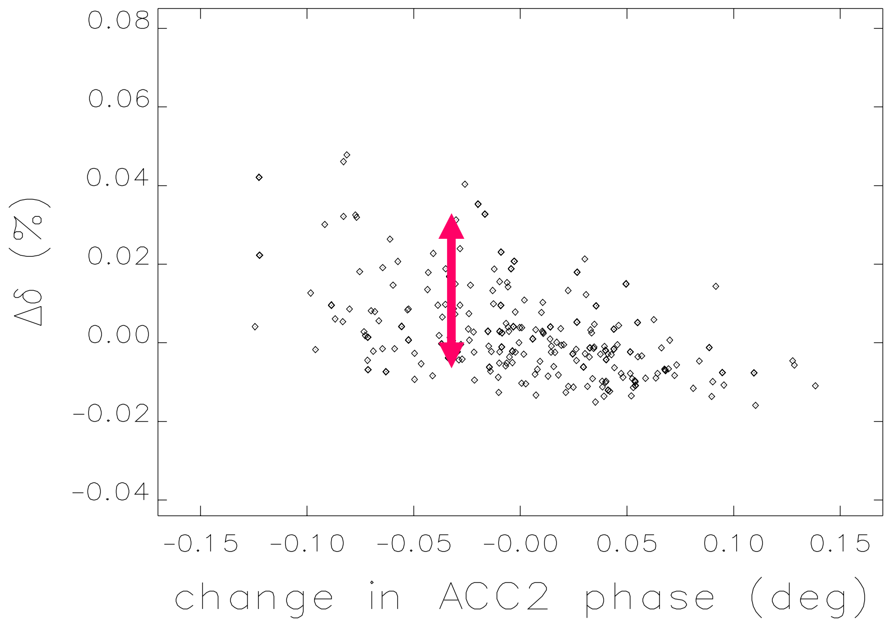
Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Curent Layout

400 Times Tracking with Alternative Layout

most sensitive jitter source on p2p energy deviation = ACC2 phase error



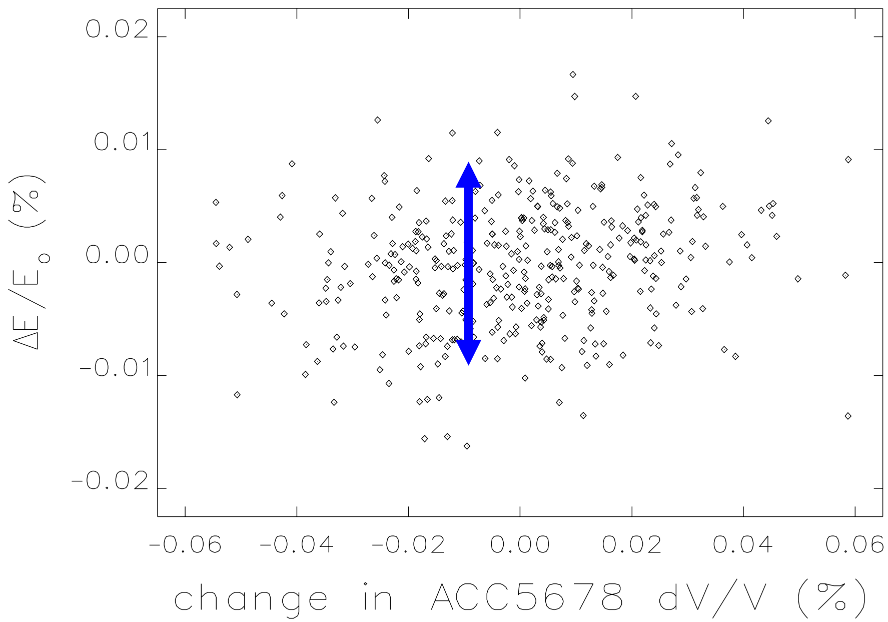


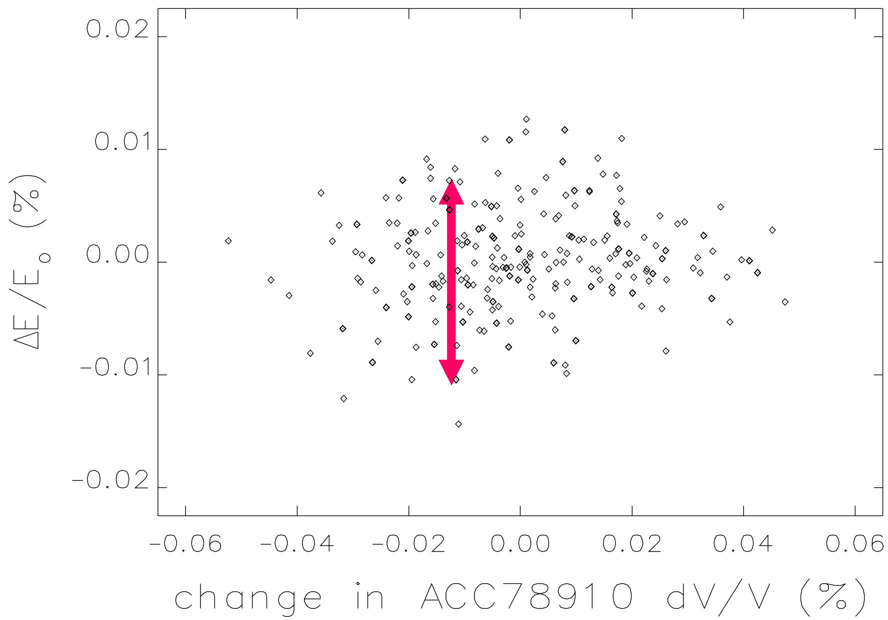
wider change in p2p energy deviation for current layout
stronger correlation with errors in other components !

Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Curent Layout **400 Times Tracking with Alternative Layout**

most sensitive jitter source on average energy = DBC2 voltage error

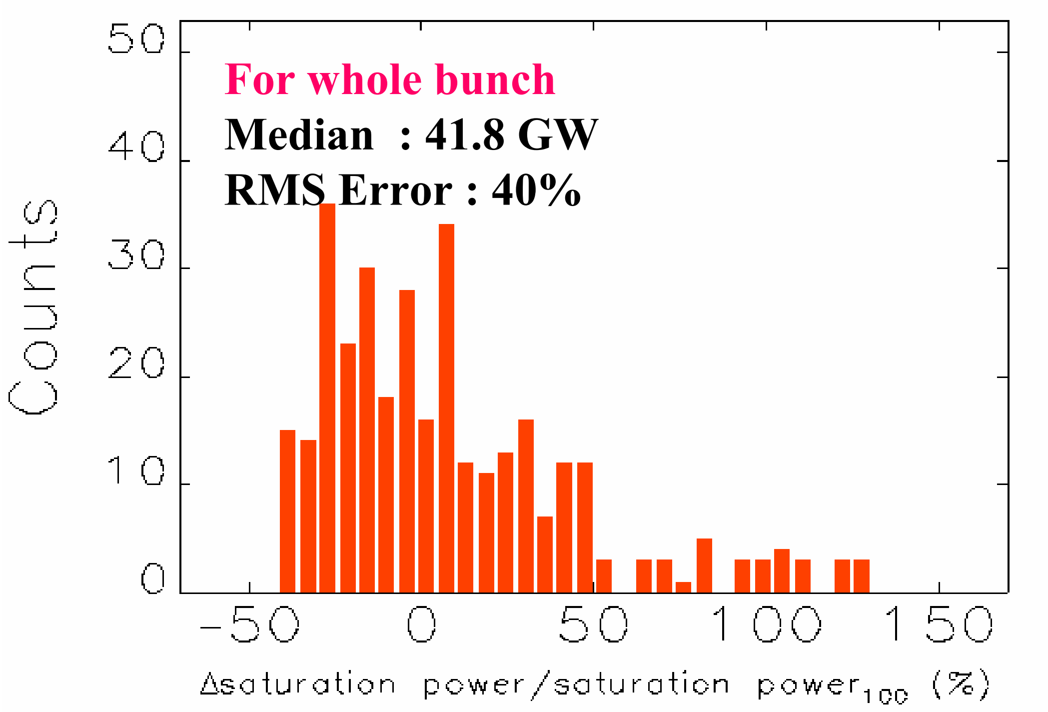




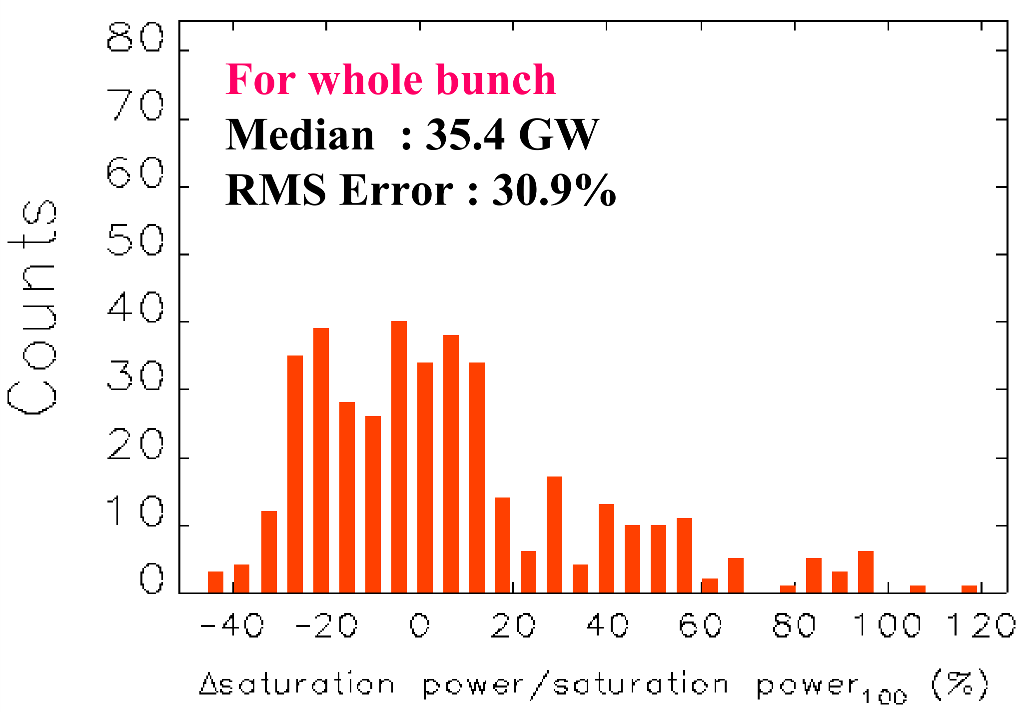
similar change in average energy for both layouts
DBC2 is exactly same for both linac layouts

Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Curent Layout



400 Times Tracking with Alternative Layout



Newly Updated Controllable Jitter Tolerance

According to Dr. Simrock's LINAC2004 Talk:

For both 1.3 GHz TESLA Module & 3.9 GHz 3rd Harmonic Module

For the short term period (1 min)
RF Phase Error < 0.02 degree (rms)
RF Amplitude Error (dV/V) < 0.02% (rms)

New Reference !

Controllable jitter tolerance depends on charge fluctuation !

$$Q = Q_0(1 + 0.03\Delta\phi_1)(1 + (\Delta E / E)_1)(1 + (\Delta V / V)_g)$$

Dr. Simrock confirmed that these can be reduced to 0.01 deg and 0.01% soon.

New Threshold of Jitter Sensitivity

By the help of S2E simulations, let's apply artificial jitter or error to all important components (GUN, ACC1 ~ ACC120, ACC39, BC1 and BC2) in order to investigate the jitter sensitivity J_s of those components on the FEL performance at the undulator (SASE1).

After considering controllable jitter tolerances in the near future, we have determined new thresholds of jitter sensitivity, which are related with FEL performance (Applying Ming Xie Model to SASE1) :

Peak-to-peak (p2p) change in SASE source wavelength should be within ±0.022%
Peak-to-peak (p2p) change in saturation length should be within ±1.6%
Peak-to-peak (p2p) change in saturation power should be within ±15%
Peak-to-peak (p2p) change in bunch arrival time should be within 36 fs (=0.5σ_z)

Then choose the jitter tolerance J_t which gives

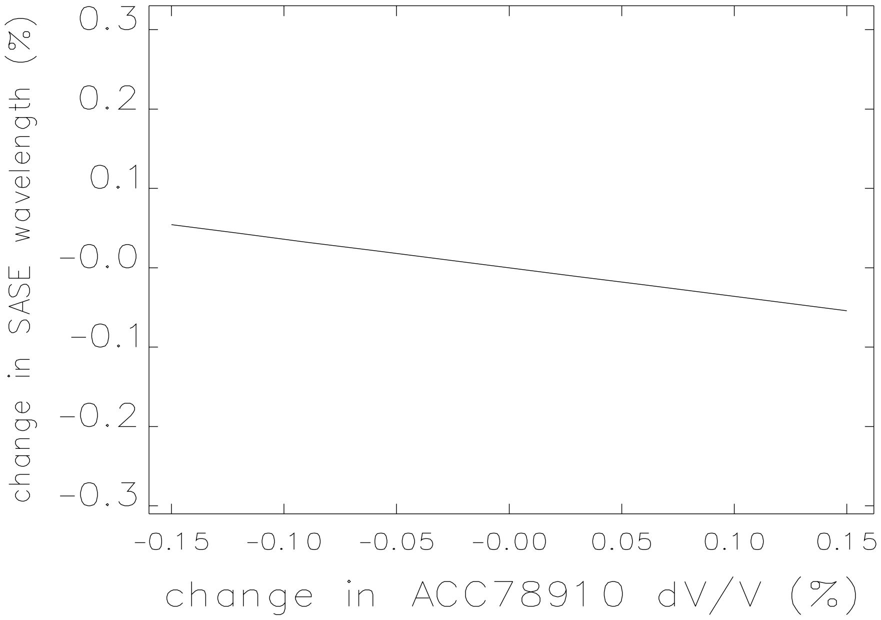
$$\sqrt{\sum_{i=1}^{n}\left(\frac{J_{t,i}}{J_{s,i}}\right)^2} < 1$$

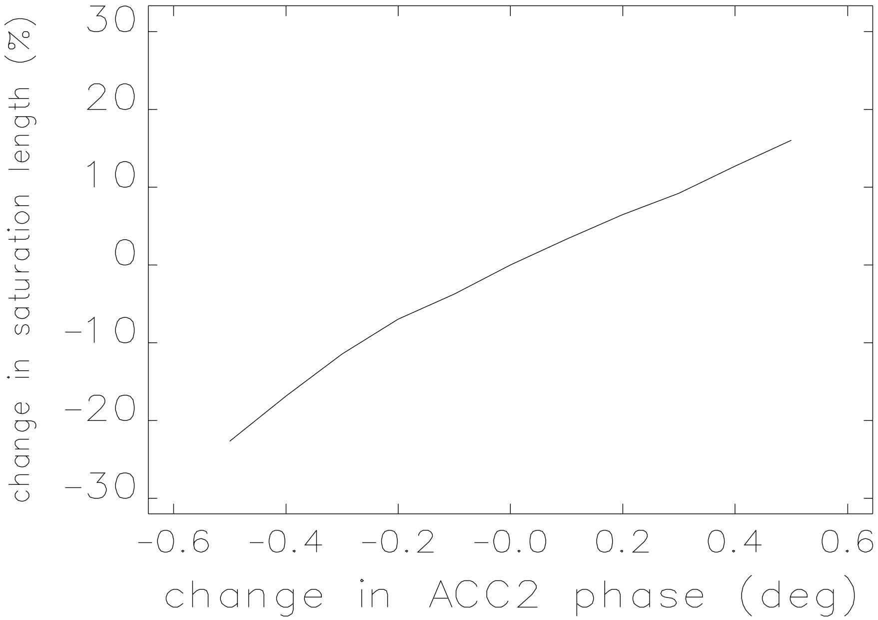
Then we have checked overall FEL performance under random tolerances set by repeating about 400 times S2E simulations.

Most Sensitive Sources to FEL Performances

Alternative Layout with 2BC

ACC78910 dV/V is the most sensitive jitter source to wavelength
ACC234 Phase is the most sensitive jitter source to saturation length





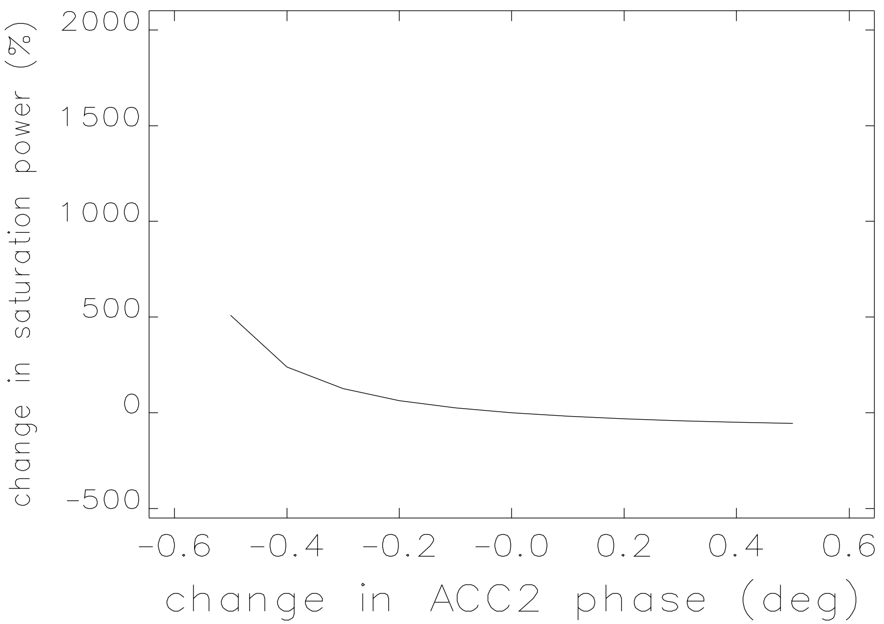
p2p sensitivity in wavelength ~ ± 0.06%
p2p change in wavelength ~ ± 0.022%

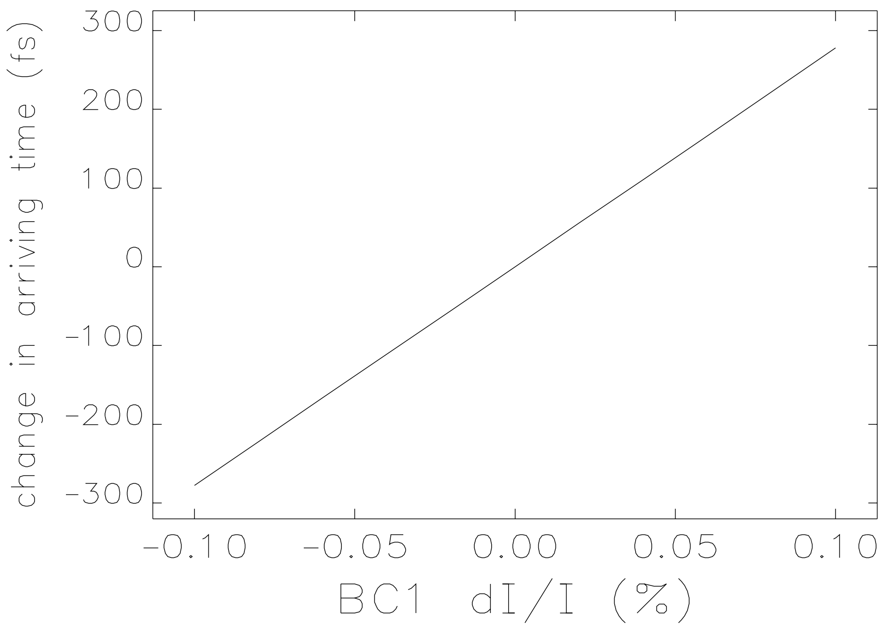
p2p sensitivity in sat. length ~ ± 0.06 deg
p2p change in sat. length ~ ± 1.6%

Most Sensitive Sources to FEL Performances

Alternative Layout with 2BC

ACC234 Phase is the most sensitive jitter source to saturation power
BC1 dI/I is the most sensitive jitter source to arriving time





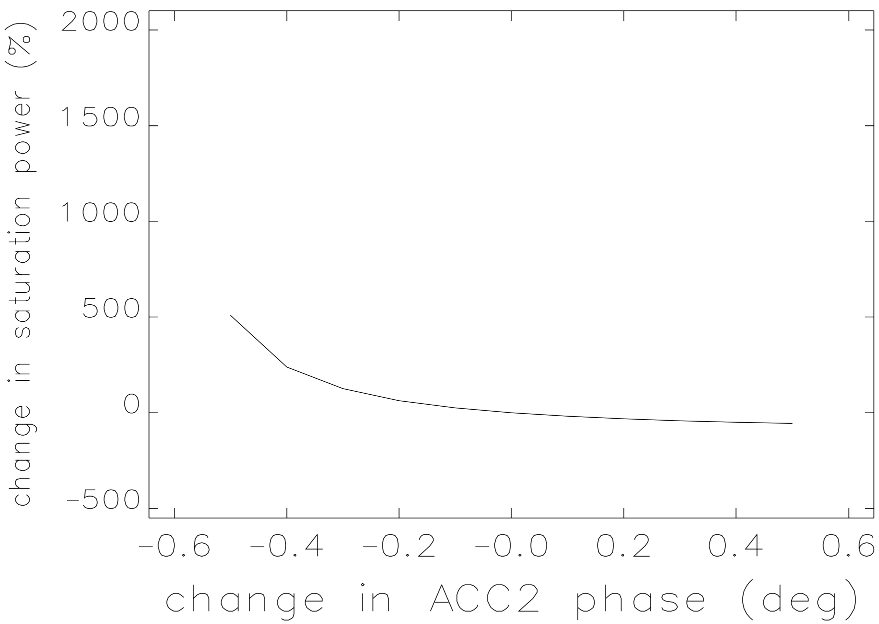
p2p sensitivity in sat. power ~ ± 0.06%
p2p change in sat. power ~ ± 15%

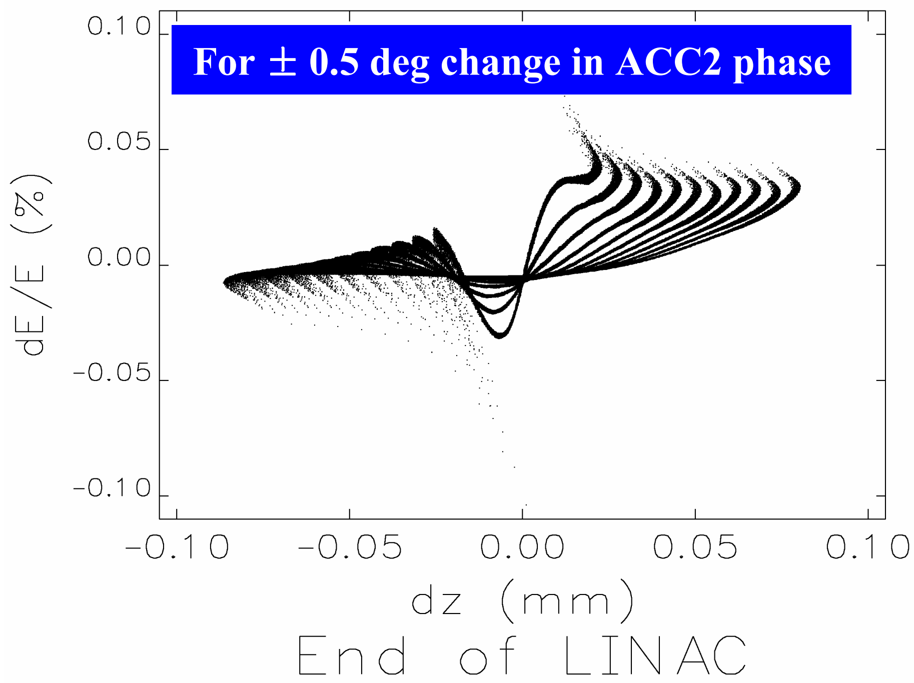
p2p sensitivity in arriving time ~ ± 0.004%
p2p change in arriving time ~ ± 36 fs

Most Sensitive Sources to FEL Performances

Alternative Layout with 2BC

ACC234 Phase is the most sensitive jitter source to saturation power and saturation length



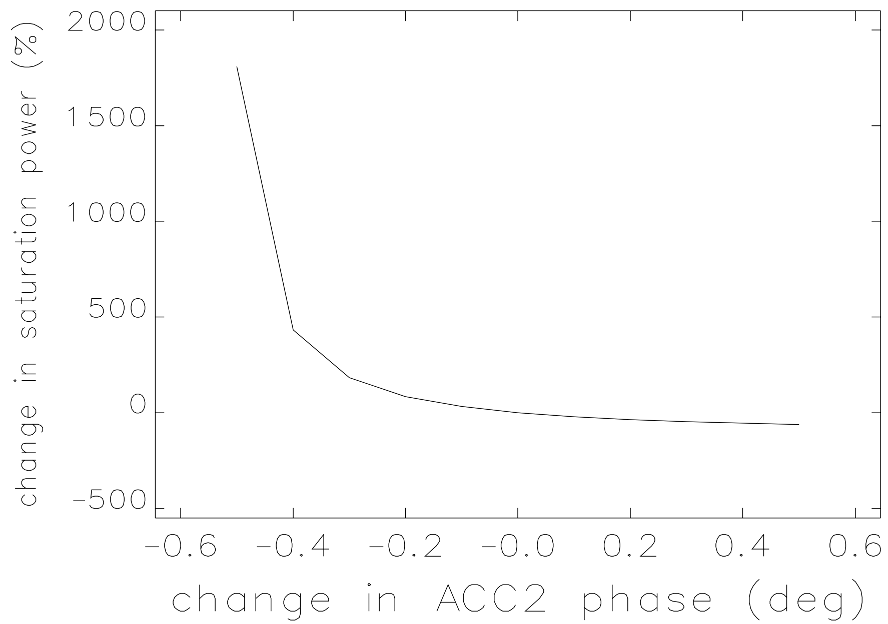


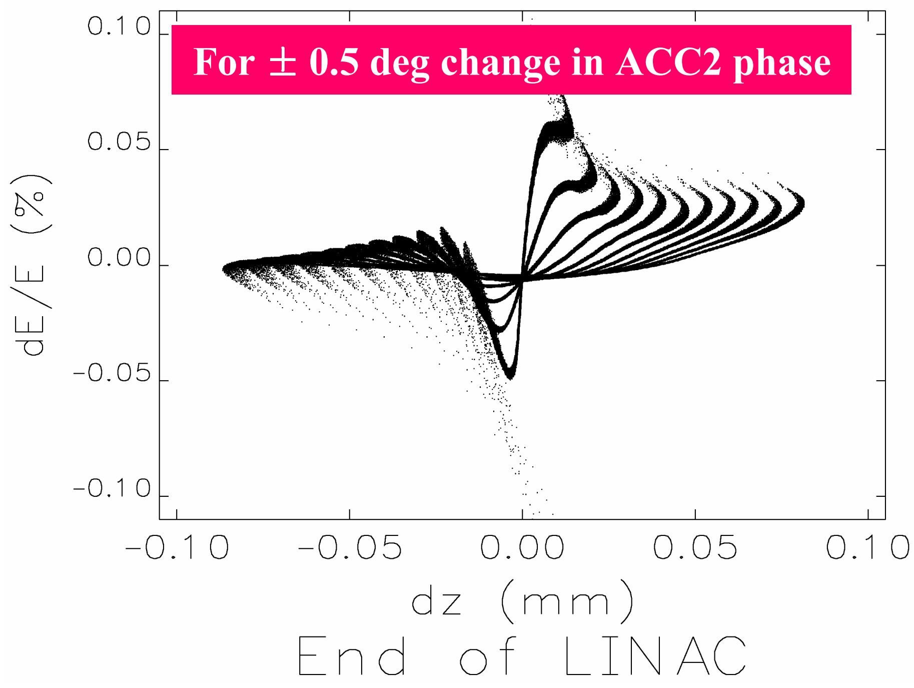
weak over-compression against ACC234 phase error

Most Sensitive Sources to FEL Performances

Current Layout with Double Chicane

ACC234 Phase is the most sensitive jitter source to saturation power and saturation length





strong over-compression against ACC234 phase error

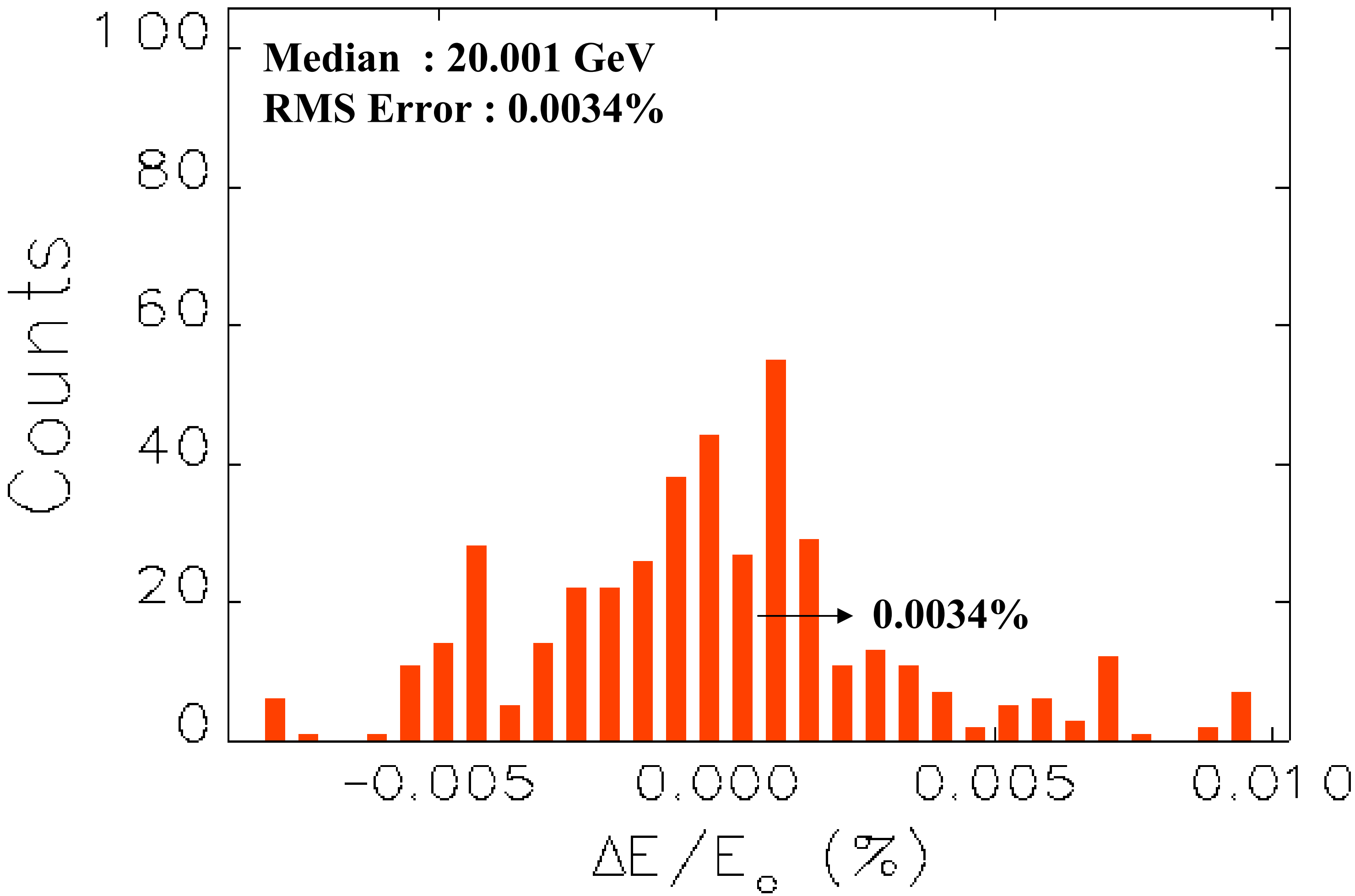
Sensitivity & Tolerance for Alternative Layout

FEL Performance Based Tolerance

	Sensitivity(p2p)	Tol. (p2p)	Tol. (rms)	Threshold
dT	± 0.729 ps	± 0.300 ps	0.100 ps	saturation length
dQ/Q	± 5.452%	± 3.000%	1.000%	saturation length
ACC1C1234 phase	± 0.133 deg	± 0.045 deg	0.015 deg	saturation length
ACC1C1234 dV/V	± 0.129%	± 0.045%	0.015%	arriving time
ACC1C5678 phase	± 0.072 deg	± 0.045 deg	0.015 deg	saturation power
ACC1C5678 dV/V	± 0.063%	± 0.045%	0.015%	arriving time
ACC234 phase	± 0.048 deg	± 0.045 deg	0.015 deg	arriving time
ACC234 dV/V	± 0.045%	± 0.045%	0.015%	arriving time
ACC39 phase	± 0.064 deg	± 0.045 deg	0.015 deg	saturation power
ACC39 dV/V	± 0.142%	± 0.045%	0.015%	arriving time
BC1 dI/I	± 0.013%	± 0.012%	0.004%	arriving time
ACC56 phase	± 0.721 deg	± 0.045 deg	0.015 deg	arriving time
ACC56 dV/V	± 0.913%	± 0.045%	0.015%	saturation length
BC2 dI/I	± 0.201%	± 0.012%	0.004%	arriving time
ACC78910 phase	±10.037 deg	± 0.045 deg	0.015 deg	SASE wavelength
ACC78910 dV/V	± 0.060%	± 0.045%	0.015%	SASE wavelength

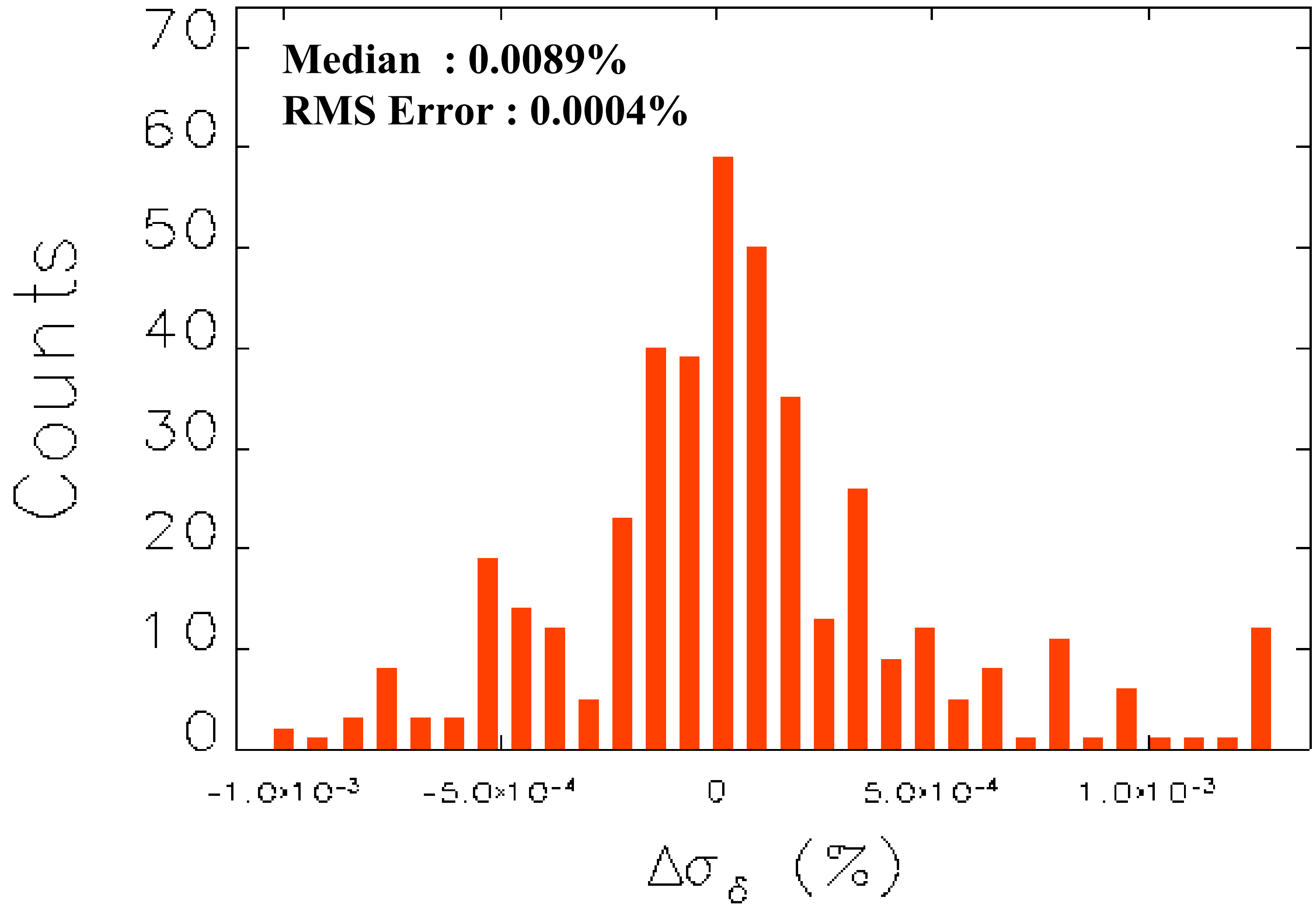
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances



S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances



S2E simulations under FEL based Tolerances

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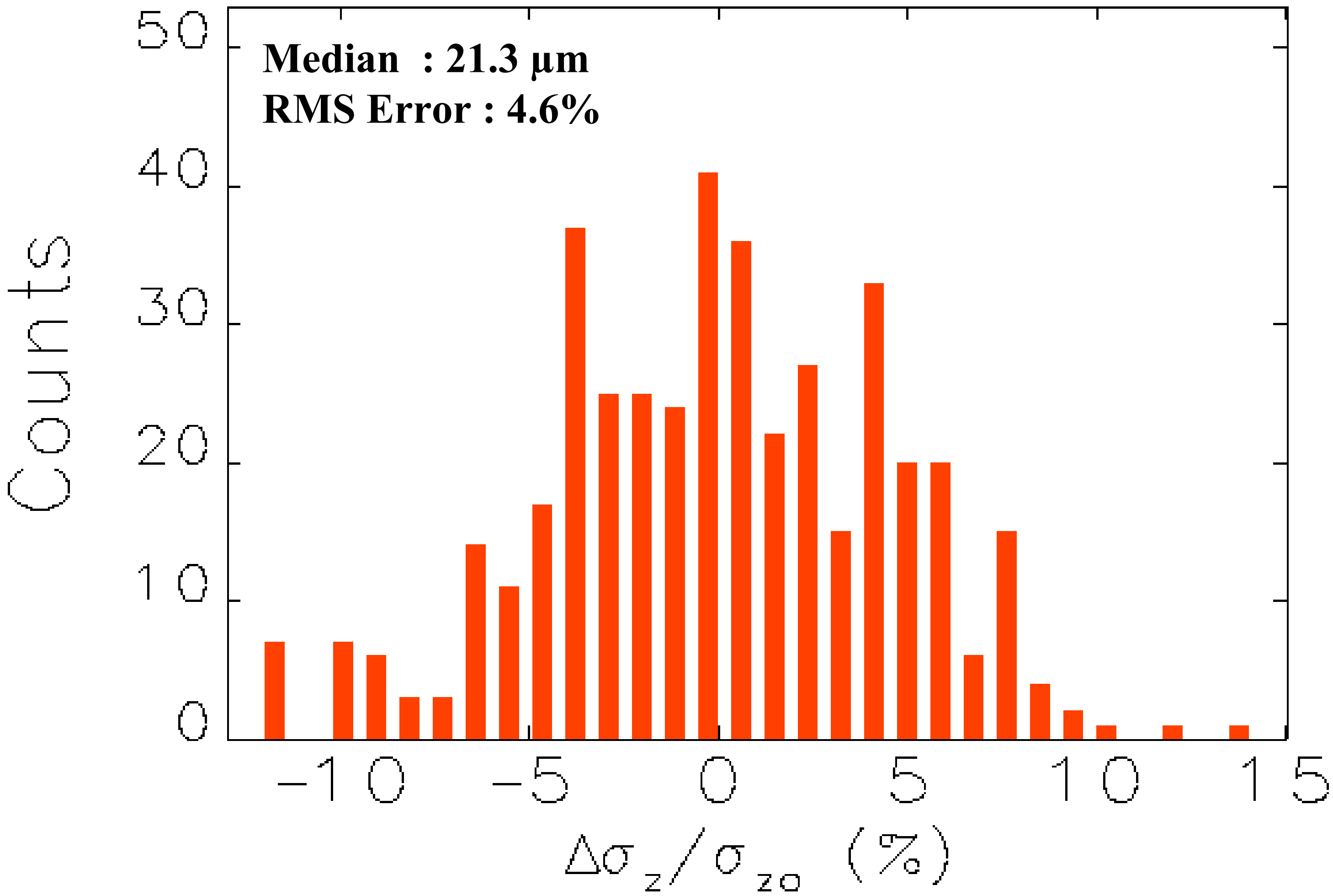

S2E simulations under FEL based Tolerances

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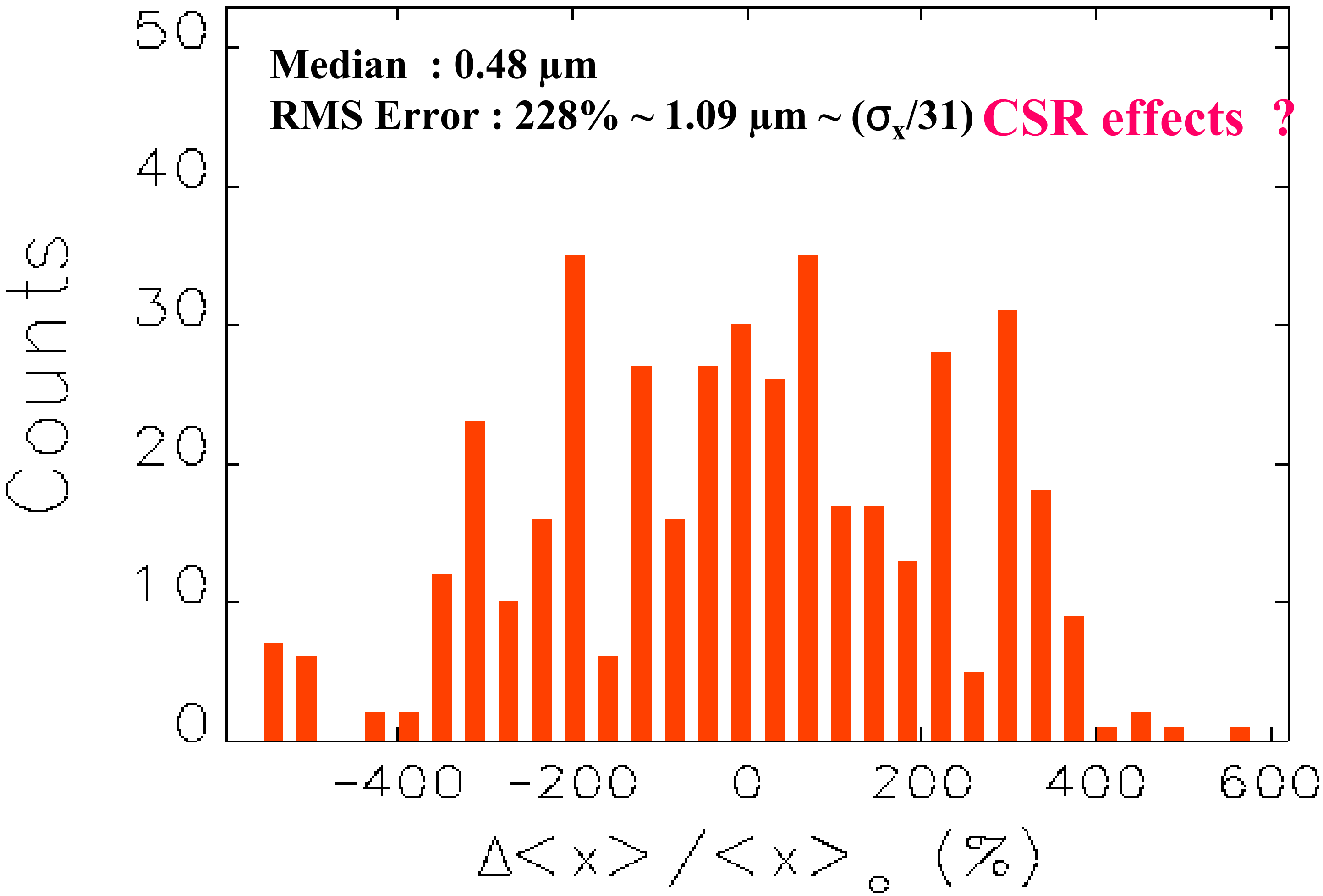
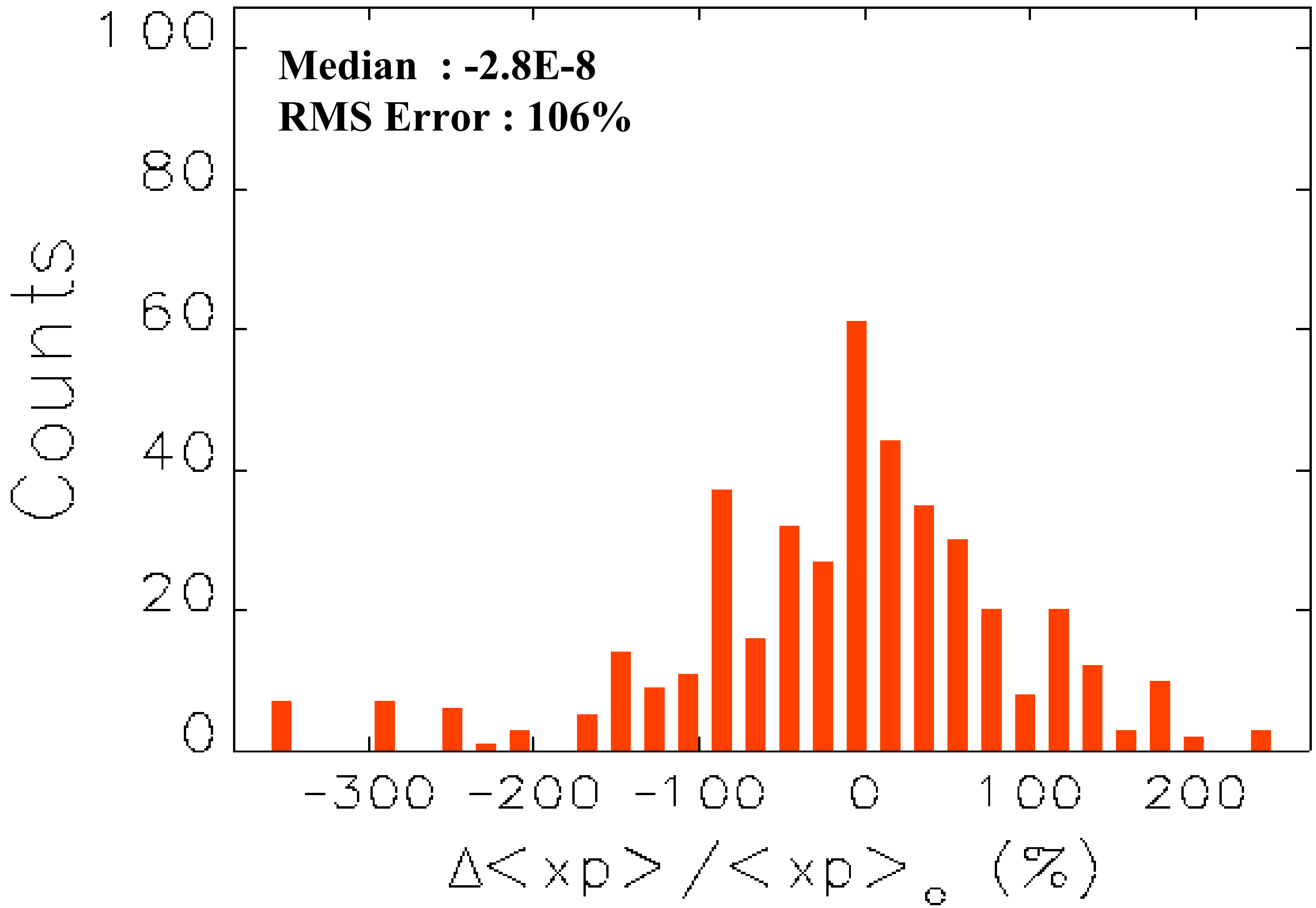
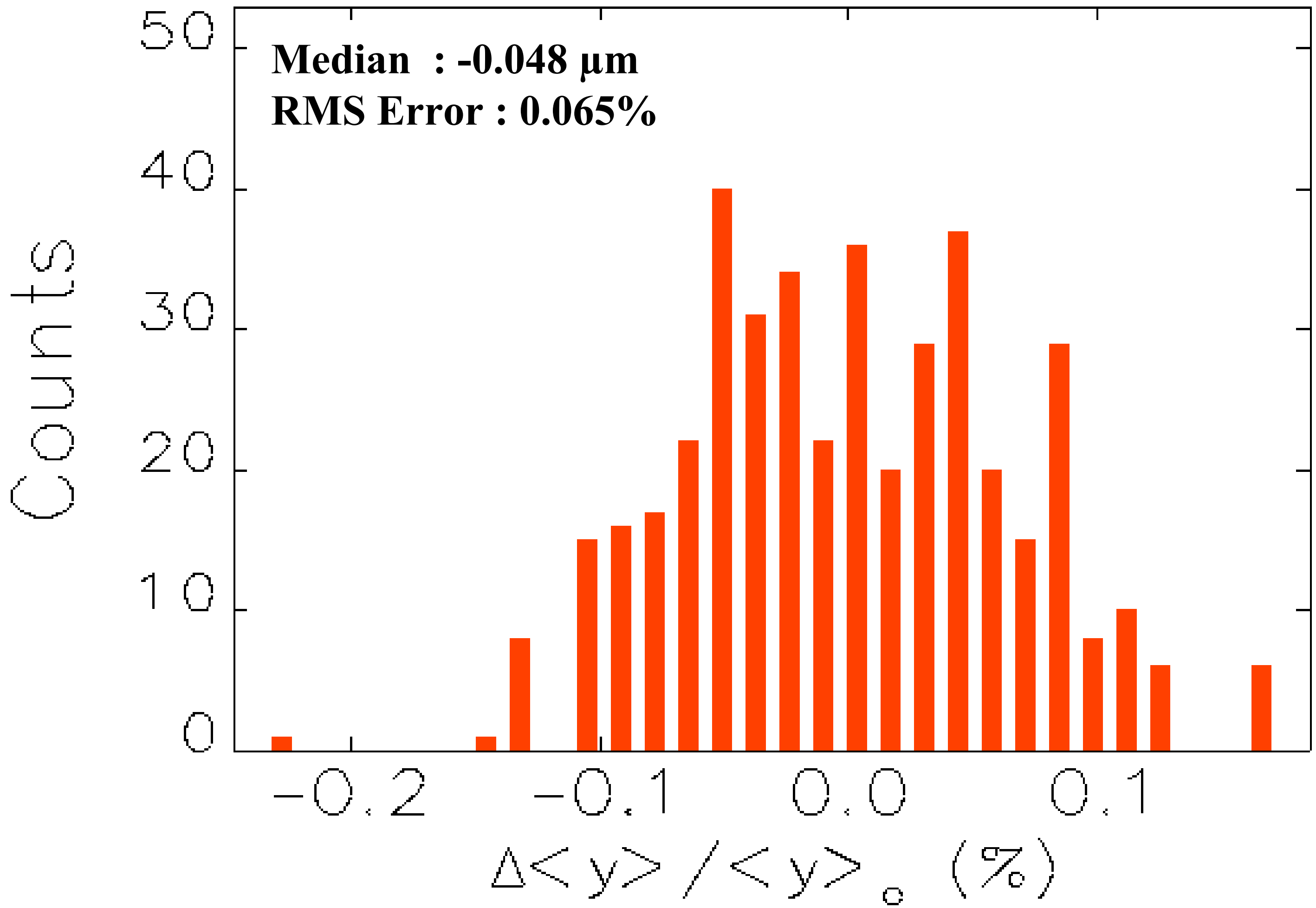


S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

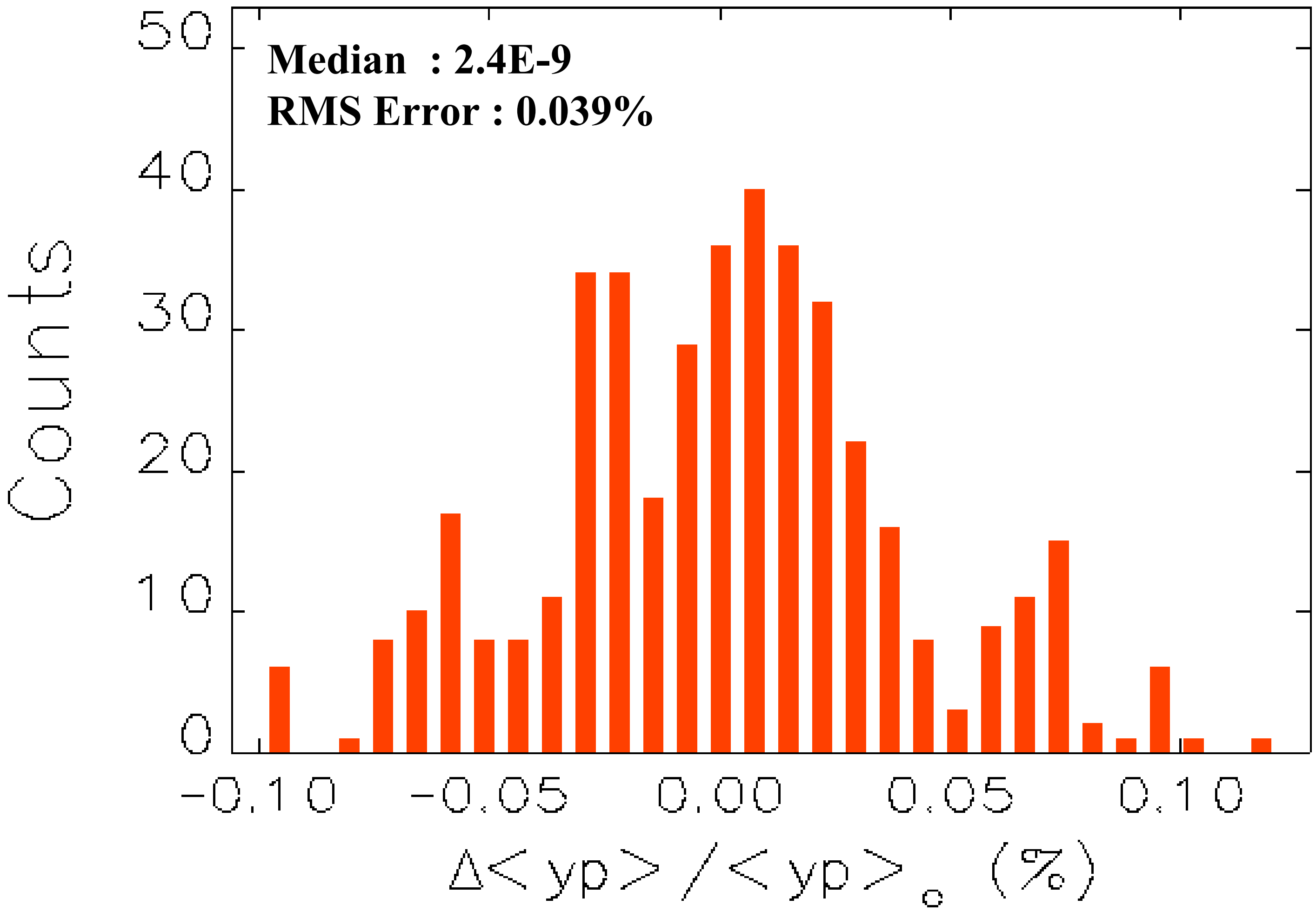


423 Times Tracking with Alternative Layout under FEL Based Tolerances



S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances



S2E simulations under FEL based Tolerances

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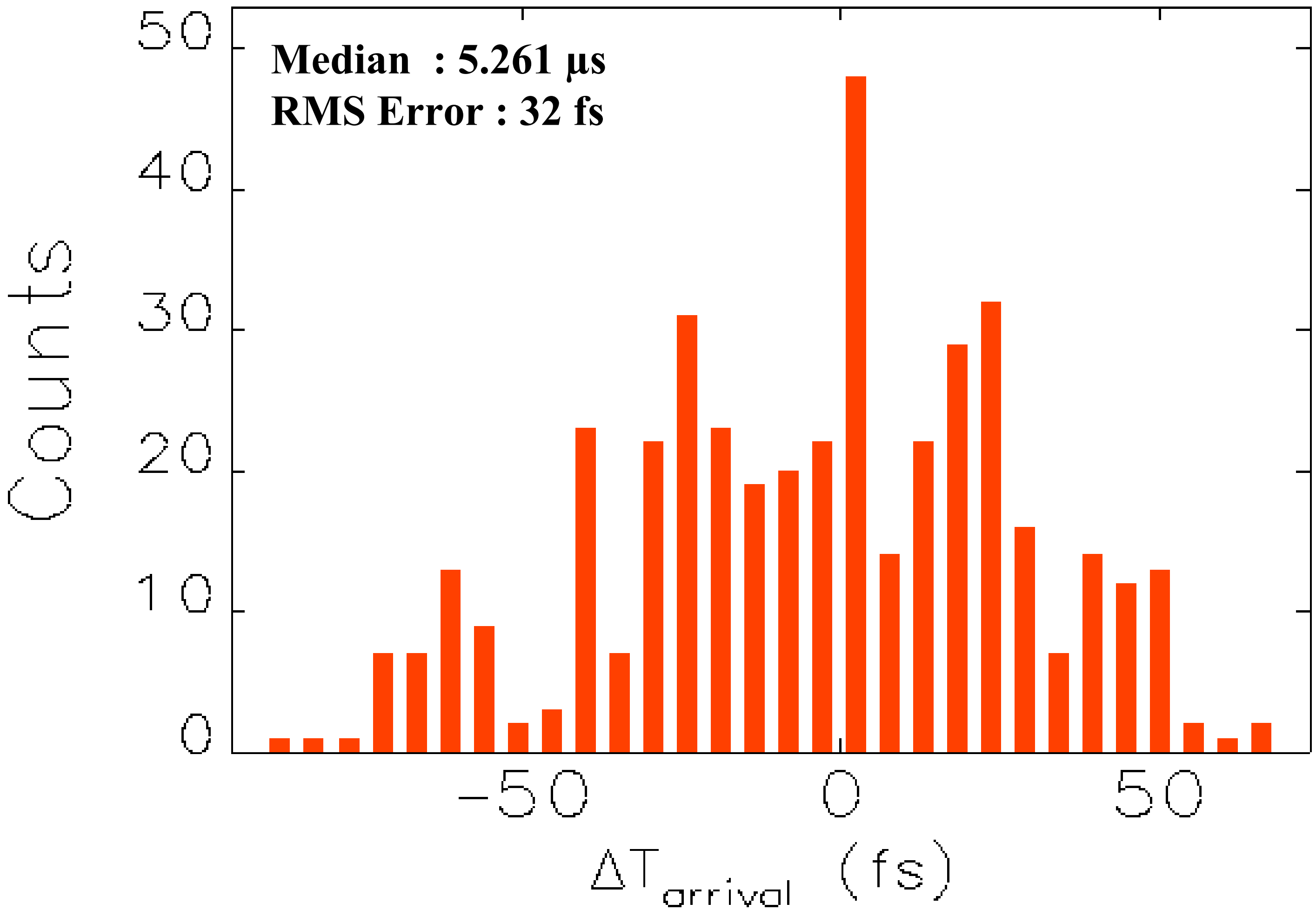

S2E simulations under FEL based Tolerances

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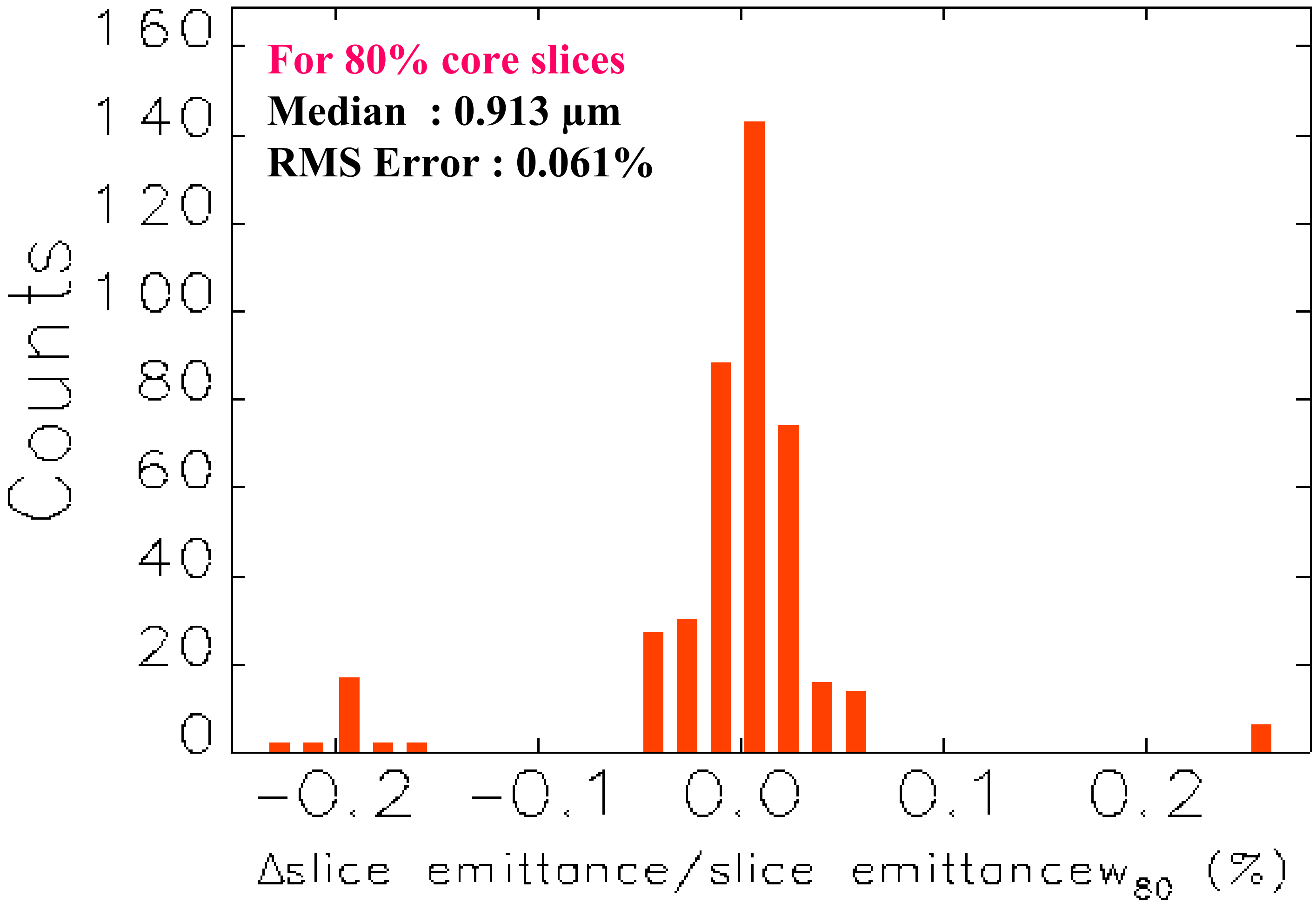

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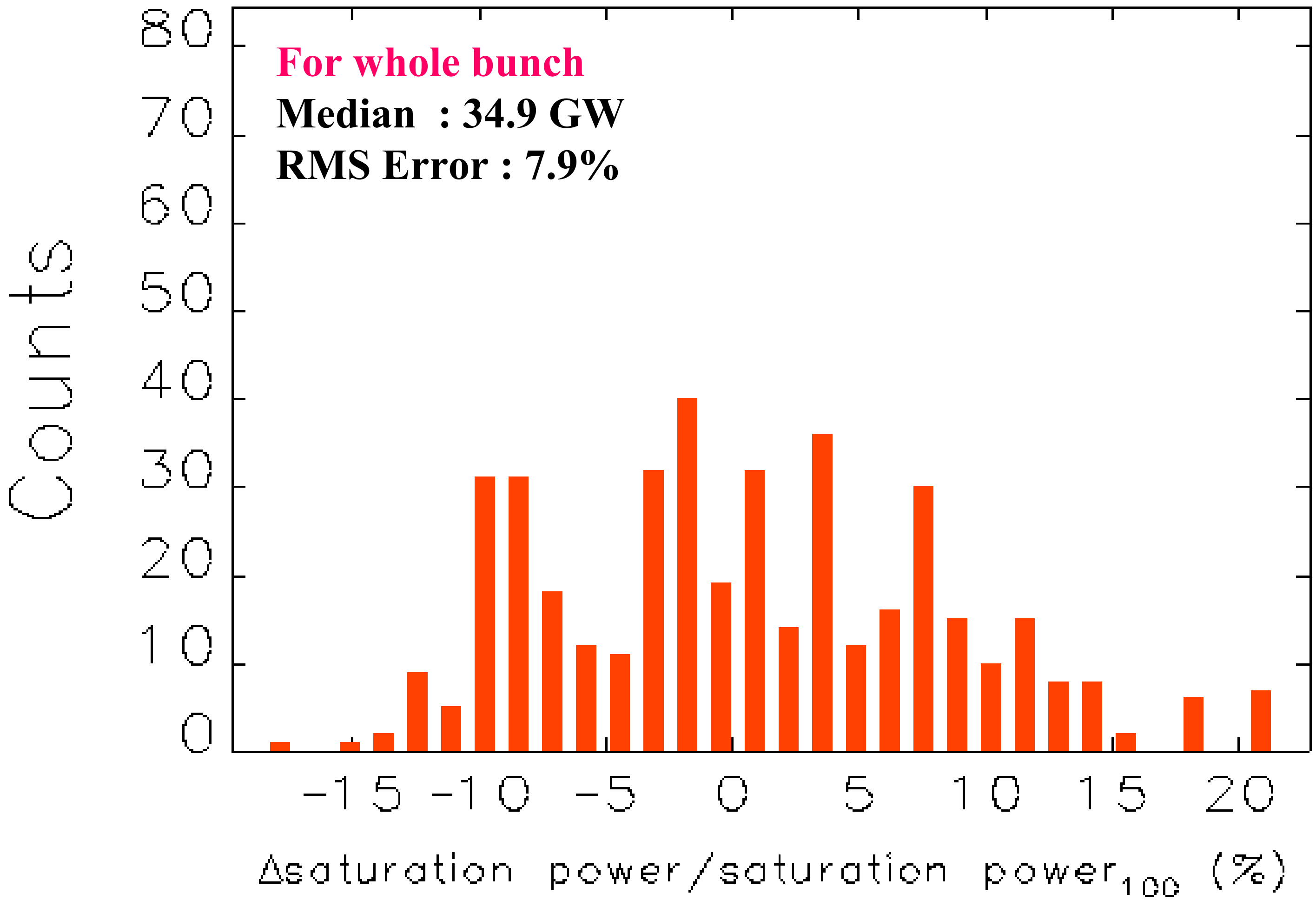

S2E simulations under FEL based Tolerances

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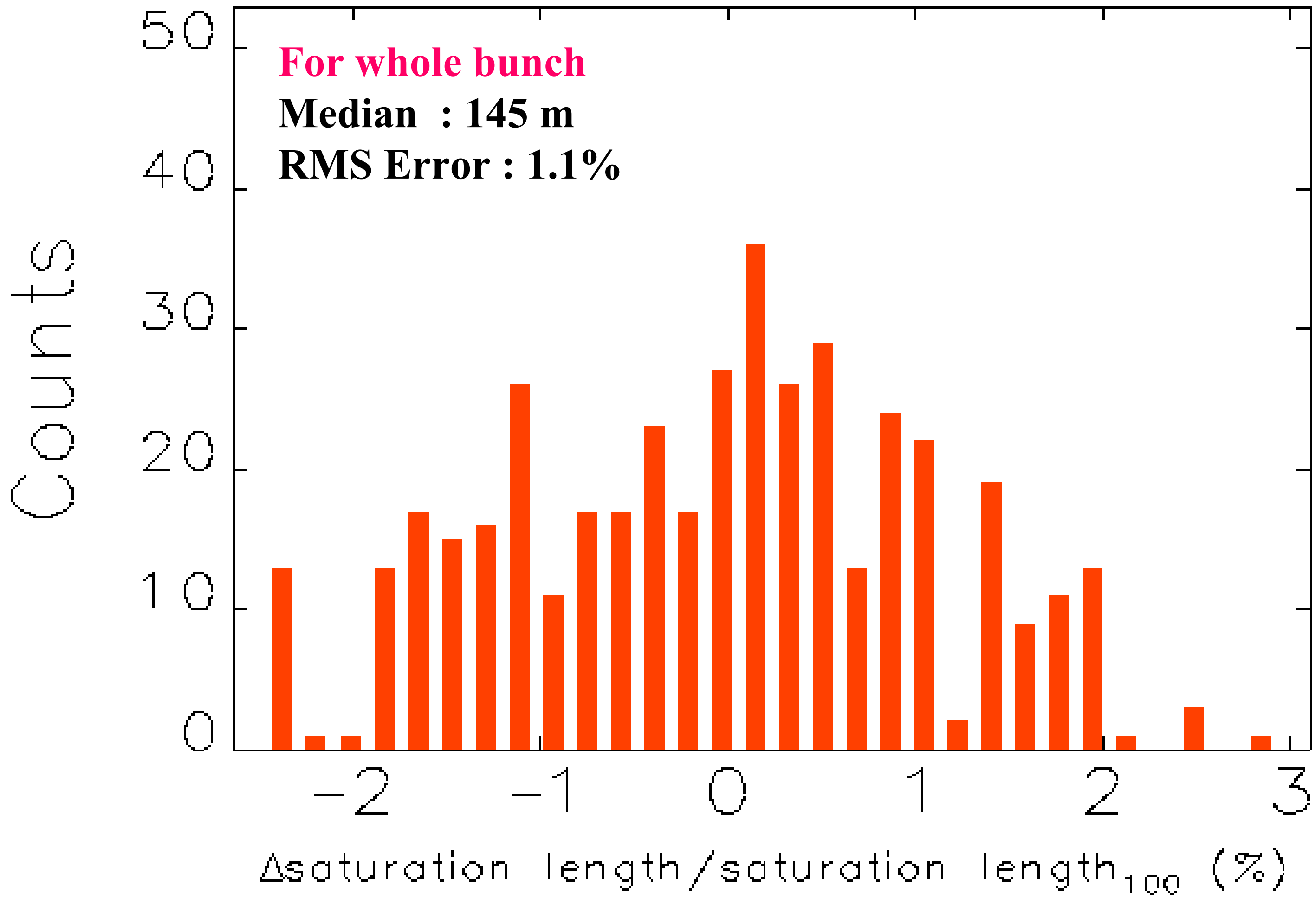

S2E simulations under FEL based Tolerances

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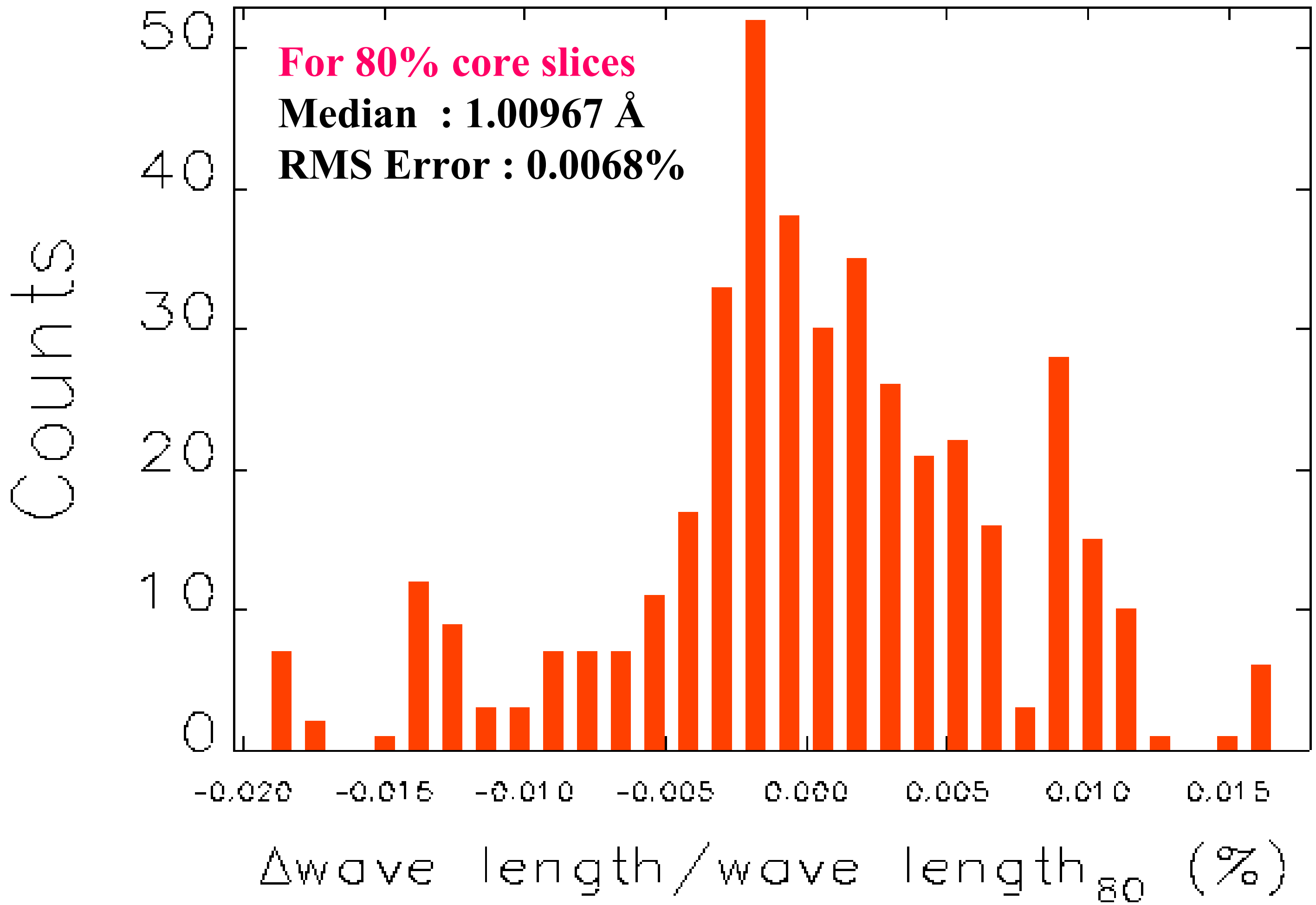

Summary

After considering the space charge force at Gun, CSR in BCs, and geometric wakefields in linac, we have investigated jitter tolerance with an alternative European XFEL layout, and compared with that of current layout.

All jitter sensitivities becomes weaker when we use alternative linac layout.

Jitter correlation with other components is also reduced when we use alternative linac layout.

If we can control all phase (voltage) errors within 0.015% (0.015 deg), jitter effect in the alternative layout is weak enough to satisfy users' requirements.

Acknowledgments

Y. Kim sincerely thanks S. Simrock, M. Borland, P. Emma, S. Schreiber, J. S. Oh, Dr. R. Brinkmann, Professor J. Rossbach , Professor I. S. Ko, Professor W. Namkung, Professor Kwang-Je Kim for their encouragements of this work and many useful comments and discussions on the jitter issues.