S2E Simulations on Jitter Issues for the European XFEL Project

- Layout (10AUG04 Version) with Two BC Stages -

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Current Layout for XFEL (13JAN04)

With Old European XFEL Injector, $\varepsilon_n = 0.90 \mu m$

Q = 1.0 nC
e-beam

$\sigma_z = 1.76$ mm $\rightarrow 113$ $\mu$m $\rightarrow 20.5$ $\mu$m

RF-GUN ACC1 ACC2 ACC3 ACC4 ACC39 BC1 BC2 ACC5 ACC6

60 MV/m 11.5 MV/m $25.0$ MV/m $20.5$ MV/m 20.5 MV/m 34.8 MV/m 160.6 deg $E = 510$ MeV $\sigma_\delta \sim 1.89\%$ $R_{56} = 87$ mm $\theta = 3.95$ deg

ASTRA with Space Charge

0.0 m $\rightarrow 12.0444$ m

$\sigma_z = 20.5$ $\mu$m

FODO MODULES

ACC7 ACC8 ACC9 ACC118

20.65 MV/m 0.0 deg

1567 m

UNDULULATOR, 250.1 m

All are projected parameters!

$E = 20.0$ GeV
$\sigma_\delta = 0.008\%$
$\sigma_x = 37.3$ $\mu$m, $\sigma_y = 31.6$ $\mu$m, $\sigma_z = 20.5$ $\mu$m
$\varepsilon_{nx} = 1.19$ $\mu$m, $\varepsilon_{ny} = 0.94$ $\mu$m

To the end of Linac: ELEGANT with CSR with geometric wakefields without space charge

TeV-Energy Superconducting Linear Accelerator Projects - TTF-2, TESLA X-ray FEL, TESLA Linear Collider
Klystron Distribution of Current Layout

Here K.No means the number of Klystron per module!

K.No = 1 2 1 1 1 2

One Klystron for 4 MODULES

One Klystron for 4 Modules, Total 29 Klystrons

UNDULATOR, 250.1 m

Multi-Klystron before BC2 reduces the jitter sensitivity in ACC234 and ACC39 modules
Alternative Layout for XFEL (10AUG04)

With New European XFEL Injector, $\varepsilon_n = 0.88 \mu m$

- $Q = 1.0 \, nC$
- $\sigma_z = 1.72 \, mm \rightarrow 94 \, \mu m \rightarrow 21.6 \, \mu m$
- $E = 518 \, MeV$
  - $\sigma_\delta \sim 1.87\%$
  - $R_{56} = 87 \, mm$
  - $\theta = 3.95 \, deg$

- $E = 518-760-1100 \, MeV$
  - $\sigma_\delta \sim 1.87-1.33-0.9\%$
  - $R_{56} \sim 5.3 \, mm$
  - $\theta \sim 0.93 \, deg$

RF-GUN \rightarrow ACC1 \rightarrow ACC2 \rightarrow ACC3 \rightarrow ACC4 \rightarrow ACC39 \rightarrow BC1 \rightarrow ACC5 \rightarrow ACC6 \rightarrow BC2

ASTRA with Space Charge
- 0.0 m
- 12.9869 m

$\sigma_z = 21.6 \, \mu m$

To the end of Linac: ELEGANT with CSR
- with geometric wakefields
- without space charge

FODO MODULES
- ACC7 \rightarrow ACC8 \rightarrow ACC9 \rightarrow ACC120
- $E = 20.0 \, GeV$
- $\sigma_\delta = 0.0088\%$
- $\sigma_x = 34.2 \, \mu m$, $\sigma_y = 29.5 \, \mu m$, $\sigma_z = 21.6 \, \mu m$
- $\varepsilon_{nx} = 1.044 \, \mu m$, $\varepsilon_{ny} = 0.896 \, \mu m$

UNDULATORATOR, 250.1 m

All are projected parameters!
Klystron Distribution of Alternative Layout

Here K.No means the number of Klystron per module!

RF-GUN ACC1 ACC2 ACC3 ACC4 ACC39 BC1 ACC5 ACC6 BC2

K.No = 1 2 1 1 1 2 1 1

One Klystron for 4 Modules, Total 29 Klystrons

ACC7 ACC8 ACC9 ACC120

UNDULATOR, 250.1 m

Multi-Klystron before BC2 reduces the jitter sensitivity in ACC234, ACC39, and ACC56
Papers On Two Linac Layouts for XFEL

On Current Linac Layout (13JAN04 Version) with a Double Chicane

S2E simulation on Linac Optimization:
APAC2004, EPAC2004
by Yujong Kim, K. Flöttmann, T. Limberg, M. Dohlus, and D. Son

S2E Simulations on Jitter:
EPAC2004
by Yujong Kim, K. Flöttmann, and T. Limberg, and D. Son

On Alternative Linac Layout (10AUG04 Version) with Two BC Stages

S2E simulation on Linac Optimization:
LINAC2004
by Yujong Kim, K. Flöttmann, T. Limberg, and D. Son

S2E Simulations on Jitter:
Not yet reported due to limited available computer, maybe, at PAC2005
## Sensitivity & Tolerance Set for Current Layout

Linac Performance Based Tolerance (refer to our EPAC2004 paper)

For each Klystron

<table>
<thead>
<tr>
<th></th>
<th>Sensitivity</th>
<th>TOL-I (rms)</th>
<th>TOL-II (rms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>dT</td>
<td>0.50 ps</td>
<td>0.1 ps</td>
<td>0.3 ps</td>
</tr>
<tr>
<td>dQ</td>
<td>-6.10%</td>
<td>1.0%</td>
<td>1.5%</td>
</tr>
<tr>
<td>ACC1C1234 Phase</td>
<td>0.20 deg</td>
<td>0.05 deg</td>
<td>0.07 deg</td>
</tr>
<tr>
<td>ACC1C1234 dV/V</td>
<td>-0.17%</td>
<td>0.02%</td>
<td>0.03%</td>
</tr>
<tr>
<td>ACC1C5678 Phase</td>
<td>0.10 deg</td>
<td>0.05 deg</td>
<td>0.07 deg</td>
</tr>
<tr>
<td>ACC1C5678 dV/V</td>
<td>-0.08%</td>
<td>0.02%</td>
<td>0.03%</td>
</tr>
<tr>
<td>ACC234 Phase</td>
<td>-0.056 deg</td>
<td>0.05 deg</td>
<td>0.07 deg</td>
</tr>
<tr>
<td>ACC234 dV/V</td>
<td>-0.06%</td>
<td>0.02%</td>
<td>0.03%</td>
</tr>
<tr>
<td>ACC39 Phase</td>
<td>-0.08 deg</td>
<td>0.05 deg</td>
<td>0.07 deg</td>
</tr>
<tr>
<td>ACC39 dV/V</td>
<td>0.19%</td>
<td>0.02%</td>
<td>0.03%</td>
</tr>
<tr>
<td>BC1 dI/I</td>
<td>0.02%</td>
<td>0.02%</td>
<td>0.02%</td>
</tr>
<tr>
<td>BC2 dI/I</td>
<td>0.31%</td>
<td>0.02%</td>
<td>0.02%</td>
</tr>
<tr>
<td>ACC5678 Phase</td>
<td>4.19 deg</td>
<td>0.05 deg</td>
<td>0.07 deg</td>
</tr>
<tr>
<td>ACC5678 dV/V</td>
<td>0.028%</td>
<td>0.02%</td>
<td>0.03%</td>
</tr>
</tbody>
</table>
S2E Simulations Under Same Jitter Tolerances

- **p2p phase error** = 3*0.05 deg
- **p2p amplitude error** = 3*0.02%

**p2p current error** = 3*0.02%

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After applying random error set (p2p = 3 × tolerance) to each component, we have performed about 400 times S2E simulations from gun to the end of linac to compare two linac layouts under same jitter tolerance set (TOL-I).
Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Current Layout  400 Times Tracking with Alternative Layout

most sensitive jitter source on bunch length = ACC2 phase error

wider change in bunch length for current layout
stronger correlation with errors in other components!
Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Current Layout  
400 Times Tracking with Alternative Layout

most sensitive jitter source on arriving time = BC1 current error

wider change in bunch arriving time for current layout stronger correlation with errors in other components!
Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Current Layout  400 Times Tracking with Alternative Layout

most sensitive jitter source on p2p energy deviation = ACC2 phase error

wider change in p2p energy deviation for current layout
stronger correlation with errors in other components!
Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Current Layout  400 Times Tracking with Alternative Layout

most sensitive jitter source on average energy = DBC2 voltage error

![Graph 1: ΔE/E₀ vs change in ACC5678 dV/V (%)]

![Graph 2: ΔE/E₀ vs change in ACC78910 dV/V (%)]

similar change in average energy for both layouts
DBC2 is exactly same for both linac layouts
Comparison Two Layouts Under TOL-I Set

400 Times Tracking with Current Layout

For whole bunch
Median : 41.8 GW
RMS Error : 40%

Counts

Δsaturation power/saturation power\textsubscript{100} (\%)

400 Times Tracking with Alternative Layout

For whole bunch
Median : 35.4 GW
RMS Error : 30.9%

Counts

Δsaturation power/saturation power\textsubscript{100} (\%)
According to Dr. Simrock’s LINAC2004 Talk:

For both 1.3 GHz TESLA Module & 3.9 GHz 3\textsuperscript{rd} Harmonic Module

For the short term period (1 min)
RF Phase Error < 0.02 degree (rms)
RF Amplitude Error (dV/V) < 0.02\% (rms)

Controllable jitter tolerance depends on charge fluctuation!

\[ Q = Q_0 (1 + 0.03 \Delta \phi_1)(1 + (\Delta E / E)_1)(1 + (\Delta V / V)_g) \]

Dr. Simrock confirmed that these can be reduced to 0.01 deg and 0.01\% soon.
New Threshold of Jitter Sensitivity

By the help of S2E simulations, let’s apply artificial jitter or error to all important components (GUN, ACC1 ~ ACC120, ACC39, BC1 and BC2) in order to investigate the jitter sensitivity $J_s$ of those components on the FEL performance at the undulator (SASE1).

After considering controllable jitter tolerances in the near future, we have determined new thresholds of jitter sensitivity, which are related with FEL performance (Applying Ming Xie Model to SASE1):

- Peak-to-peak (p2p) change in SASE source wavelength should be within ±0.022%
- Peak-to-peak (p2p) change in saturation length should be within ±1.6%
- Peak-to-peak (p2p) change in saturation power should be within ±15%
- Peak-to-peak (p2p) change in bunch arrival time should be within 36 fs (=0.5$\sigma_z$)

Then choose the jitter tolerance $J_t$ which gives

$$\sqrt{\sum_{i=1}^{n} \left( \frac{J_{t,i}}{J_{s,i}} \right)^2} < 1$$

Then we have checked overall FEL performance under random tolerances set by repeating about 400 times S2E simulations.
Most Sensitive Sources to FEL Performances

**Alternative Layout with 2BC**

ACC78910 dV/V is the most sensitive jitter source to wavelength
ACC234 Phase is the most sensitive jitter source to saturation length

![Graph showing change in SASE wavelength with change in ACC78910 dV/V](image1)

- p2p sensitivity in wavelength $\sim \pm 0.06\%$
- p2p change in wavelength $\sim \pm 0.022\%$

![Graph showing change in saturation length with change in ACC2 phase](image2)

- p2p sensitivity in sat. length $\sim \pm 0.06$ deg
- p2p change in sat. length $\sim \pm 1.6$%
Most Sensitive Sources to FEL Performances

Alternative Layout with 2BC

ACC234 Phase is the most sensitive jitter source to saturation power BC1 dI/I is the most sensitive jitter source to arriving time

p2p sensitivity in sat. power $\sim \pm 0.06\%$
p2p change in sat. power $\sim \pm 15\%$
p2p sensitivity in arriving time $\sim \pm 0.004\%$
p2p change in arriving time $\sim \pm 36$ fs
Most Sensitive Sources to FEL Performances

Alternative Layout with 2BC

ACC234 Phase is the most sensitive jitter source to saturation power and saturation length

weak over-compression against ACC234 phase error
Most Sensitive Sources to FEL Performances

Current Layout with Double Chicane

ACC234 Phase is the most sensitive jitter source to saturation power and saturation length

strong over-compression against ACC234 phase error
## Sensitivity & Tolerance for Alternative Layout

### FEL Performance Based Tolerance

<table>
<thead>
<tr>
<th></th>
<th>Sensitivity((p2p))</th>
<th>Tol. ((p2p))</th>
<th>Tol. ((\text{rms}))</th>
<th>Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td>(dT)</td>
<td>(\pm 0.729) ps</td>
<td>(\pm 0.300) ps</td>
<td>0.100 ps</td>
<td>saturation length</td>
</tr>
<tr>
<td>(dQ/Q)</td>
<td>(\pm 5.452)%</td>
<td>(\pm 3.000)%</td>
<td>1.000%</td>
<td>saturation length</td>
</tr>
<tr>
<td>ACC1C1234 phase</td>
<td>(\pm 0.133) deg</td>
<td>(\pm 0.045) deg</td>
<td>0.015 deg</td>
<td>saturation length</td>
</tr>
<tr>
<td>ACC1C1234 dV/V</td>
<td>(\pm 0.129)%</td>
<td>(\pm 0.045)%</td>
<td>0.015%</td>
<td>arriving time</td>
</tr>
<tr>
<td>ACC1C5678 phase</td>
<td>(\pm 0.072) deg</td>
<td>(\pm 0.045) deg</td>
<td>0.015 deg</td>
<td>saturation power</td>
</tr>
<tr>
<td>ACC1C5678 dV/V</td>
<td>(\pm 0.063)%</td>
<td>(\pm 0.045)%</td>
<td>0.015%</td>
<td>arriving time</td>
</tr>
<tr>
<td>ACC234 phase</td>
<td>(\pm 0.048) deg</td>
<td>(\pm 0.045) deg</td>
<td>0.015 deg</td>
<td>arriving time</td>
</tr>
<tr>
<td>ACC234 dV/V</td>
<td>(\pm 0.045)%</td>
<td>(\pm 0.045)%</td>
<td>0.015%</td>
<td>arriving time</td>
</tr>
<tr>
<td>ACC39 phase</td>
<td>(\pm 0.064) deg</td>
<td>(\pm 0.045) deg</td>
<td>0.015 deg</td>
<td>saturation power</td>
</tr>
<tr>
<td>ACC39 dV/V</td>
<td>(\pm 0.142)%</td>
<td>(\pm 0.045)%</td>
<td>0.015%</td>
<td>arriving time</td>
</tr>
<tr>
<td>BC1 dI/I</td>
<td>(\pm 0.013)%</td>
<td>(\pm 0.012)%</td>
<td>0.004%</td>
<td>arriving time</td>
</tr>
<tr>
<td>ACC56 phase</td>
<td>(\pm 0.721) deg</td>
<td>(\pm 0.045) deg</td>
<td>0.015 deg</td>
<td>arriving time</td>
</tr>
<tr>
<td>ACC56 dV/V</td>
<td>(\pm 0.913)%</td>
<td>(\pm 0.045)%</td>
<td>0.015%</td>
<td>saturation length</td>
</tr>
<tr>
<td>BC2 dI/I</td>
<td>(\pm 0.201)%</td>
<td>(\pm 0.012)%</td>
<td>0.004%</td>
<td>arriving time</td>
</tr>
<tr>
<td>ACC78910 phase</td>
<td>(\pm 10.037) deg</td>
<td>(\pm 0.045) deg</td>
<td>0.015 deg</td>
<td>SASE wavelength</td>
</tr>
<tr>
<td>ACC78910 dV/V</td>
<td>(\pm 0.060)%</td>
<td>(\pm 0.045)%</td>
<td>0.015%</td>
<td>SASE wavelength</td>
</tr>
</tbody>
</table>
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

Median : 20.001 GeV
RMS Error : 0.0034%
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

Median : 0.0089%
RMS Error : 0.0004%
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

Median : 21.3 μm
RMS Error : 4.6%

Counts

Δσ_z/σ_{z0} (%)
S2E simulations under **FEL based Tolerances**

423 Times Tracking with Alternative Layout under FEL Based Tolerances

- Median : 0.48 μm
- RMS Error : 228% ~ 1.09 μm ~ (σ_x/31) **CSR effects**

![Histogram with counts and Δ<x> / <x> (in %)]
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

Median : -2.8E-8
RMS Error : 106%
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

Median : -0.048 μm
RMS Error : 0.065%
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

Median : 2.4E-9
RMS Error : 0.039%
423 Times Tracking with Alternative Layout under FEL Based Tolerances

Median : 5.261 µs
RMS Error : 32 fs

Counts

$\Delta T_{\text{arrival}}$ (fs)

0
10
20
30
40
50

0
50
-50
0
50
423 Times Tracking with Alternative Layout under FEL Based Tolerances

For 80% core slices
Median : 0.913 μm
RMS Error : 0.061%
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

For whole bunch
Median : 34.9 GW
RMS Error : 7.9%

Counts

Δsaturation power/saturation power_{100} (%)
S2E simulations under FEL based Tolerances

423 Times Tracking with Alternative Layout under FEL Based Tolerances

For whole bunch
Median : 145 m
RMS Error : 1.1%
S2E simulations under **FEL based Tolerances**

423 Times Tracking with Alternative Layout under FEL Based Tolerances

For 80% core slices
Median : 1.00967 Å
RMS Error : 0.0068%
After considering the space charge force at Gun, CSR in BCs, and geometric wakefields in linac, we have investigated jitter tolerance with an alternative European XFEL layout, and compared with that of current layout.

All jitter sensitivities becomes weaker when we use alternative linac layout.

Jitter correlation with other components is also reduced when we use alternative linac layout.

If we can control all phase (voltage) errors within 0.015% (0.015 deg), jitter effect in the alternative layout is weak enough to satisfy users’ requirements.
Acknowledgments

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