Optimising CMOS Pixel Sensors for the ILC Micro-Vertex Detector

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on behalf of DAPNIA/Saclay, LPSC/Grenoble, LPC/Clermont-F., DESY, Uni. Hamburg, JINR-Dubna & IPHC/Strasbourg

contributions from IPN/Lyon, Uni. Frankfurt, GSI-Darmstadt, STAR coll.(LBNL, BNL)

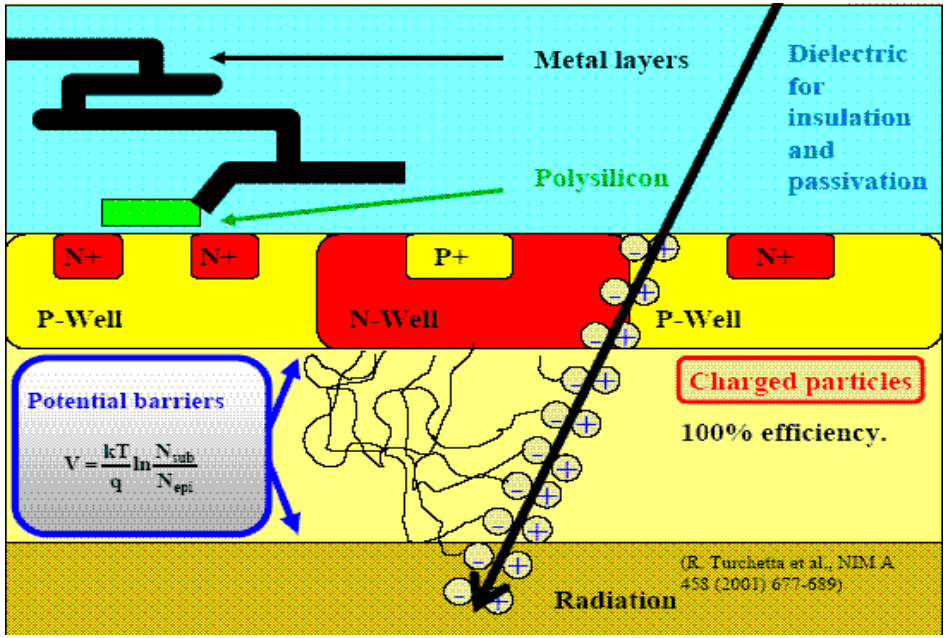
▷ **More information on IPHC Web site:** **http://wwwires.in2p3.fr/ires/web2/rubrique.php3?id_rubrique=63**

OUTLINE

- **Reminder on CMOS sensors:** Specific advantages — Vertexing applications
- **Achieved performances** (AMS-0.35 OPTO fab. process) :
  - Detection efficiency — Spatial resolution — Operating temperature — Radiation tolerance
- **Fast read-out architecture:** Progress since May 2005 — Plans until 2009
- **Summary**

Main Features and Advantages of CMOS Sensors

- p-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    $Q \sim 80$ e-h / $\mu m \mapsto$ signal $\lesssim 1000$ e$^-$
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode with help of reflection on boundaries with p-well and substrate (high doping)

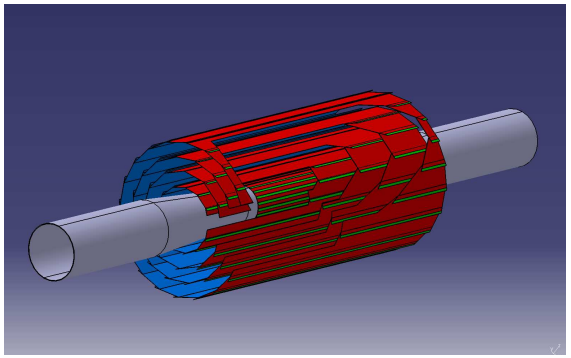


- Specific advantages of CMOS sensors:
  - ◇ Signal processing μcircuits integrated on sensor substrate (system-on-chip) $\mapsto$ compact, flexible
  - ◇ Sensitive volume ($\sim$ epitaxial layer) is $\sim$ 10–15 μm thick $\longrightarrow$ thinning to $\lesssim$ 30 μm permitted
  - ◇ Standard, massive production, fabrication technology $\longrightarrow$ cheap, fast turn-over
  - ◇ Room temperature operation
  - ◇ Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation
    - ⋈ Very thin sensitive volume $\rightarrowtail$ impact on signal magnitude (mV !)
    - ⋈ Sensitive volume almost undepleted $\rightarrowtail$ impact on radiation tolerance & speed
    - ⋈ Commercial fabrication (parameters) $\rightarrowtail$ impact on sensing performances & radiation tolerance

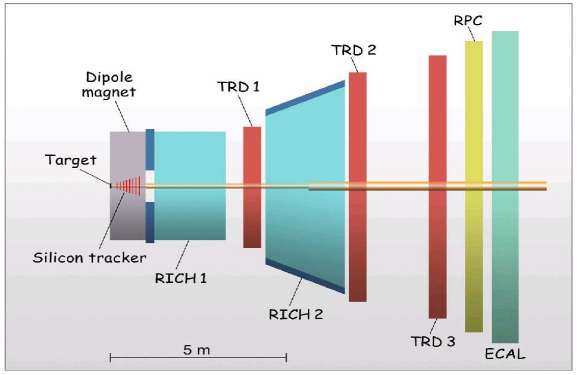
Vertexing Applications of MIMOSA Sensors

- **Vertex Detector upgrade for STAR expt at RHIC**
  - **2–3 cylindral layers : $\sim$ 2000/3000 cm^2**
  - **$\sim$ 500 millions pixels ($\leq$ 30 μm pitch)**
  - **2 steps : 2008 (analog outputs) & 2011 (digital outputs)**

- **Beam telescope (FP6 project EUDET)**
  - **2 arms of 3 planes (plus 1 high resolution plane)**
  - **provide $\lesssim$ 1 μm resolution on 3 GeV e$^-$ beam (DESY)**
  - **2 steps : 2007 (analog outputs) & 2009 (digital outputs)**



- **ILC vertex detector (option)**
  - **5–6 cylindrical layers : $\gtrsim$ 3000 cm^2**
  - **300-500 milion pixels (20–40 μm pitch)**
  - **1st complete ladder prototype $\sim$ 2010**

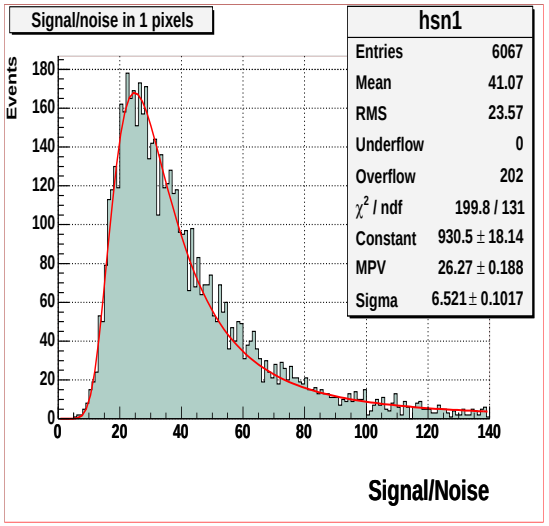


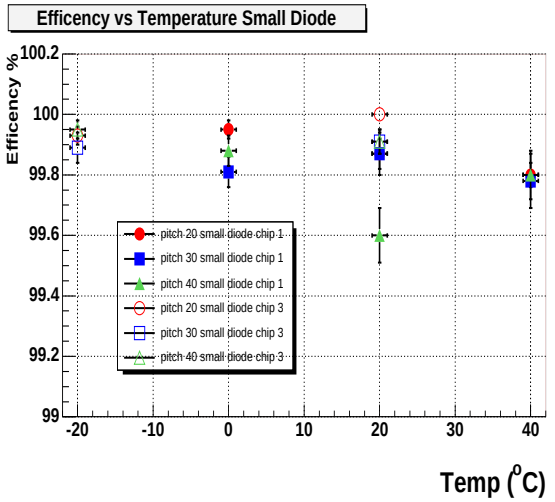
- **CBM vertex detector (FAIR/GSI)**
  - **3 rectangular layers : $\sim$ 2000 cm^2**
  - **200–300 milion pixels ($\sim$ 20–30 μm pitch)**

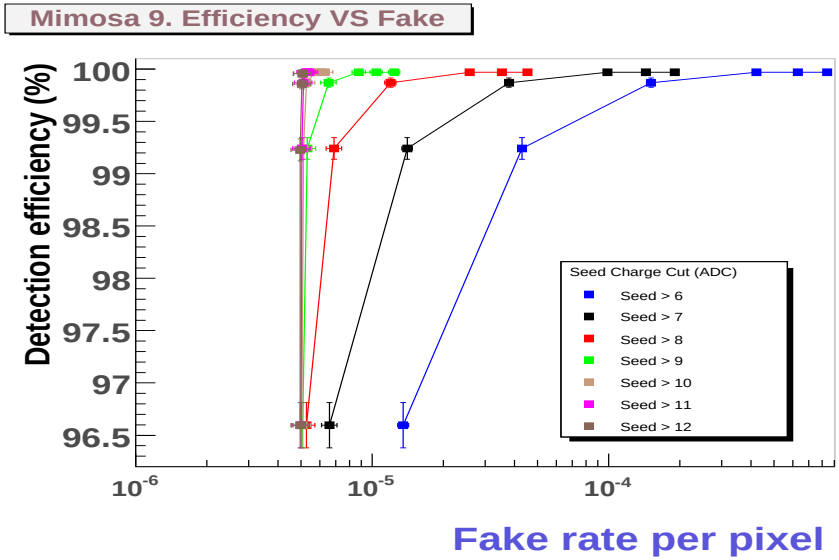
Detection Efficiency

Numerous MIMOSA chips tested on H.E. beams (SPS, DESY) $\mapsto$ well established perfo. (analog output):

- **Best performing technology: AMS 0.35 μm OPTO**
  ($\sim$ 11 μm epitaxy $\rightarrowtail$ "20 μm" option being tested)
- **N $\sim$ 10 e^- $\mapsto$ S/N $\gtrsim$ 20 – 30 (MPV) $\Rrightarrow$ ϵ_{det} $\gtrsim$ 99.5 %**
- **$T_{oper.}$ $\gtrsim$ 40 °C**
- **Technology without epitaxy also performing well :**
  very high S/N but large clusters (hit separation $\searrow$)
- **Macroscopic sensors : MIMOSA-5 ($\sim$ 3.5 cm^2; 1 Mpix)**
  MIMOSA-20 (1x2 cm^2; 200 kpix)
  MIMOSA-17 (0.8x0.8 cm^2; 65 kpix)







Efficiency vs rate of fake clusters :

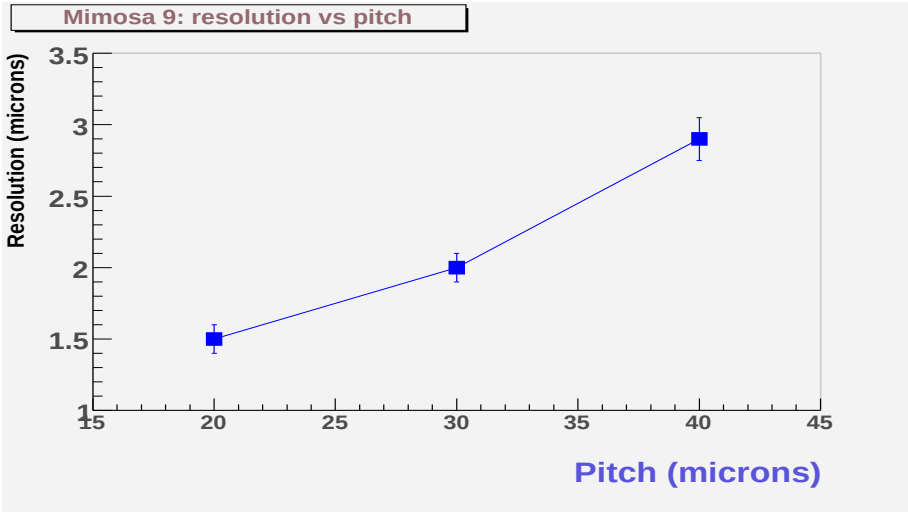
- **vary cut on seed pixel : 6 $\rightarrowtail$ 12 ADC units (N $\sim$ 1.5 u.ADC)**
- **vary cut on Σ of crown charge : 0, 3, 4, 9, 13, 17 ADC units**

$\Rrightarrow$ **ϵ_{det} $\sim$ 99.9 % for fake rate $\sim$ 10^{-5}**

Spatial Resolution (vs ADC resolution)

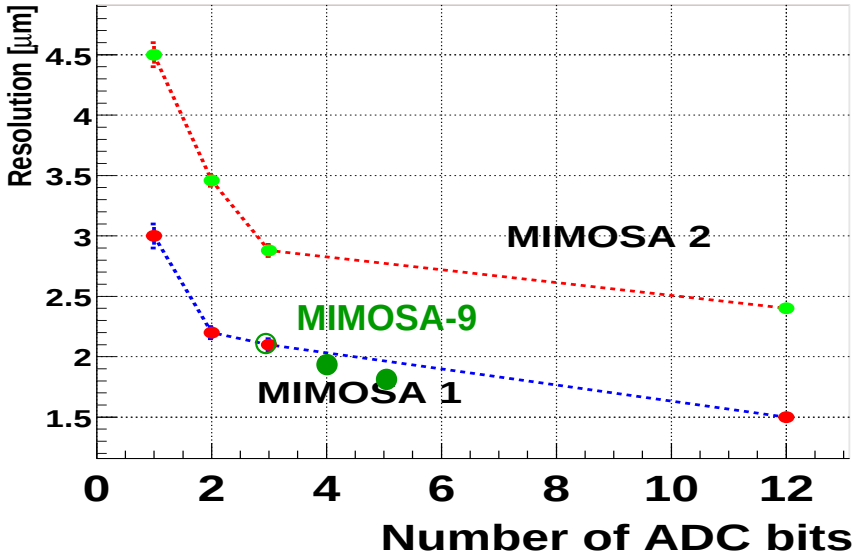
Single point resolution versus pixel pitch:

- clusters reconstructed with eta-function, exploiting charge sharing between pixels
- $\sigma_{sp} \sim 1.5\ \mu m$ (20 μm pitch)
  $\longmapsto \sigma_{sp} \lesssim 3\ \mu m$ (40 μm pitch)
- obtained with signal charge encoded on 12 bits



σ_{sp} dependence on ADC granularity:

- minimise number of ADC bits
  $\longmapsto$ minimise dimensions, $t_{r.o.}$ & P_{diss}
- effect simulated on real MIMOSA data
  (20 μm pitch ; 120 GeV/c π^- beam)



- ▷▷ $\sigma_{sp} < 2\ \mu m$ (4 bits) $\longmapsto$ 1.7–1.6 μm (5 bits)
  (MIMOSA-9 : 20 μm pitch; T= + 20°C)
- Warning : results based on simple pixel (N $\lesssim$ 10 e^- ENC)
  $\Rightarrow$ rad. tol. pixel integrating CDS (N $\lesssim$ 15 e^- ENC) not yet evaluated

AMS 0.35 OPTO engineering run (fabricated in Summer 2006):

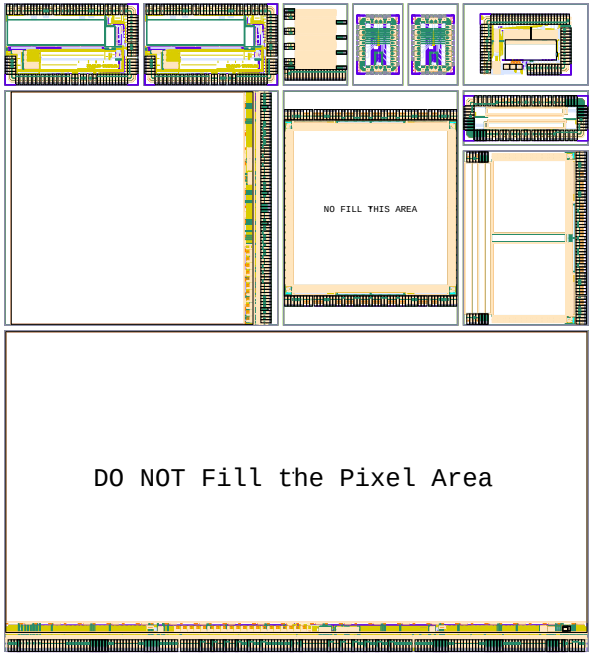
≙ 2 + 4 wafers (8" ⇛ 50 reticles/wafer) ≙ 2 epitaxy thicknesses : $\sim$ 11 & 15 μm ⇔ "14 μm" & "20 μm" options

◇ triggered by MIMO★-3 (= MIMOSA-20) fabrication :

200 kpixels, $\sim$ 2 cm^2, 2 // outputs, $t_{r.o.} \lesssim$ 4 ms

◇ includes 8 other chips :

- ✳ MIMOSA-16 : fast col. // archi. like MIMOSA-8
- ✳ MIMOSA-17 (MIMO★-3M) : 0.8 x 0.8 cm^2, rad.tol., 800 μs
  - ↪ EUDET beam telescope arms, CBM Vx Det. demonstrator
- ✳ MIMOSA-18 (IMAGER) : precision $\lesssim$ 1 μm (EUDET: DUT)
- ✳ MIMOSA-19 bio-med. imaging: special diode shape
- ✳ test structures : in-pixel amplification, discrimination, ...
- ✳ ADCs: flash from LPCC



< $\sim$ 20 mm >

Status of tests:

◇ 2 wafers tested in 2006 (1 with "14" & 1 with "20" μm epitaxy) ↦ fab. mistake (non uniform effect on sensors)

↪ not dramatic: "20 μm" option was characterised with ^{55}Fe source

◇ Second batch fabricated in 2007 ↦ 2 wafers presently under test

MIMOSA-20 : CCE for ”14” and ”20” μm Epitaxy

IPHC Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

Réunion Capteurs CMOS, lundi 26 fevrier 2007

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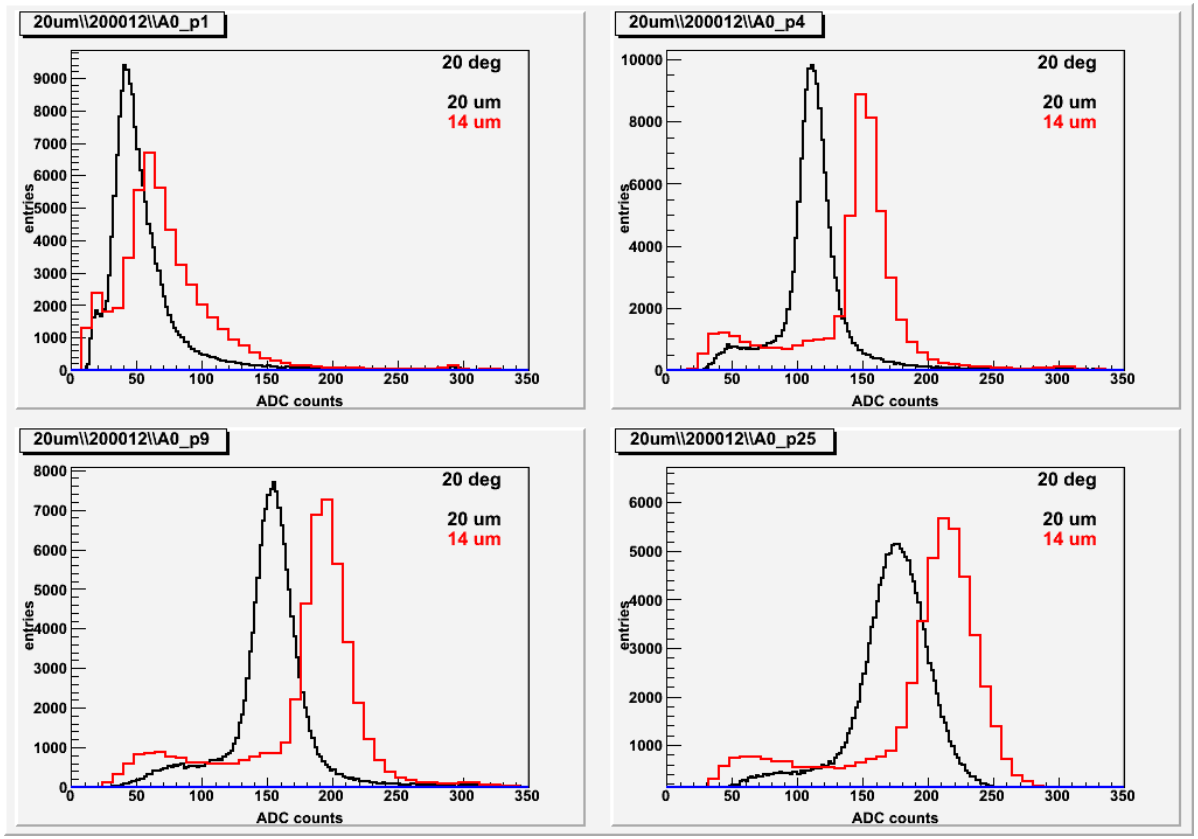
Comparaison pour Mimosa20 entre les deux types de couches épitaxie



IPHC, 23 rue du Loess BP 28, 67037, Strasbourg Cedex 02, France

- MIMOSA-20 (”14” & ”20” μm epitaxy) illuminated with ^{55}Fe source

  $\rightarrowtail$ charge collected in seed pixel, 2x2, 3x3 and 5x5 clusters

  $\rightarrowtail$ **CCE (”14” μm) $\sim$ 30–40 % higher than CCE (”20” μm)**

Radiation Tolerance: AMS-0.35 OPTO Evaluation

Requirements:

- **beamstrahlung (GuineaPig X 3) :** $\lesssim 10^3$ $e^{\pm}_{BS}$**/cm^2/25** μs $\rightarrow$ $\lesssim$**2·10^{12} $e^{\pm}_{BS}$/cm^2/yr**
  $\hookrightarrow$ **O(100) kRad/yr – O(10^{11}) n_{eq}/cm^2/yr** (NIEL $\sim$ 1/30)
- **neutron gas:** $\lesssim 10^{10}$ **n_{eq}/cm^2/yr**

Non-ionising radiation tolerance:

- **MIMOSA-15 irradiated with O(1 MeV) neutrons tested on DESY e^- beams : Very Preliminary results**
  - T = - 20°C, $t_{r.o.} \sim 700\ \mu s$
  - **5.8·10^{12} n_{eq}/cm^2 values derived with standard and with soft cuts**

Fluence	0	0.47	2.1	5.8 (5/2)	5.8 (4/2)
S/N (MPV)	27.8 $\pm$ 0.5	21.8 $\pm$ 0.5	14.7 $\pm$ 0.3	8.7 $\pm$ 2.	7.5 $\pm$ 2.
Det. Eff. (%)	100.	99.9 $\pm$ 0.1	99.3 $\pm$ 0.2	77. $\pm$ 2	84. $\pm$ 2.

Ionising radiation tolerance:

- **Pixels modified against hole accumulations (thick oxide) and leakage current increase (guard ring)**
- **MIMOSA-15 tested with $\sim$ 5 GeV e^- at DESY after 1 MRad (10 keV X-Ray) exposure : Very Preliminary results**
  - T = - 20°C, $t_{r.o.} \sim 180\ \mu s$
  - $t_{r.o.} << 1$ms crucial at T_{room}

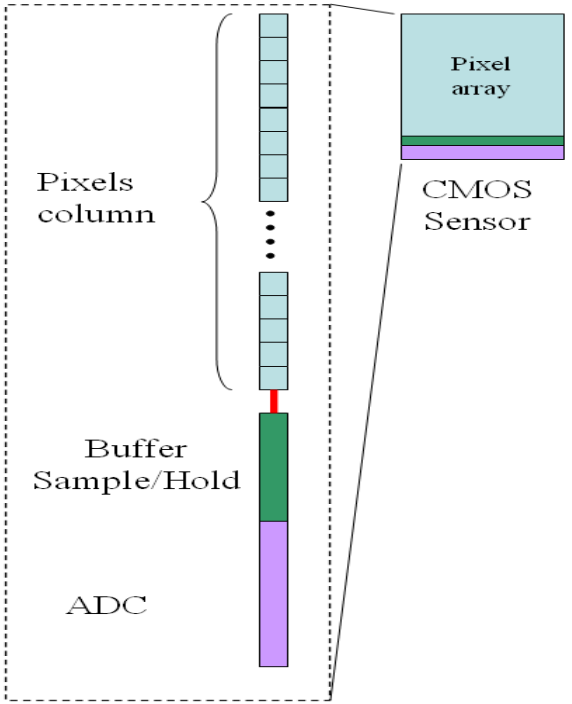
Integ. Dose	Noise	S/N (MPV)	Detection Efficiency
0	9.0 $\pm$ 1.1	27.8 $\pm$ 0.5	100 %
1 MRad	10.7 $\pm$ 0.9	19.5 $\pm$ 0.2	99.96 $\pm$ 0.04 %

Preliminary conclusion:

- **at least 3 years of running viable at T_{room} (or close to)**
- **further assessment needed (also with $\sim$ 10 MeV e^-) : sensors with integ. CDS, ADC, ...**

Fast Read-Out Architecture

- **Parallel development of 3 components (analog, mixed, digital):**
  - **column // arrays with CDS/pixel & discriminated outputs**
  - **4-5 bit ADCs intended to replace discriminators**
  - **$\varnothing$ μcircuits & output memories**



- **2 stage approach :**

  1) Develop sensors for mid-term (2009) applications

  $\hookrightarrow$ less severe requirements, almost suited to 3 outer layers:

  - **EUDET: 1x2 cm^2, t$_{r.o.}$ $\sim$ 100 μs, discri. binary charge encoding (no ADC);**
  - **STAR: 2x2 cm^2, t$_{r.o.}$ $\sim$ 200 μs, discri. binary charge encoding (no ADC);**

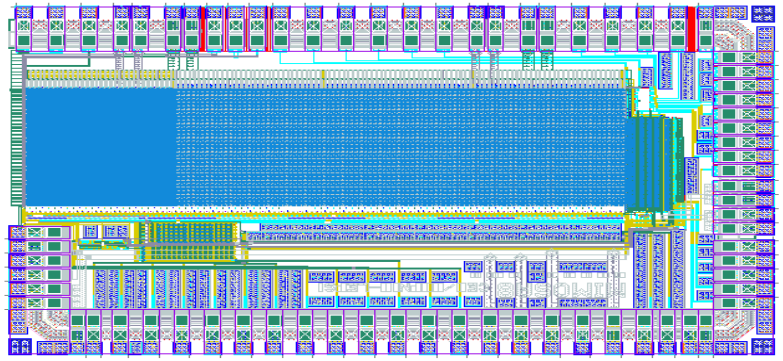
  $\hookrightarrow$ will be operated in real experimental conditions by 2009/2010

  2) Develop ILC sensors (mainly for inner layers) extrapolating from EUDET & STAR:

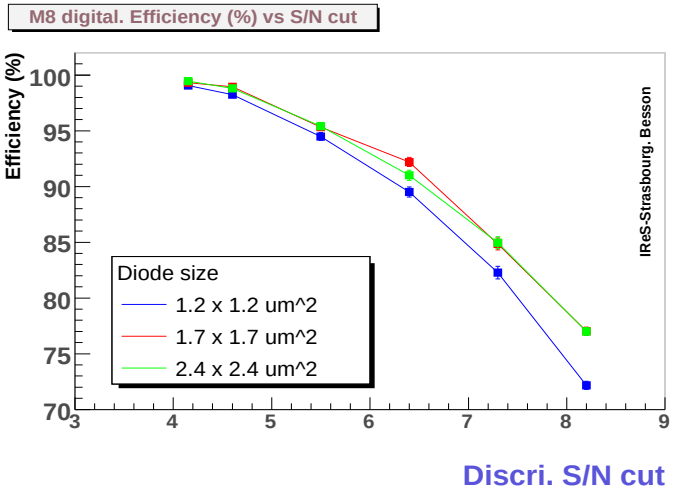
  - **increase row read-out frequency by $\sim$ 50 %**
  - **replace discriminators with ADCs**

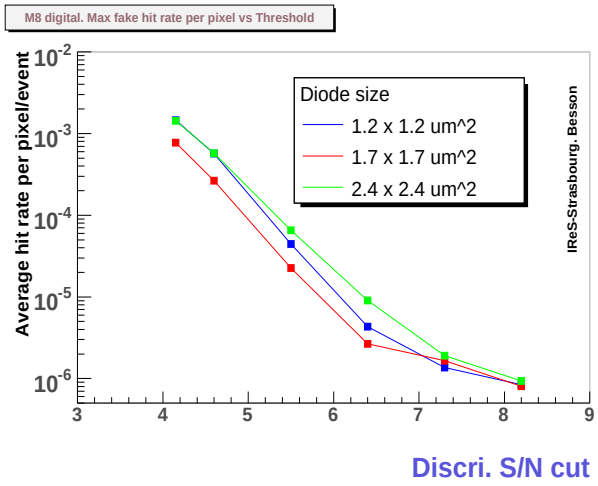
High Read-Out Speed Architecture

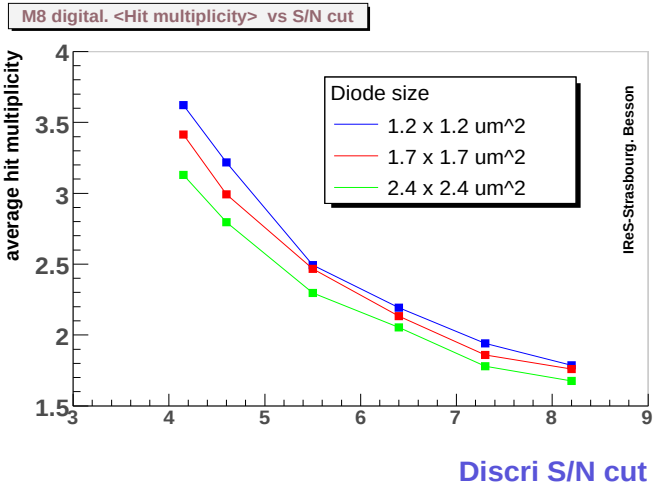
- **MIMOSA-8: TSMC 0.25 μm digital fab. process ($<$ 7 μm epitaxy)**
  - **32 // columns of 128 pixels (pitch: 25 μm)**
  - **read-out time $\sim$ 50 μs (resp. 20 μs) with (resp. without) DAQ**
  - **on-pixel CDS**
  - **discriminator (and DS) integrated at end of each of 24 columns**



- **Detection performance with 5 GeV/c e^- beam (DESY):**







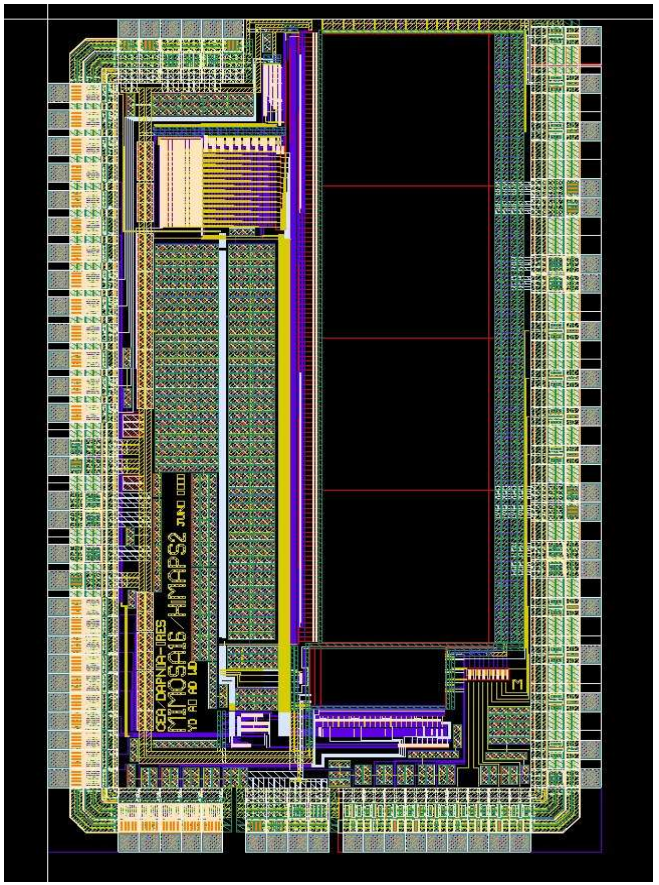
▷▷ **Excellent m.i.p. detection performances despite modest thickness of epitaxial layer**

✳ **det. eff. $\sim$ 99.3 % for fake rate of $\sim$ 0.1 %** ✳ **discri. cluster mult. $\sim$ 3–4** ✳ **$P_{diss} \lesssim$ 500 μW / col.**

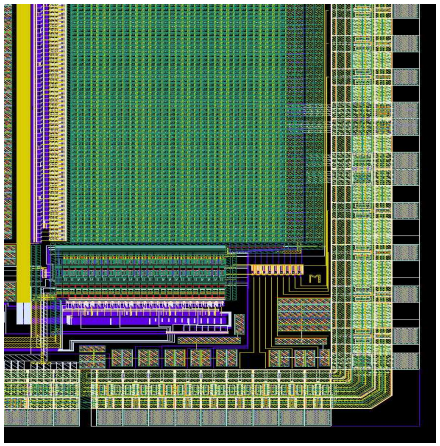
▷▷ **Architecture validated for next steps: techno. with thick epitaxy, rad. tol. pixel at T_{room}, ADC, $\emptyset$, etc.**

Tests of MIMOSA-16

- **MIMOSA-16 design features :**
  - **AMS-0.35 OPTO translation of MIMOSA-8**
    $\hookrightarrow \sim$ **11–15** μm **epitaxy instead of** < 7 μm
  - **32 // columns of 128 pixels (pitch: 25** μm**)**
  - **on-pixel CDS (DS at end of each column)**
  - **24 columns ended with discriminator**
  - **4 sub-arrays :**
    - **S1 : like MIMOSA-8 (1.7x1.7** μm^2 **diode)**
    - **S2 : like MIMOSA-8 (2.4x2.4** μm^2 **diode)**
    - **S3 : S2 with ionising radiation tol. pixels**
    - **S4 : with enhanced in-pixel amplification**
      (against noise of read-out chain)



$\Rightarrow$

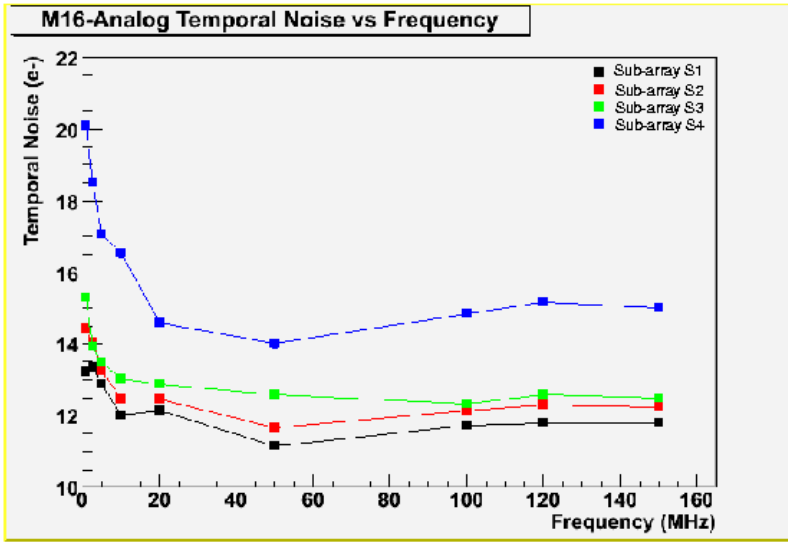


- **Preliminary tests of analog part ("20** μm**" epitaxy) performed in Saclay:**
  - **sensors illuminated with** ^{55}**Fe source and** $F_{r.o.}$ **varied up to** $\gtrsim$ **150 MHz**
  - **measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs** $F_{r.o.}$
- **Tests of analog part ("14** μm**" epitaxy) started in Saclay** $\rightarrowtail$ **first results (CCE)**
- **Next steps :**
  - **digital part** $\geq$ **June at IPHC**
  - **beam tests** $\gtrsim$ **4 Septembre at CERN (T4 – H6)**
- **Later in 2007 : tests of sensors produced in 2nd batch**

MIMOSA-16 Lab Test Results (Analog Part)

Pixel noise and charge collection efficiency for "20 μm option :

Temporal noise vs Frequency
Chip#0 (old mezzanine board)
Columns 28-31



Charge Collection Efficiency vs Frequency
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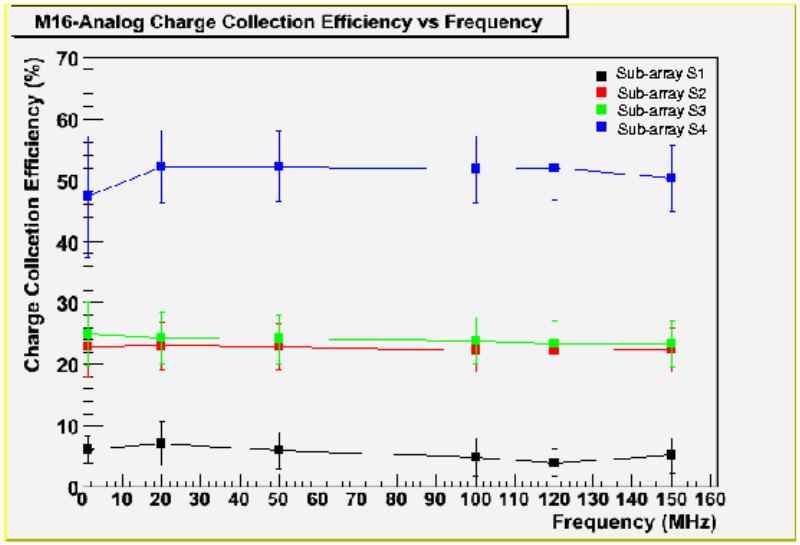


⇛ **Noise performance satisfactory (**like MIMOSA-8 and -15**)**

⇛ **CCE: very poor for S1 (**1.7x1.7 μm^2**) & poor for S2/S3 (**2.4x2.4 μm^2**)**

⟶ **already observed with MIMOSA-15 but more pronounced for "20 μm" option**

↪ suspected origin: diffusion of P-well, reducing the N-well/epitaxy contact, supported by CCE of S4 (4.5x4.5 μm^2 diode)

- **Several different ADC architectures under development at IN2P3 and DAPNIA**
  - **LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5- and 4-bit ADC for a column pair**
  - **LPCC (Clermont) : flash 4+1.5-bit ADC for a column pair**
  - **DAPNIA (Saclay) : Ampli + SAR (4- and) 5-bit ADC**
  - **IPHC (Strasbourg) : SAR 4-bit and Wilkinson 4-bit ADCs**

Lab	proto.	phase	bits	chan.	$F_{r.o.}$ (MHz)	dim. (μm^2)	P_{diss}	eff. bits	Problems
LPSC	ADC1 ADC2 ADC3	tested fab design	5 4 4	8 8 >8	15-25 25 25	43x1500 40x943	1700 μW 800 μW	4	Offset & N
LPCC	ADC1 ADC2	tested fab	5.5 5.5	1 1	5(T)–10(S) 10	230x400 40x1100	20 000 μW 1000 μW	2.5	P_{diss} & bits
DAPNIA	ADC1 ADC2	tested fab	5 5	4 4	4 4	25x1000 25x1000	300 μW 300 μW	$\gtrsim 2$	Missing bits
IPHC	ADC1 ADC2	fab fab	4 4	16 16	10 10	25x1385 25x1540	660 μW 545 μW		

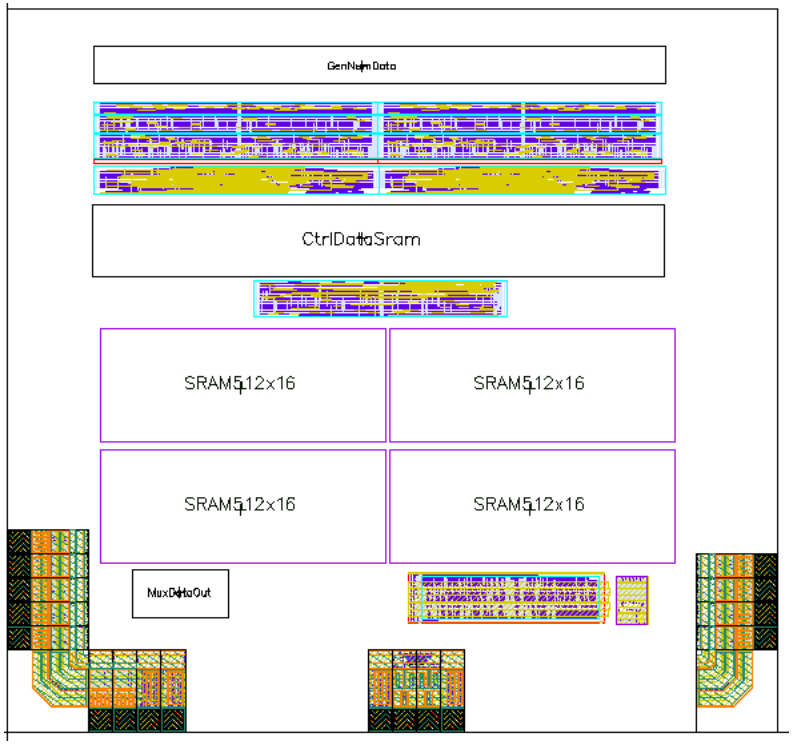
⇛ **1st mature ADC design expected to come out in 2007/08**

⇛ **Submission of 1st col. // pixel array proto equipped with ADCs in Spring 2008 ⟶ with integ. ∅ in 2009**

Zero Suppression Micro-Circuit : Floor Plan

1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :

- 2 step, line by line, logic (adapted to EUDET and STAR):
  - ◇ step-1 (inside blocks of 64 columns) :
    identify up to 6 series of $\leq$ 4 neighbour pixels per line
    delivering signal $>$ discriminator threshold
  - ◇ step-2 : read-out outcome of step-1 in all blocks
    and keep up to 9 series of $\leq$ 4 neighbour pixels
- 4 output memories (512x16 bits) taken from AMS I.P. library
- surface $\sim$ 3.6 x 3.6 mm^2



Status :

- design under way
- submission scheduled for end of June
  ↪ back from foundry end of Septembre
- tests completed by end of year

♣ Extension of MIMOSA-16 ⟼ larger surface, smaller pitch, optimised pixel, JTAG, more testability

Pixel characteristics (still under study) :

- ✳ pitch : 18.4 μm (compromise resolution/pixel layout)
- ✳ diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- ✳ 64 columns ended with discriminator
- ✳ 4–8 columns with analog output for test purposes
- ✳ $\geq$ 6 sub-matrices : $\geq$ 3 pixel designs w/o ionising rad. tol. diode

  $\Rrightarrow$ active digital area : 64 x 384–576 pixels (8.3–12.5 mm^2)

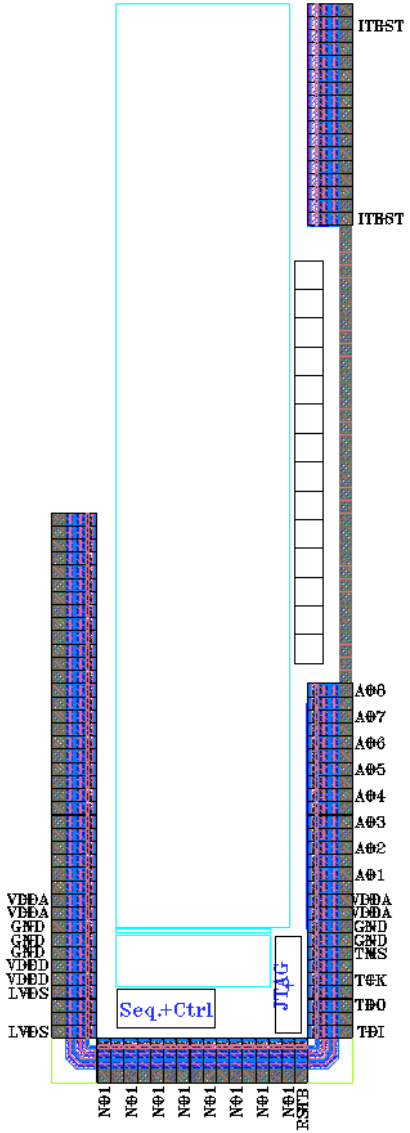
Testability :

- ✳ JTAG + bias DAC ⟼ programmable chip steering
- ✳ 2 additionnal DC voltages to emulate pixel's output for independent discriminator performance assessment
- ✳ output frequency $\leq$ 40 MHz

Status :

- ✳ Design under way at IPHC (also at DAPNIA)

  ↪ submission end of Septembre '07

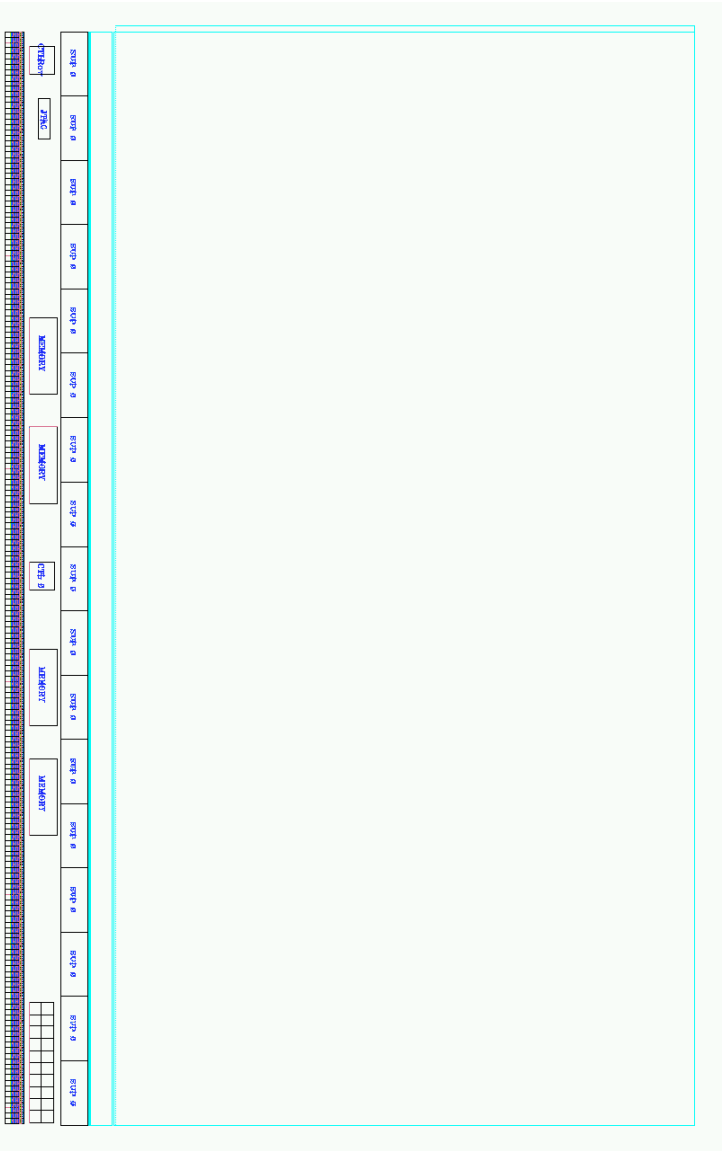


Spring 2008 : MIMOSA-22+

- **MIMOSA-22 complemented with ∅ (SUZE-01)**
- 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
- larger surface : active area ∼ 0.5 cm^2
  - **final column depth (544/576 pixels)**
  - ≳ 1/4 of final number of columns (≥ 256 / 1088)
- ▶ opportunity for engineering run combining various chips

End 2008 / early 2009 : Final chip for EUDET

- Extension of MIMOSA-22+
- Active area : 1088 columns of 544/576 pixels (2 x 1 cm^2)
- **Read-out time ∼ 100** μs
- Chip dimensions : 20 x 12 mm^2 ⟶ engineering run



Next steps for ILC:

- **incorporate ADC** (with integrated discrimination) ⟶ outer layers
- **increase r.o. frequency** by ∼ 50 % (new ∅ & memory design) ⟶ inner layers

SUMMARY

- CMOS sensors are developed for running conditions with beam background $>>$ MC simulations
- Fast read-out sensors progressing steadily :
  - ⁂ col. // architecture with discriminated output operational
  - ⁂ ADCs close to final design ($\lesssim$ beginning 2008)
  - ⁂ $\varnothing$ μcircuits : 1st generation (EUDET, STAR) close to fabrication
- AMS-035 OPTO fabrication technology assessed $\rightarrowtail$ baseline for R&D :
  - ⁂ detection efficiency (T), radiation tolerance, noise $\rightarrowtail$ fake hits, etc.
    - $\hookrightarrow$ equip EUDET, STAR, CBM demonstrators in 2007/2008 with new generation of full scale sensors
      - $\hookrightarrow$ real experimental conditions
- Milestones until final chip well identified :
  - ⁂ 1st step : final sensors with discriminated binary charge encoding for EUDET (2009) and STAR (2010)
  - ⁂ 2nd step : replace discri. with ADC (outer layers) and increase r.o. frequency by $\sim$ 50 % (inner layers)
  - ⁂ also: find final fabrication process ($<$ 0.2 μm feature size)
- Concern :
  - ⁂ system integration issues not covered $\rightarrowtail$ prototype ladder ????

BACK-UP SLIDES

Main R&D Directions

- **High r.-o. speed, low noise, low power dissip., highly integrated signal processing architecture:**
  - ⁂ analog part (charge collection, pre-amp, CDS, ...) inside pixel
  - ⁂ mixed (ADC) and digital (sparsification) micro-circuits integrated inside pixel or aside of active surface

- **Optimal fabrication process:**
  - ⁂ epitaxial layer thickness
  - ⁂ number of metal layers
  - ⁂ yield
  - ⁂ (dark current)
  - ⁂ cost
  - ⁂ life time of ($<$ 0.2 μm) process

- **Radiation Tolerance:**
  - ⁂ dark current
  - ⁂ doping profile
  - (⁂ latch-up)

- **Industrial thinning procedure:**
  - ⁂ minimal thickness
  - ⁂ mechanical prop.
  - ⁂ individual chips rather than wafers (?)
  - ⁂ yield

- **Room temperature operation:**
  - ⁂ minimise cooling requirements
  - ⁂ performances after irradiation

Main Requirements

for the ILC Vertex Detector :

physics & running condition requirements

Constraints from Required $\sigma_{i.p.}$ (1/2)

- $\sigma_{\mathbf{IP}} = \mathbf{a} \oplus \mathbf{b}/\mathbf{p} \cdot \mathbf{sin}^{\mathbf{3/2}}\theta$ with $\mathbf{a} <$ 5 μm and $\mathbf{b} <$ 10 μm

  ▷ limits on $\mathbf{a}$ and $\mathbf{b}$ are still "very educated guesses"

  ▷ SLD: $\mathbf{a}$ = 8 μm and $\mathbf{b}$ = 33 μm

- Upper bound on $\mathbf{a}$ drives the pixel pitch and the radii of the inner and outer layer of the Vx Det.

- Upper bound on $\mathbf{b}$ drives radius and material budget of inner layer (& beam pipe)

- Constraint on σ_{IP} satisfies simultaneoulsy requirement on double hit separation in inner most layer ($\sim$ 30 – 40 μm)

Constraints from Required $\sigma_{i.p.}$ (2/2)

Constraint on a : $z_{IP} \approx \frac{z_0 \cdot R_4 - z_4 \cdot R_0}{R_4 - R_0} \rightarrowtail a = \sigma_{IP} \approx \frac{(R_4^2 \cdot \Delta z_0^2 + R_0^2 \cdot \Delta z_4^2)^{1/2}}{R_4 - R_0}$

- Numerical examples based on $R_4 = 4 \cdot R_0$ (ex: R_4/R_0 = 60 / 15 mm or 64 / 16 mm)
  - ▷ $\Delta z_4 = \Delta z_0 = \sigma_{sp} = 3\,\mu m \Rightarrow a \approx 1.37 \cdot 3\,\mu m \approx 4.1\,\mu m$
  - ▷ $\Delta z_4 = 5\,\mu m$ and $\Delta z_0 = 2.5\,\mu m \Rightarrow a \approx 1.5 \cdot 2.5\,\mu m \approx 3.8\,\mu m$

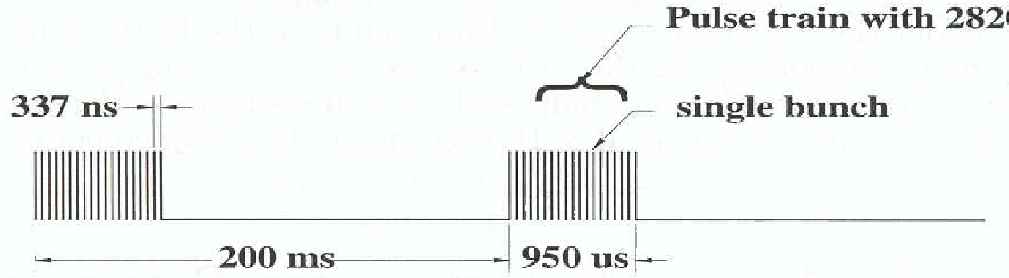
⇛ Twice larger pitch in outer layer than in inner most layer satisfies constraint $a < 5\,\mu m$

Constraint on b : $b \approx 0.0136 \cdot (1 + 0.038 \cdot \ln t/\sin\theta) \cdot R_0 \cdot \sqrt{t}$ where $t = \frac{e_{pipe}}{X_0^{Be}} + t_{L0}$

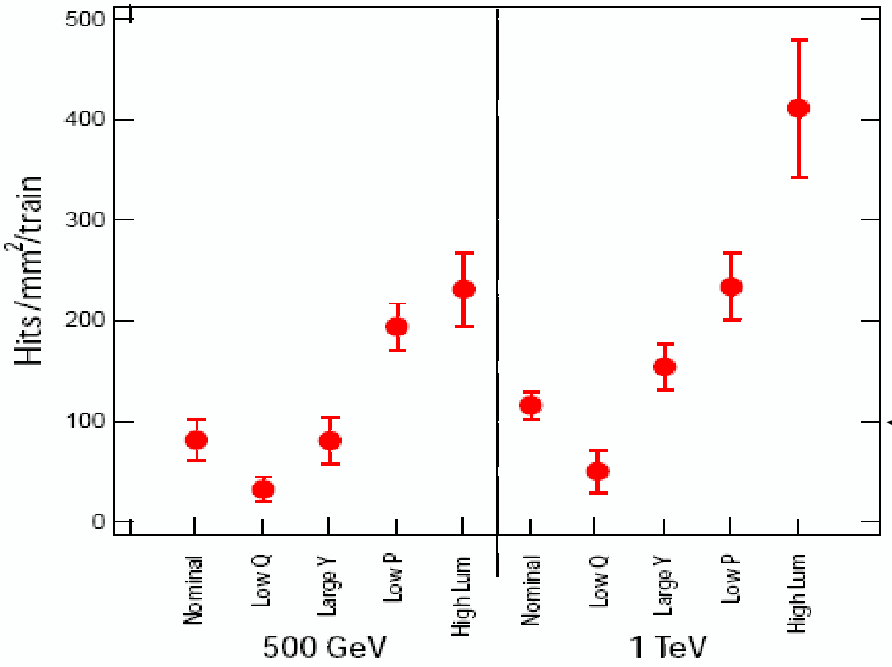
- ▷ $b < 10\,\mu m \Rightarrow t \lesssim 0.4\,\%$
- ▷ $e_{pipe} \approx 400 - 500\,\mu m \rightarrowtail \frac{e_{pipe}}{X_0^{Be}} \sim 0.11 - 0.14\,\% \rightarrowtail t_{L0} \lesssim 0.25\,\%$

- Ladders equipped with CMOS sensors & developed for STAR HFT reach already $\sim$ 0.3 % X_0

Time Structure for the ILC



Backgrounds



~0.035/mm²/bunch

M. Breidenbach

Constraints from Beamstrahlung

- **1st layer (L0) : $\gtrsim$ 5 hits/cm^2/BX for 4T / 500 GeV / R_0 = 1.5 cm / no safety factor**
  $\rightarrowtail \lesssim$ 1.8·10^{12} e$^{\pm}$/cm^2/yr (safety factor of 3)
  - **2nd layer: 8 times less (direct)**
  - **3rd layer: 25 times less (direct)**

- **Consequences on Occupancy in 1st layer (L0): $\lesssim$ 0.9 % hit occupancy in 50 μs (r.o. time of TESLA TDR)**
  $\hookrightarrow$ signal spread on $\lesssim$ 4.5–9 % pixels (cluster multiplicity $\sim$ 5-10)

  $\Rrightarrow$ 1) aim for shorter read-out time in L0 than in TDR $\rightarrowtail$ typically $\lesssim$ 25 μs
  (compromise with power dissipation, multiple scattering, ...)

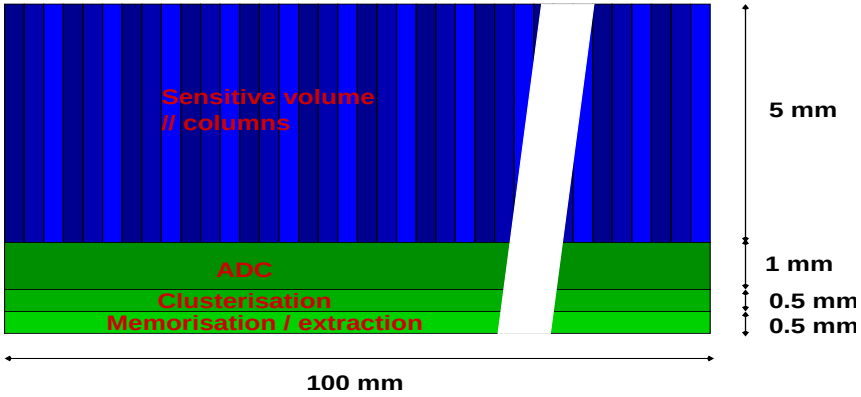
  2) aim for shorter read-out time in L1 than in TDR $\rightarrowtail$ typically $\sim$ 50 μs (vs 250 μs)
  and presumably smaller radius (e.g. $\sim$ 20 – 22 mm)
  (use tracks extrapolated from L1-4 down to L0)

  3) aim for relaxed read-out time in L2, L3, L4: $\sim$ 100 – 200 μs (vs 250 μs)
  $\hookrightarrow$ depends on backscattered e$^{\pm}$ rate

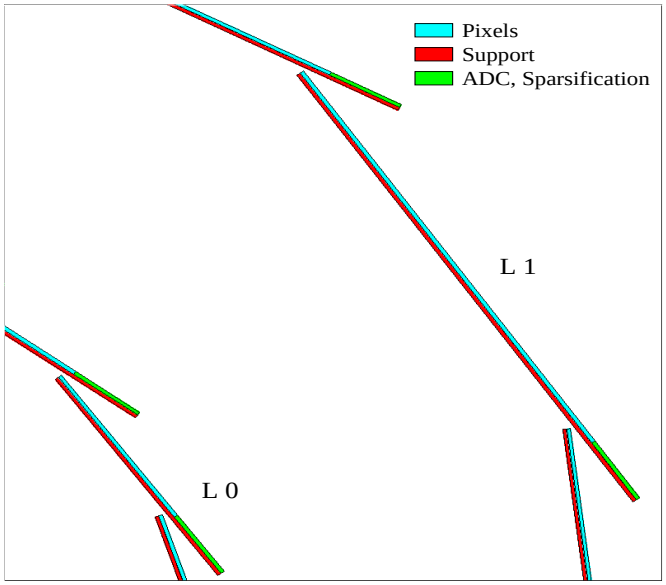
- **Consequences on Radiation Tolerance in L0 :**
  - ※ **dose integrated over 3 years: $\lesssim$ 5.4·10^{12} e/cm^2 $\longrightarrow \lesssim$ 2·10^{11} n$_{eq}$/cm^2 (NIEL $\sim$ 1/30)**
    - ◇ **neutron dose integrated over 3 years much smaller : $\lesssim$ 3·10^{10} n$_{eq}$/cm^2 (safety factor of 10)**

Consequences on Inner Layer Design

- $\lesssim$ 25 μs in L0:
  - columns of 256 pixels (20 μm pitch) $\perp$ beam axes
    - read out in // at $\sim$ 10 MHz $\longrightarrow$ 5 mm depth
- $\sim$ 50 μs in L1:
  - columns of 512 pixels (25 μm pitch) $\perp$ beam axes
    - read out in // at $\sim$ 10 MHz $\longrightarrow$ 13 mm depth

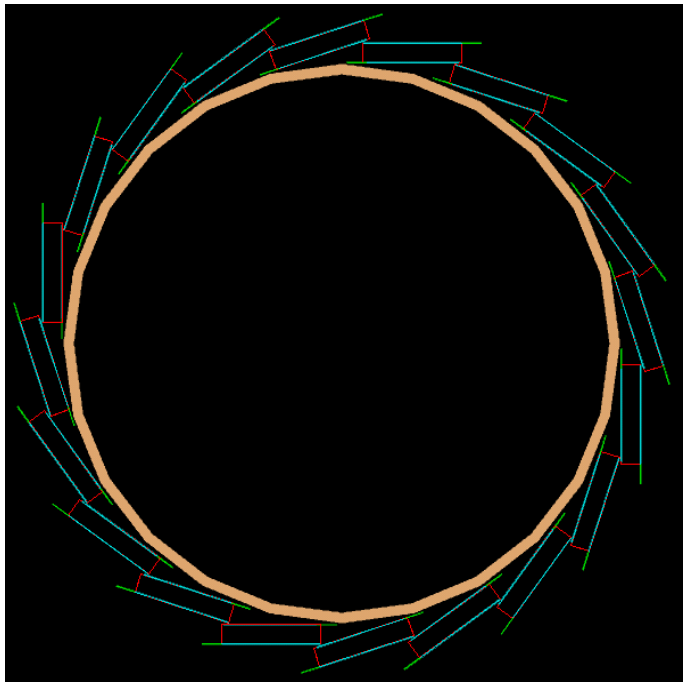
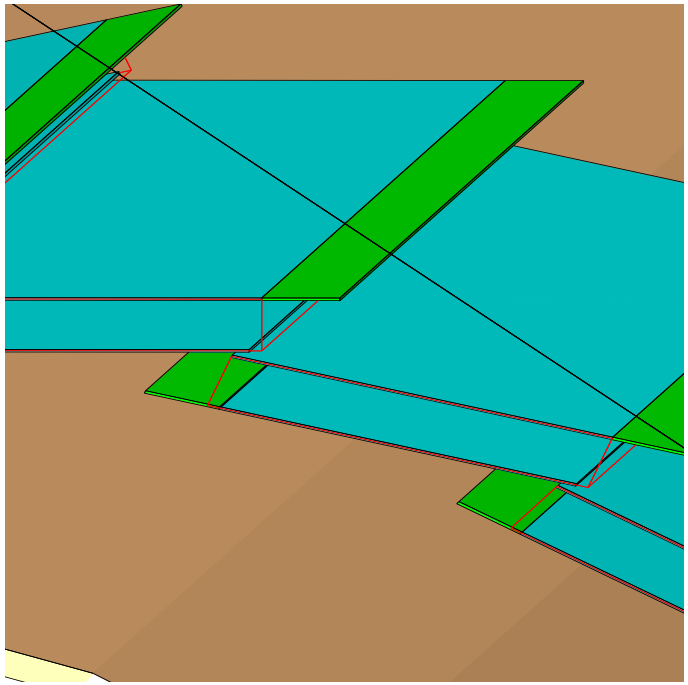
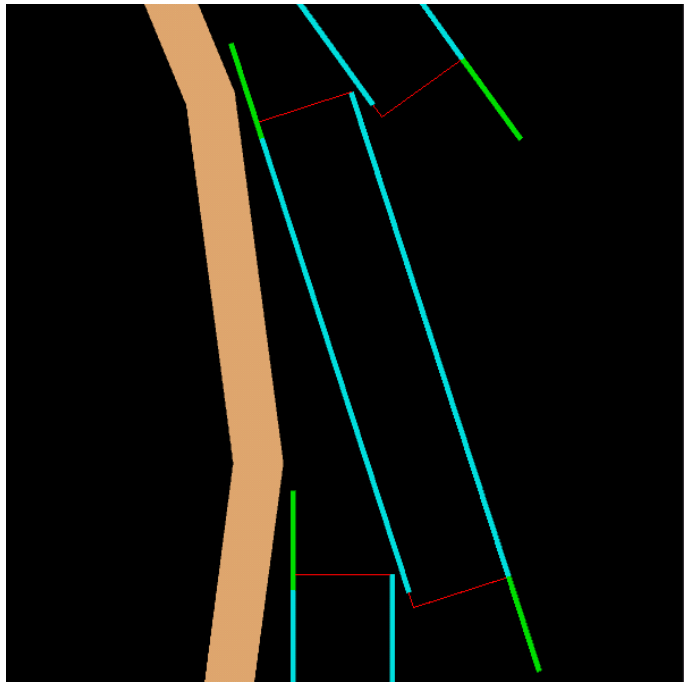


- $\lesssim$ 2 mm wide side band hosting ADC, sparsification, ...
  - $\hookrightarrow$ effect on material budget SMALL :
    - b increases by $\sim$ 5 – 10 %
- Option with discriminator instead of ADC :
  - $\sim$ 1 mm wide side band $\Rightarrow$ effect on $\mathrm{b} < 5$ %



Adapting the Inner Most Layer to High Background

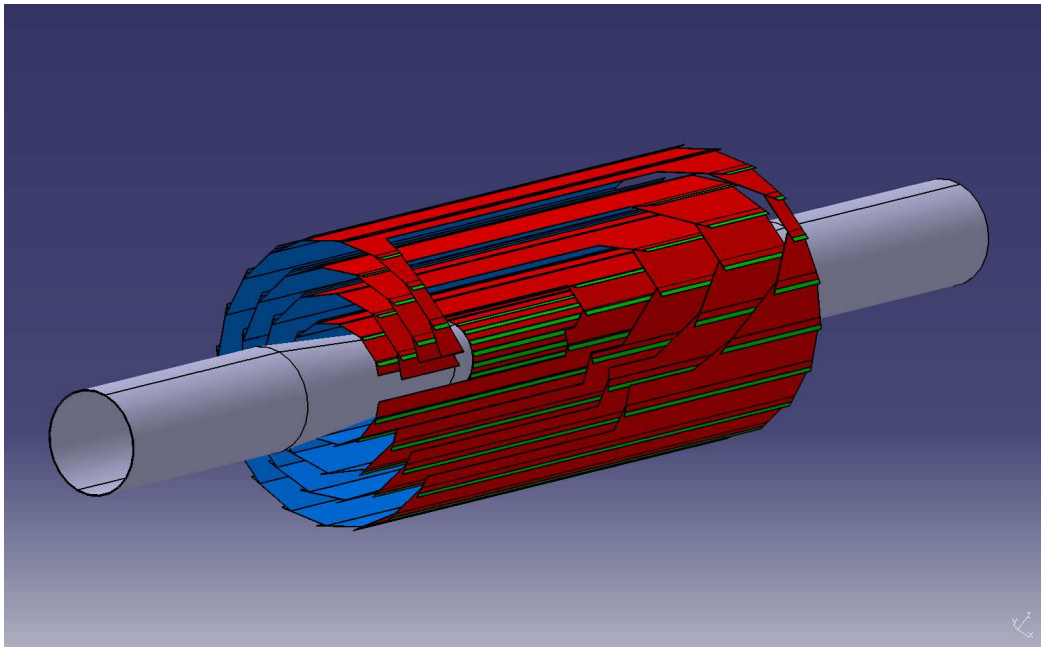
- Design inner most layer (L0) to minimise its sensitivity to (unexpected) high occupancy ($\gtrsim$ 10 %)
- Double sided layer $\longrightarrow \sim$ 1 mm long mini-vectors connecting impacts on both sides of layer
  - ▷ Needs a detailed feasibility (engineering) study ....

Basic Vertex Detector Design features

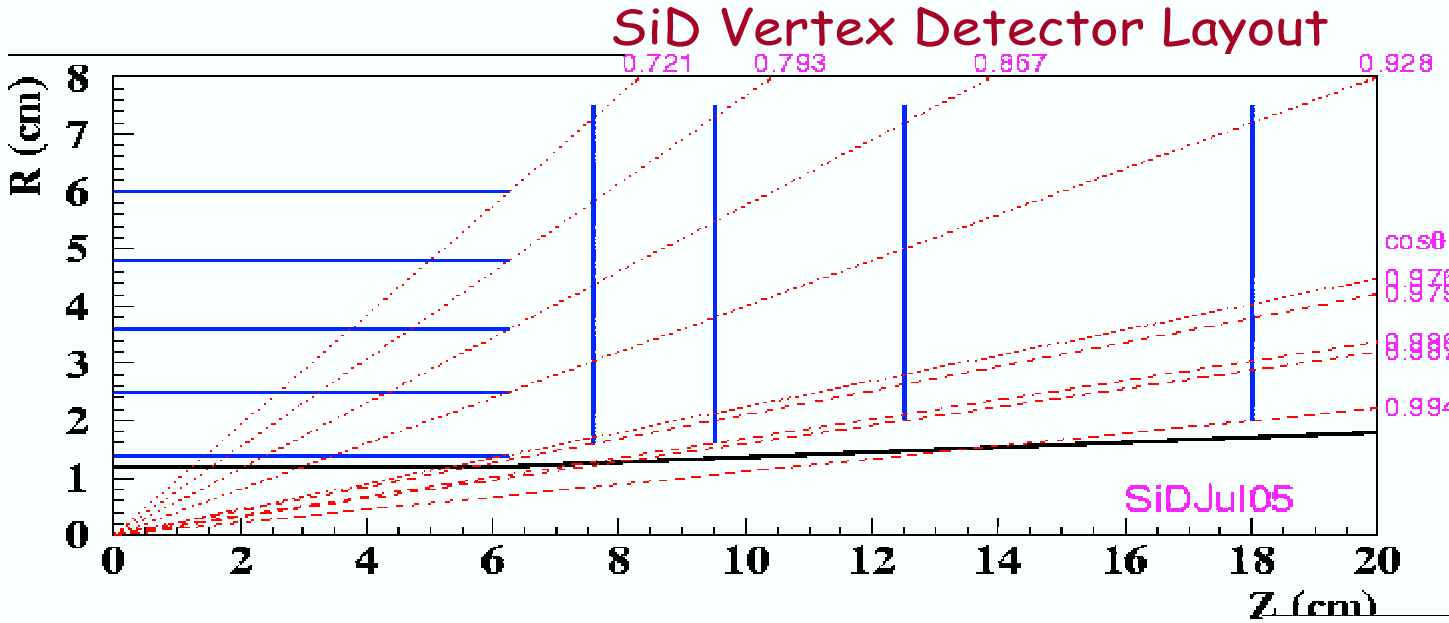
- Geometry : 5 cylindrical layers (R = 15 – 60 mm), $\|cos\theta\| \leq$ 0.90 – 0.96 (possibly 6 layers)
- L0 and L1 : fast col. // architecture
- L2, L3 and L4 : possibly multi-memory pixel architecture (?)
- Pixel pitch varied from 20 μm (L0) to 40 μm (L4) by 5 μm steps $\rightarrow$ minimise P_{diss}

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	15	20	25	20	25	$<$100	$<$5
L1	$\leq$ 25	25	50	$\leq$26	$\leq$ 65	$<$130	$<$7
L2	37	30	$<$200	24	75	$<$100	$<$5
L3	48	35	$<$200	32	70	$<$110	$<$6
L4	60	40	$<$200	40	70	$<$125	$<$6
Total				142	**305**	$<$565	$<$3–30



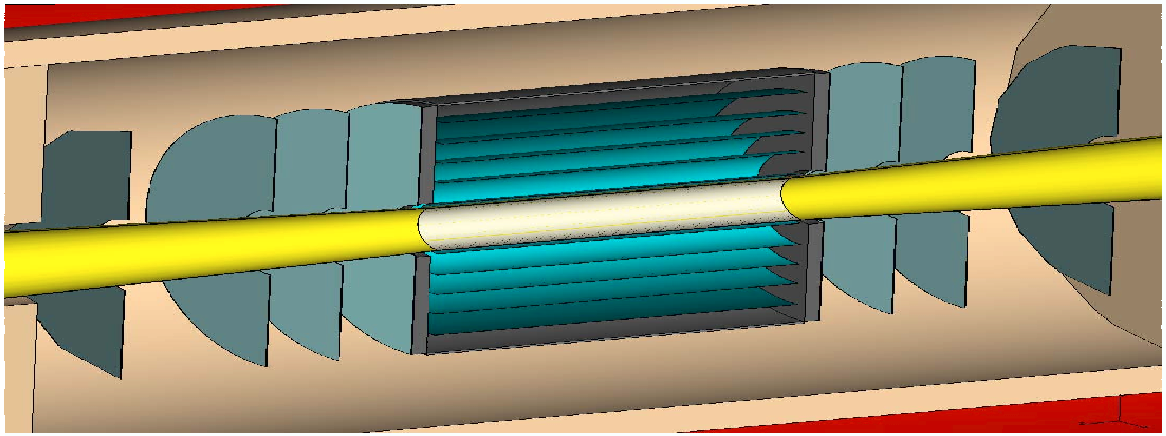
- Ultra thin layers: $\lesssim$ 0.2 % X_0/layer (extrapolated from STAR-HFT; 35 μm thick sensors)
- Very low P_{diss}^{mean}: $<<$ 100 W (exact value depends on duty cycle)
- Fake hit rate $\lesssim 10^{-5} \rightarrow$ whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)

Alternative Approach : SiD Vertex Detector Geometry



5 barrel layers
4 end disks

5 Tesla



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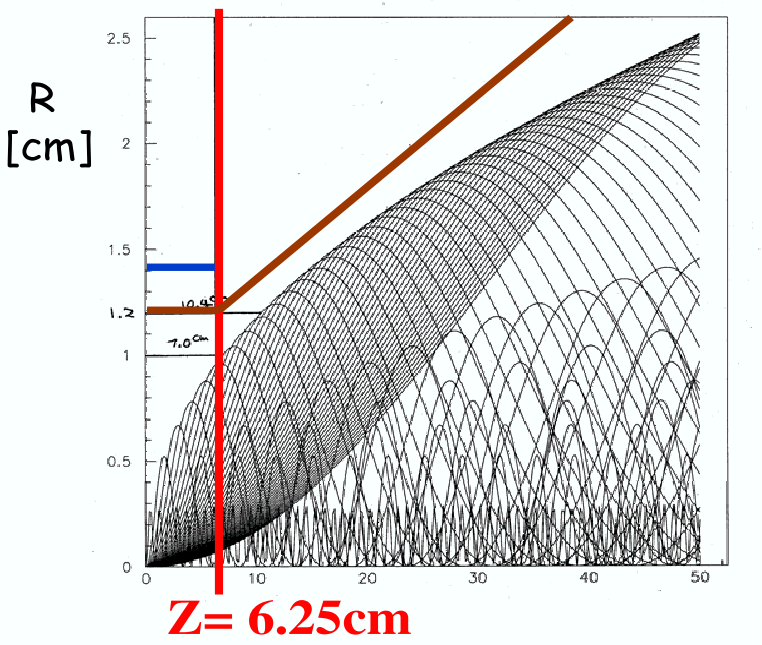


Summary of Sensor Perfo. Obtained vs Requirements

- **Impact parameter resolution :**
  - **a** $< 5\ \mu m$ ✓
  - **b** $< 10\ \mu m$ ✓ $\longrightarrow$ **thinning** ✓ **, ladder design** ✓ **(from STAR), stitching not yet investigated**
- **Radiation tolerance at room temperature :**
  - **neutrons** ✓
  - **X-Rays** ✓
  - **10 MeV electrons** ✓ $\longrightarrow$ **only assessed at T** $\lesssim 0^{\circ}$**C**
- **Fast, low power, integrated signal processing :**
  - **read-out speed** ✓
  - **integrated ADC** $\longrightarrow$ **under developement**
  - **integrated sparsification** $\longrightarrow$ **studies starting**
  - **power dissipation** ✓ **(duty cycle** $<$ **1/20)** $\longrightarrow$ **pulsed powering not fully assessed for this duty cycle**

- Overall geometry :
  - matching with neighbour trackers
- Sensor geometry and features
- Heat removal
- Thermal distortions
- Handling thin silicon
- Assembly and alignment procedures
- Connections, cabling, and optical fibers
- Paths for cables, optical fibers, and air flow
- Lorentz forces

⇒ **Only few people taking care of so many crucial and delicate topics**

Observed Radiation Tolerance

of MIMOSA Sensors

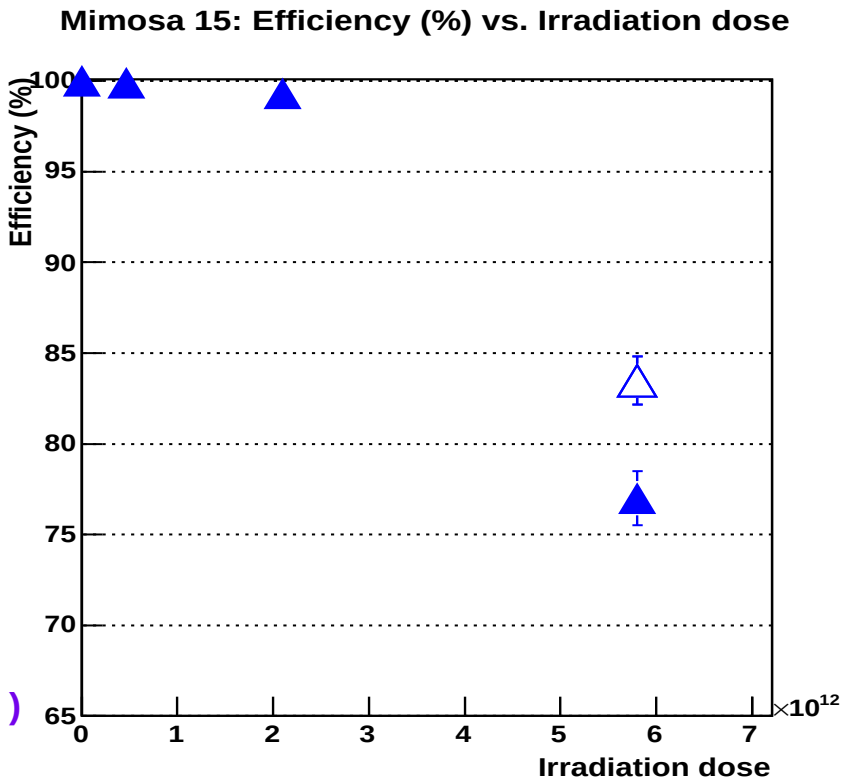
Radiation Tolerance: Non-Ionising Radiation

- **MIMOSA-15 irradiated with neutrons of O(1 MeV) at JINR (Dubna) $\mapsto$ doses of 0.47 / 2.1 / 5.8 $\cdot 10^{12} n_{eq}/cm^2$**
- **Performance assessment of sensors (20 μm pitch) installed on $\sim$ 5 GeV e^- beam at DESY (July 2006)**
  - **running conditions: T = - 20°C, $t_{r.o.} \sim 700\ \mu s$ (2.5 MHz)**

    $\hookrightarrow$ **Very Preliminary results ...**

Fluence	0	0.47	2.1	5.8 (5/2)	5.8 (4/2)
	(10^{12} n_{eq}/cm^2)				
Noise (e^-)	9.0 $\pm$ 1.1	9.2 $\pm$ 1.2	9.3 $\pm$ 1.2	9.6 $\pm$ 2.0	9.6 $\pm$ 1.9
S/N (MPV)	27.8 $\pm$ 0.5	21.8 $\pm$ 0.5	14.7 $\pm$ 0.3	*8.7* $\pm$ 2.	*7.5* $\pm$ 2.
Det. Eff. (%)	100.	99.9 $\pm$ 0.1	99.3 $\pm$ 0.2	77. $\pm$ 2.	84. $\pm$ 2.

- 5.8·10^{12} n_{eq}/cm^2 values derived with **standard** and with **soft** cuts



$\Rightarrow$ **Fluences $\gg 10^{12} n_{eq}/cm^2$ affordable with simple pixels (no CDS $\mapsto$ low N)**

provided T < 0°C and $t_{r.o.} \ll 1$ ms

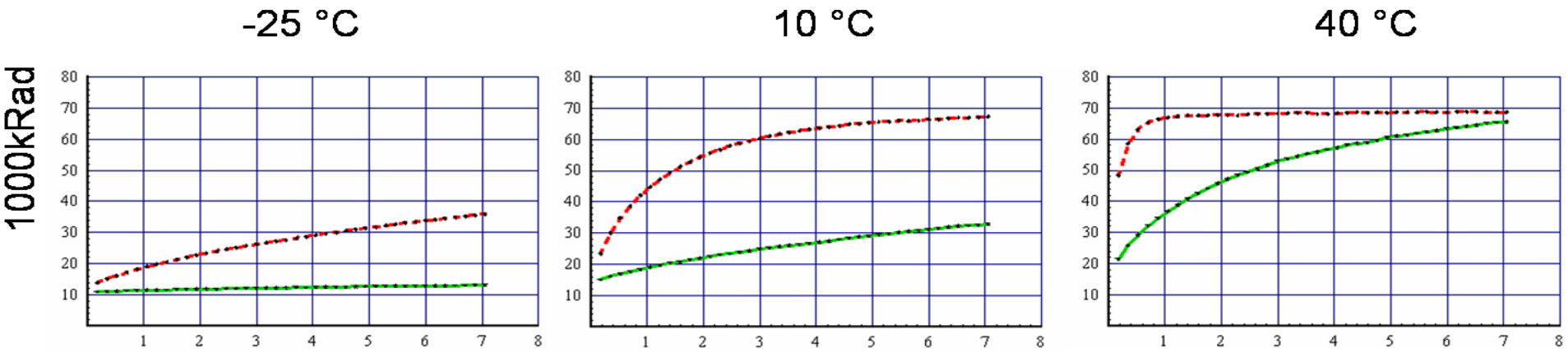
$\triangleright\triangleright\triangleright$ **Fluences $>>$ 1·10^{12} n_{eq}/cm^2 can presumably be accommodated with pixels including CDS by optimising pixel pitch, charge collection syst., fabrication techno., etc.**

Radiation Tolerance : Ionising Radiation

- Pixel design needs to be modified to withstand high radiation doses (esp. at T_{room}):
  - removal of thick oxide nearby the N-well (against charge accumulation)
  - implantation of P+ guard-ring in polysilicon around N-well (against leakage current)

- Characterisation of MIMOSA-11 in laboratory : Noise (e^- ENC) vs Integration time (ms)

  for Ordinary and Radiation Tolerant pixels, measured at T = - 25°C, + 10 °C and + 40°C



- Characterisation of MIMOSA-15 with $\sim$ 5 GeV e^- at DESY after 1 MRad (10 keV X-Ray) exposure :
  - Radiation Tol. pixels, measured at T = - 20°C with $t_{r.o.} \sim 180\ \mu s$ (10 MHz) $\Rightarrow$ Very preliminary results :

※ 1 MRad tolerance demonstrated at T $<$ 0°C

(read-out time $\ll$ 1 ms, no CDS)

Integ. Dose	Noise	S/N (MPV)	Det. Efficiency
0	9.0±1.1	27.8±0.5	100 %
1 MRad	10.7±0.9	19.5±0.2	99.96±0.04 %

※ *need to cross-check detection performance at T_{room} with pixels including CDS*

Radiation Tolerance : Low Energy Electrons

Investigation of sensitivity to $\sim$ 10 MeV electrons (NIEL factor $\sim$ 1/30)

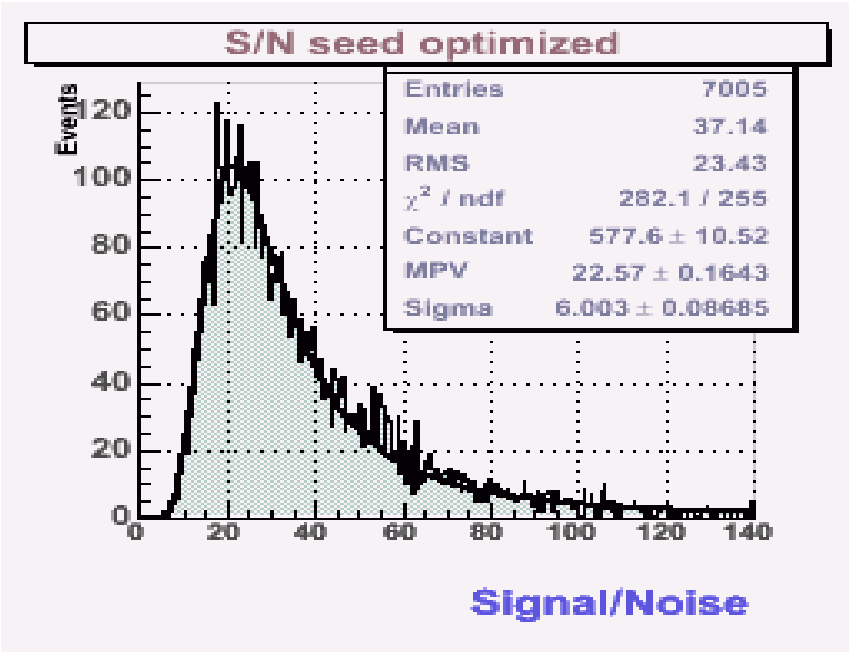
$\hookrightarrow$ **similar to beamstrahlung $e^{\pm}$ in 4 T field at 15 mm radius**

1) **MIMOSA-9 exposed to $10^{13} e^{-}_{9.4MeV}$/cm^2 in Darmstadt : equivalent to $\lesssim$ 300 kRad/cm^2 and $\sim 3 \cdot 10^{11} n_{eq}$/cm^2**

2) **Irradiated chip tested with $\sim$ 6 GeV e^- at DESY**

$\hookrightarrow$ **Test result at -20°C : S/N $\sim$ 23 $\rightarrowtail \epsilon_{det} > 99.3\%$**

(before irradiation: S/N $\sim$ 28 and ϵ_{det} = 99.93 $\pm$ 0.03 %)



▷ **Sensors still need to be tested at room temperature (compatible with very light cooling system)**

Developments simultaneously oriented towards well focussed applications and towards generic objectives useful to several applications

Application	version	2006	2007	2008	2009	2010	2011
STAR	HFT-1	final proto	Prod.				
	HFT-2	R&D	R&D	proto final	Prod.		
EUDET	BT-1	2 Prod.					
	BT-2	R&D	final proto ?	Prod.			
Imaging		R&D	final proto	Prod. ?			
Generic topics							
Fast sensors :	○ architecture	R&D	R&D	R&D +	R&D ++	ILC proto	CBM proto
	○ ADC	R&D	final proto	↗			
	○ digital	pre-study	R&D	final proto	↗		
Radiation tolerance		R&D	R&D	R&D	R&D	↗	
Fabrication technologies		R&D	R&D	R&D	R&D	↗ ???	
Thinning		R&D	D	D	OK ???		