DESY PRC R&D 03/01 Update 2(07)
Project: DEPFET for ILC
Type of Document: Status Report
Date: 17.4.2007
Verision: 2.0

DEPFET Pixel Vertex Detector for the ILC

L. Feld[1], R. Jussen, W. Karpinski, K. Klein
(1. Physikalisches Institut, RWTH Aachen, Germany)

P. Hettkamp, R. Kohrs, M. Karagounis, M. Koch, H. Krüger, P. Lodomez, M. Mathes, L. Reuen, C. Sandow, J. Schneider, E. von Törne, M. Trimpl, J. Velthuis, N. Wermes[2]
(Bonn University, Germany)

W. de Boer[3], J. Bol, A. Sabellek
(Universität Karlsruhe, Germany)

P. Fischer[4], F. Giesen, C. Kreidl, I. Peric
(Mannheim University, Germany)

L. Andricek, X. Chen, A. Frey, K. Heinzinger, P. Lechner, G. Lutz, H. G. Moser[5], R. H. Richter, M. Schnecke, A. Raspereza, S. Rummel, L. Strüder, J. Treis
(MPI für Physik, Munich, Germany)

Z. Dolezal, Z. Drasal, P. Kodys[6], D. Scheirich
(Charles University, Prague, Czech Republic)

I. Carbonell, J. Fuster, C. Lacasta[7], M. Vos
(Instituto de Fisica Corpuscular (IFIC), CSIC-UVEG, Valencia, Spain)

[1]Lutz.Feld@physik.rwth-aachen.de
[2]wermes@physik.uni-bonn.de
[3]deboer@ekp.uni-karlsruhe.de
[4]peter.fischer@ti.uni-mannheim.de
[5]hgm@hll.mpg.de
[6]kodys@ipnp.troja.mff.cuni.cz
[7]Carlos.Lacasta@ific.uv.es

Abstract

DEPFET pixels offer a unique possibility for a high resolution pixel vertex detector as the innermost component of the tracking system in an ILC detector. The key idea of DEPFET sensors is the integration of amplifying transistors into a fully depleted bulk in such a way that all signal charges are collected in the 'internal gates' of the transistors. The excellent noise performance obtained through the low input capacitance in combination with the full signal from the depleted bulk leads to a large S/N ratio. The sensor itself can therefore be made very thin (50 μm) without loss of efficiency. Readout is performed by cyclic enabling of transistor rows in a large matrix. The total system, including readout and sequencing chips, is expected to dissipate less than 10 W for a five layer geometry assuming a 1:200 power duty cycle.
In this status report the progress of the DEPFET development towards an ILC vertex detector with respect to the last PRC review in May 2005 is presented. Since then properties of prototype matrices and dedicated ASIC electronics have been characterized in various laboratory and test beam measurements. In particular a point resolution of less than 2 μm has been demonstrated (using 450 μm thick sensors). Based on these results larger matrices, improved readout and control electronics have been designed which are presently in production. These second generation systems will show larger gain, reduced system noise and almost ILC size. Further technological development includes the thinning technology, now routinely done on 6" wafers and preparation for bump bonding. In parallel software was developed to simulate the performance of a DEPFET based vertex detector in an ILC detector.

1 Introduction

This status report summarizes the progress achieved towards a DEPFET pixel vertex detector suited for application at the ILC. The initial R&D, described in the PRC report from May 2003, was oriented towards TESLA [1]. The anticipated environment at ILC [2] is very similar and the assumed boundary conditions remain valid. The general requirements for a vertex detector in the high multiplicity environment of the ILC and how they are addressed by a DEPFET system are summarized as follows:

- ▷ Aim at a spatial point resolution per layer of $\lesssim 4\,\mu$m. This can be achieved by pixels of $25 \times 25\,\mu\text{m}^2$ size guaranteeing a binary resolution of $25\,\mu\text{m}/\sqrt{12} \approx 7\,\mu$m. Analog interpolation assuming an anticipated signal to noise ratio of $\gtrsim 40$ will significantly improve this value to $\lesssim 3.5\mu$m ($R - \phi$) and $\lesssim 4\mu$m (z). Using a GEANT4 simulation it can be demonstrated that the required impact parameter resolution of [19]

$$\sigma(IP_{r-\phi}) = 5\mu m \oplus \frac{10\mu m}{p \cdot \sin^{3/2}\theta},$$

  can be met with such a pixel layout. With 450 μm thick detectors a resolution below 2 μm has already been achieved in test beams.

- ▷ The innermost layer is at a radius of ≈ 15 mm. The active area in this innermost layer must therefore have a length (along the beam) of ≈ 10 cm. This requires 4096×512 pixels of $25\,\mu\text{m} \times 25\,\mu$m.

- ▷ The innermost layer should tolerate an accumulated radiation dose after 5 years of operation of 200 krad. Irradiation tests of DEPFET devices suggest that the sensors are radiation tolerant well above this limit.

- ▷ Minimum radiation length should restrict multiple scattering. The design goal is to reach in the order of 0.1% of a radiation length per module. A thinning technology compatible with DEPFET production has been developed. It can be used to build an all silicon sensor module with a thickness in the active part of $50\,\mu$m. Due to the low noise characteristics of the DEPFET a signal to noise ratio > 40 is still achievable with such a module.

- ▷ Operation at a bunch train repetition rate of 5 Hz with each train delivering 2820 bunches during ≈ 1 ms. Assuming that the low duty cycle of 1:200 given by ILC can be exploited the average power dissipation of the system will be well below 10 W.

- ▷ A hit multiplicity of ≈ 0.03 hits per mm^2 and bunch at $\sqrt{s} = 500$ GeV must be tolerated. In a recent study [3] this value approaches 0.04 hits per mm^2 and bunch for the nominal ILC layout with 14 mrad crossing

angle. In other layouts of the ILC interaction region it can even double. Assuming 30% double hits and pixels of $25 \times 25\,\mu\text{m}^2$ size the hit occupancy in one train will be about 10%. This occupancy is probably unacceptable for cluster reconstruction and pattern recognition so that a sensor operated this close to the beam must be read out several times during one bunch train. A line readout rate of 40 MHz would decrease the occupancy by a factor of 20 to half a percent (for a sensor with 4096 pixels read out at both ends).

▷ Operation in a magnetic field of 3-5 T. The effect of the Lorentz angle is expected to be small due to the thin sensor.

The status of the project as reported in the PRC review in May 2005 [25] was:

▷ Small (64×128 pixel) DEPFET matrices with close to ILC pixel sizes ($32\ \mu$m $\times$ $24\ \mu$m) had been produced successfully at the MPI semiconductor laboratory.

▷ Single pixels had been successfully operated in laboratory setups. Low noise and complete, fast clear had been demonstrated [12].

▷ A 128 channel readout chip (CURO) had been designed and produced. The chip operated in stand alone mode with the required rate.

▷ A 2×64 channel control chip (Switcher II) needed to switch the DEPFET gate and clear contact had been designed and produced. The chip works at the required frequency.

▷ A system made of a 64×128 DEPFET Matrix, CURO and Switcher II had been built and operated successfully in the laboratory and in a beam test. However, the required noise performance and system speed had not yet been achieved

▷ DEPFET pixels had been irradiated up to 1 Mrad and were still operational.

▷ The thinning process had been developed on 4" wafers. Using diodes it could be demonstrated that basic properties of a sensor did not deteriorate during the thinning process.

The main goals since the last PRC review in may 2005 were:

▷ Radiation tests of the ASIC electronics and further tests of the DEPFET with different particle types.

▷ Carry out a rigorous test beam program to assess the performance of the full DEPFET system in a particle environment, preferentially in high energy beams at CERN.

- ▷ Determine the limits of noise and readout speed of the present system.
- ▷ Design a new generation of readout chips adapted to the known parameters of the matrices favoured by the test program.
- ▷ Prepare for the construction of a 512×512 close to full size system with multiple readout chips.
- ▷ Enlarge the collaboration.

Almost all of these goals have been achieved or are close to being achieved. They will be detailed in the following sections. The report is organized as follows: Section 2 describes the DEPFET sensor. After a short introduction of the operation principle, the production technology and some of the implemented structures are described. Section 3 describes the ASIC electronics for control and readout. Section 4 proposes a system for operation at ILC. Results form laboratory tests and beam tests are summarized in Section 5, including radiation hardness studies in Section 5.2. In section 6 software development is described. The simulation software is especially useful to extrapolate the performance to ILC conditions using parameters extracted from beam tests. In section 7 an overview on new developments presently in production is given. A summary and outlook is given in Section 8.

2 The DEPFET Sensor

2.1 DEPFET Principle and Operation

The DEPleted Field Effect Transistor structure, abbreviated DEPFET, provides detection and amplification properties jointly. The concept was proposed in 1987 [4] and developed to a level of maturity in the nineties [5–8].

The DEPFET principle of operation is shown in Figure 1. A MOS or junction field effect transistor is integrated onto a detector substrate. By means of sidewards depletion [9] and additional n-implants below the transistor a potential minimum for electrons is created underneath ($\approx 1\,\mu$m) the transistor channel. This can be considered as an internal gate of the transistor. A particle entering the detector creates electron-hole pairs in the fully depleted silicon substrate. While the holes drift into the rear contact of the detector, the electrons are collected in the internal gate where they are stored. The signal charge leads to a change in the potential of the internal gate, resulting in a modulation of the channel current of the transistor.

The simultaneous detection and amplification feature makes DEPFET pixel detectors very attractive for low noise operation [10, 11] and hence very large S/N. In the case of the ILC the use of very thin ($50\,\mu$m) detectors (see sect. 3.4) operated with very low power consumption (see sect. 4.1) is planned. The low noise, even at room temperature, is obtained because the capacitance of the internal gate is very small, much smaller than the

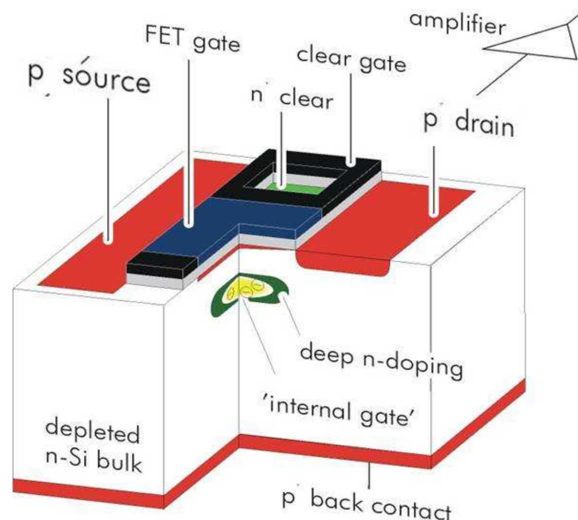

Figure 1: The DEPFET detector and amplification structure is based on planar p-channel MOSFET structure on a completely depleted substrate. A deep n-implant forms a potential minimum for electrons which are collected there. The accumulated charge in this internal gate modulates the transistor current. The charge can be removed by the clear contact.

pixel cell area which governs the capacitance of standard pn-junction pixels in hybrid pixel detectors. Furthermore, no external connection circuitry to the first amplification stage is needed. External amplification enters only at the second level stage. The pixel delivers a current signal which is roughly proportional to the number of collected electrons in the internal gate. Signal electrons as well as electrons accumulated from bulk leakage current must be removed from the internal gate after readout. Clearing, i.e. the removal of charges from the internal gate, is performed by periodically applying a positive voltage pulse to a *clear* contact. The potential barrier between the internal gate and the *clear* contact can be lowered by an additional *clear-gate* which may be held at constant potential but which may also be pulsed. For individual pixel structures with full charge collection, the best noise value measured so far at room temperature is $1.6\,e^-$ (see Figure 2).

For the ILC, where speed is the driving element, a total noise contribution of $\lesssim 100\,e^-$, including noise from the DEPFET sensor and from the readout chip, is the realistic goal. As the output of a DEPFET is a current, further processing of the signal is current based. This also allows high-speed on-chip pedestal subtraction, simply by subtracting two – signal and pedestal – currents (see sect. 3.1).

2.2 DEPFET Operation

In a real detector a single DEPFET pixel will be operated as follows:

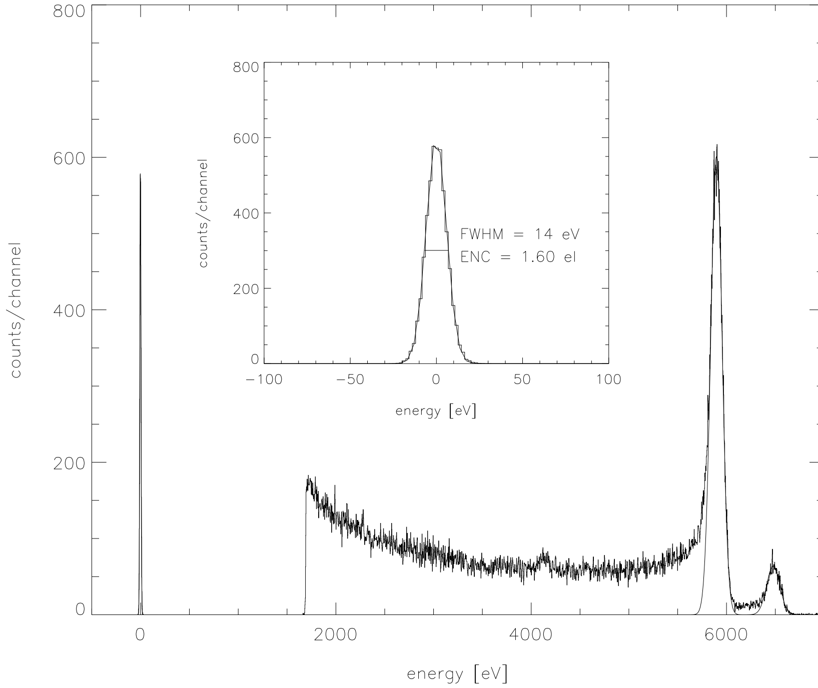

Figure 2: Fe^{55} spectrum obtained using a linear DEPFET single pixel in ILC layout at room temperature and $10\mu s$ shaping time. The rms noise of 1.6 e^- is obtained from the width of the pedestal.

- ▷ The DEPFET is switched off. In this state the transistor consumes almost no power, however, the pixel is sensitive to ionizing particles. Electrons generated by ionisation in the depleted bulk will drift towards the internal gate and accumulate there.
- ▷ During a readout cycle a voltage (above the transistor threshold) is applied to the external gate, switching on the transistor. The source-drain current, composed of a pedestal current defined by the external gate and a signal current, proportional to the charge in the internal gate, is measured.
- ▷ A voltage is applied to the clear contact, removing completely the signal charge in the internal gate.
- ▷ Now the current is measured again, this time measuring the pedestal current. In an external readout circuit this pedestal is subtracted from the first reading, the difference giving the signal.
- ▷ The external gate voltage is set back, switching off the transistor.

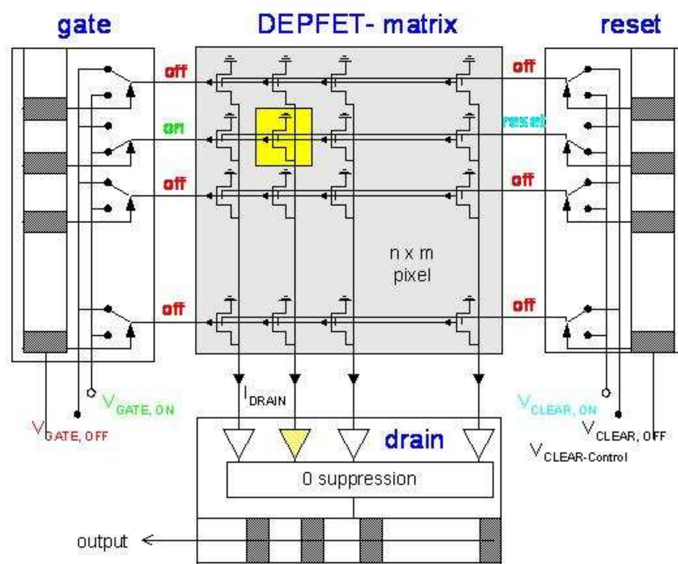

Figure 3: Schematics of a DEPFET matrix. Drains reading the current are connected column wise to a readout chip. Gates and clears are connected row wise to switcher chips. The switcher steps through the rows while all pixels of a row are read in parallel.

This sample-clear-sample cycle is planned to be as short as 50 ns. In a pixel detector the pixels will be arranged in columns and rows (see Figure 3). All transistor drains of a column are connected to one amplifier node. The gate contacts and clear contacts are connected row wise, thus all pixels in a row can be read and cleared in parallel. In a rolling shutter mode readout, one row is switched on and all pixels of this row are read (sample-clear-sample cycle) in parallel. Then this row is switched off and the next row is read and so forth until all rows have been read and the cycle starts again. This way the readout of a complete frame[8] needs about 50 μs. This scheme resembles the readout of a column parallel CCD, the signals are read out sequentially by a chip at the periphery. But unlike in an CCD no charge transfer is needed and only one row is electrically active. Actually, it is possible to address each pixel individually. Hence the sensor could be divided into different sections which are read with different frame rates, e.g. if the background occupancy is inhomogeneous. Even a triggered ROI (region of interest) readout can be realized.

[8]In our design proposal (sect 4) a frame of the innermost ladder has 1024 rows

2.3 PXD4 Pixel Production

In 2004 the first prototype DEPFET matrices were produced. The production (dubbed PXD4) was made on high ohmic unthinned (450 μm thick) high resistivity 6” FZ wafers. Double poly and double metal technology was introduced into the process line to build the complex DEPFET matrices with FET and clear gates and crossed contact lines (Figure 4). The largest matrices contained 64×128 pixels. On the same wafers prototype matrices for x-ray imaging (large circular pixels) for astrophysics use were produced. The production contained several variants, e.g. using different clear structures. To improve the clear behavior, an extra high energy implant (HE) was implemented in some matrices. This has the disadvantage that the distance between the potential minimum where the charge is collected and the channel increases leading to a smaller gain.

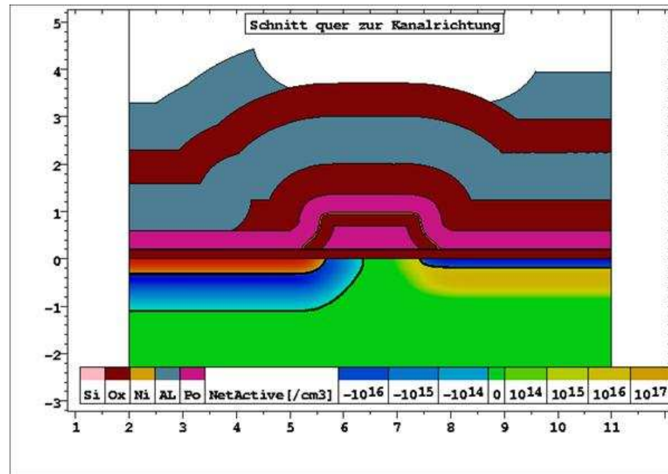

Figure 4: Cross section through an DEPFET pixel.

An interesting feature is the double pixel. Two pixels in adjacent rows share the same clear structure and their transistor gates are connected together. On the other hand the drain readout lines (for the signal readout) are routed in separate columns. This allows a very compact design resulting in small pixels sizes. For practical operation it has the advantage that two rows are read out in parallel, thus virtually doubling the readout speed. The price to pay is twice the number of readout lines.

3 The Readout and Control ASIC

As explained in the previous section two ASIC chips are necessary to operate a DEPFET matrix: Firstly a switcher chip which generates row wise the voltages needed to switch on the transistor and activates the clear. Secondly a chip reading out the current signal of all columns in parallel. The latter

should automatically subtract the pedestal in the sample-clear-sample cycle and store the result. Furthermore, it could perform 0-suppression, cluster finding and sparse readout, eventually digitizing the data on chip.
A complete system needs in addition a controller, which synchronizes switcher and readout chips.

3.1 The CURO Readout Chip

A fast operation as required at the ILC was the major design goal for the readout chip [16]. Therefore, signal processing (e.g. pedestal subtraction, signal storage and compare) on the chip is done in a current-mode operation perfectly adapted to the current signal of the DEPFET device. Furthermore, a subtraction of two signals as needed for the pedestal subtraction can be done very fast and accurate with currents. By means of the pedestal subtraction described above a fast correlated double sampling is performed suppressing the 1/f noise contribution of the sensor. The 128 channel chip offers the possibility of zero-suppression and sparse readout. All hits in a row are found by comparison to programmable and trimmable thresholds. The analog amplitudes as well as the digital hit pattern are stored in a mixed signal memory. The digital hit pattern is scanned by a fast hit finder. The addresses of the hits are stored in a RAM for later readout, the corresponding analog amplitudes are multiplexed to off-chip ADCs (which could be integrated onto the chip in a later version). The address RAM can be read during the long bunch pause. The addresses are then associated to the digitized values. The CURO chip has been fabricated using a $0.25\,\mu$m process. Radiation tolerance for the doses expected at the ILC is therefore not considered to be a critical issue. The hit detection and zero suppression (i.e. the digital part) has been operated successfully at more than 100 MHz. The analog part (double correlated sampling, current comparison) has been tested up to a row rate of 25 MHz with sufficient accuracy. The intrinsic noise contribution of the sampling in the chip at this speed has been measured to be 100 nA. This is somewhat in disagreement with the calculated value (about a factor of two larger [16]). For the present DEPFET devices with a charge to current gain of up to $g_q \approx 400\,\mathrm{pA/\,e^-}$, this translates to a noise contribution of the fast readout of $\mathrm{ENC} = 250\,\mathrm{e^-}$.

3.2 The Switcher II Control Chip

The SWITCHER-II[9] chip is used to apply suited potentials to the rows of the matrix. Three signals are required in the prototype devices: external gate, clear and clear-gate, the latter being probably not required for future designs. One SWITCHER can provide two voltages for 64 channels. The i-th channels is first selected by an internal counter. An on-chip sequencer

[9] a previous, low speed version in a different technology was used for slower matrices

is used to connect the outputs to externally supplied voltages by means of simple analog multiplexers in an arbitrary sequence. The multiplexers use high voltage transistors so that voltages of up to 25 V can be used. The multiplexers have been optimized for high speed by providing a low output resistance of typically 500 Ω for the rising edge and 200 Ω for the falling edge. The falling edge is more important because it switches 'on' the gates or 'off' the clear signals. The chip operates at the required rate of 50 MHz. Level shifters are used to control the high voltage transistors from a digital control section supplied with a floating 5 V supply. Several SWITCHER chips can be daisy chained by signals at the top and at the bottom. The active channel is then automatically stepping through one chip and then to the next chip above or below, depending on a programmed direction flag.

3.3 Test System

A test system for operation of a 64 × 128 pixel PXD4 matrix read out by one CURO and controlled by two Switchers (one for FET gate control, one for clear) has been constructed. The system is controlled by a FPGA, data transfer to a PC is done via an USB link. Several systems were built and distributed in the collaboration. Most of the measurements reported were obtained using these systems [13–15]. They were also used as DUTs in the beam tests at DESY [13] and as telescope planes and DUTs in the CERN beam test (see 5.3).

3.4 Wafer Thinning

One of the design goals for an ILC vertex detector is to minimize multiple scattering by allowing only 0.1% of a radiation length (X_0) per layer. Since silicon alone has an X_0 of 9.36 cm this material budget would already be used up by a sensor thickness of 100 μm. Giving room to additional contributions from readout and control electronics and routing material the silicon thickness should not exceed 50 μm. A thinning process has been developed based on wafer bonding and anisotropic etching which allows to produce monolithic structures with thin sensors and a support frame. The process is described in the last PRC report [24] and in [20]. Since then the process has been transferred from 4" wafers to the 6" wafers and bonding and thinning is done by industry. Thin diodes made with this thinning technology have a reverse current of $< 100\ pA/cm^2$ at $U_{bias} < 100V$ (see Figure 5), thus keeping the excellent properties of the material before thinning.

Large mechanical samples have been produced corresponding to the proposed ILC detector size (inner layer, Fig 6). In order to reduce the material further a hole pattern can be etched into the support frame (Figure 7). This reduces the material in the support frame by 33%.

Including switcher chips and gold bumps a material budget of 0.12% can

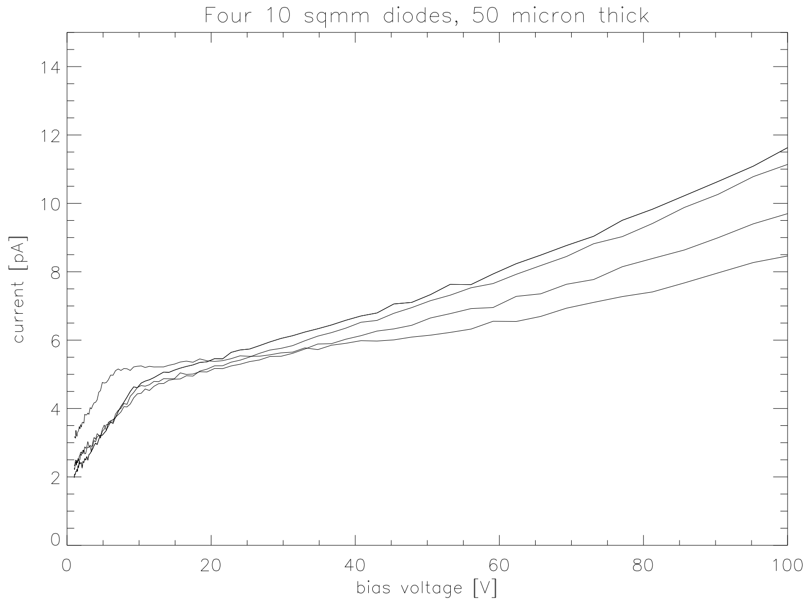

Figure 5: Reverse currents measured in diodes after thinning to 50 μm.

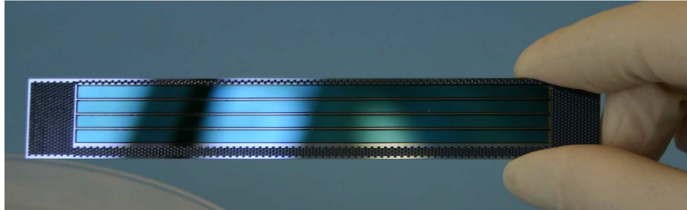

Figure 6: Mechanical sample of the ILC sensor. The inner area is thinned to 50 μm. The sensor (area 10 cm $\times$ 1.3 cm) is supported by a frame of 450 μm thick silicon. This frame provides mechanical rigidness and support for ASIC chips. The width of the frame along the module is 1 mm and 3 mm respectively. Despite the thin sensor area the structure can still be handled manually.

be achieved with such a module (Table 1). This accounts for all material within the acceptance of the vertex detector $|\cos(\Theta)| < 0.96$ ($\pm$5 cm at R=1.5 cm).

Such an all silicon module would need no additional support material. There is no need of gluing thinned, fragile silicon sensors on such support materials. In addition there is no CTE mismatch of different materials.

For structures of 10 cm $\times$ 1.3 cm (50 μm thick) supported by such a frame of 1 mm and 3 mm along the module a gravitational sag of 20 μm has been measured [21], which is considered to be tolerable.

The next step will be the production of passive pixel detectors on thin

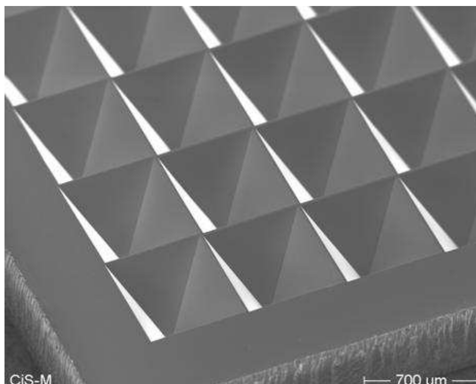

Figure 7: Microphotography of a hole pattern etched into the support frame for material reduction.

component	material	X_0 cm	area mm^2	thickness μm	equiv. thickness μm	$\%X_0$
sensor	Si	9.36	13 × 100	50	50	0.05
frame	Si	9.36	2 × 100	450	45	0.05
Switcher	Si	9.36	3 × 100	50	11.5	0.01
gold bumps	Au	0.33			0.46	0.01
all						0.12

Table 1: Material breakdown of the proposed ILC module (innermost layer module). The material is normalized to the sensitive area of 13 × 100 mm^2. The gold bumps (gate and clear per line, service bumps for switcher) have a diameter of 48 μm

material (2007) and a DEPFET production in 2008/2009.

4 Layout of a DEPFET System for ILC

In the present planning we want to use eight sensor modules in the inner layer, each 10 cm long and 1.3 cm wide. These eight modules cover the innermost radius of 1.5 cm with some overlap. Each module has 512 pixels (pitch 25 μm in R-ϕ) and 4096 along z. Readout is done from both sides, each side serving 512 × 2048 pixels. Due to the double pixel structure (explained in Section 2.3) the effective row number per half is 1024, with 1024 readout channels. With 50 ns readout time per (double-) row, a complete frame can be read in 50 μsec, and 20 readout cycles can be performed during a bunch train of 1 ms. In the outer layers background occupancy is less prominent and longer readout times and hence longer module dimensions are possible. A possible layout is described in Table 2, a view of the inner layer is shown

Layer	Number of ladders	Radius (mm)	Ladder length (mm)	width (mm)	readout time
1	8	15.5	100	13	50 μs
2	8	26.0	2×125	22	250 μs
3	12	38.0	2×125	22	250 μs
4	16	49.0	2×125	22	250 μs
5	20	60.0	2×125	22	250 μs

Table 2: Default geometrical parameters of the DEPFET based ILC micro-vertex detector.

in Figure 8.

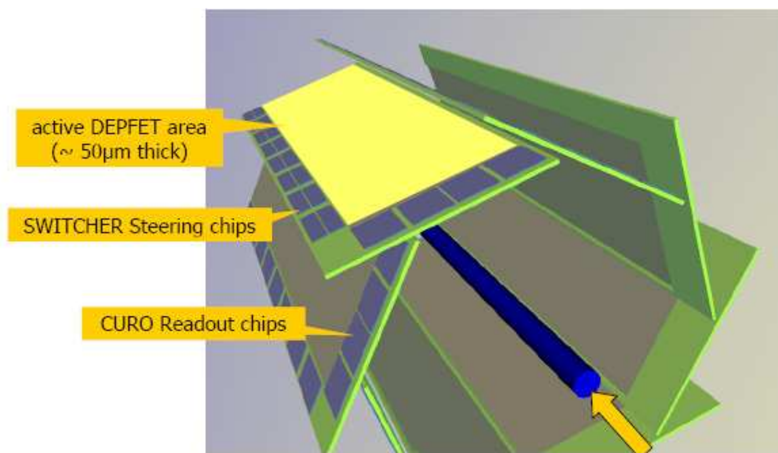

Figure 8: Artist's view of the innermost layer of the ILC vertex detector. Eight modules form the inner layer (one module per ladder). Each module is read out at both ends (only half of a module is shown). Along the module switcher chips control the FET gates and clears. In the outer layers a ladder is made from two modules, each module is read out at one end.

4.1 Total Power Consumption

The DEPFET has the inherent advantage that only during the readout sequence a pixel consumes power. In between readout cycles power consumption is almost zero although the pixel is sensitive to ionising particles. The power consumption of an active pixel is 500 μW. In a module of an inner layer 2×1024 pixels are active at a time (two double rows), resulting in 1W per ladder. The switchers consume 225mW per active row, 50mW for an active chip and 10mW for the idle chips,(Switcher III, see section 7.2), with two active rows and two (out of 32) active switcher this adds to 0.85W.

layer	ladders	active rows	columns	power/ladder	power/layer
1	8	2	1024	12W	96W
2	8	2	1535	21W	168W
3	12	2	1536	21W	252W
4	16	2	1536	21W	336W
5	20	2	1536	21W	420W
all					1272W

Table 3: Power dissipation per layer. The total power is 1272W, however, with the ILC duty cycle of 1/200 this is reduced to 6.4W

A channel of the readout chips (DCD1, see section 7.3) consumes 5 mW, hence the 2048 channels total to 10.2W, the dominant contribution. Altogether a inner ladder consumes about 12W. The outer modules are slightly wider and longer, hence produce 21W per ladder. These values and a total breakdown are listed in Table 3. Altogether a complete detector dissipates 1272W. However, most of the active electronics can be switched off in the pause between the bunches. This reduces the total power by a factor of 1/200 and the complete vertex detector should dissipate on average about 6.4W. It should be stressed that most of the power is consumed by the electronics at the module ends, outside the acceptance, where cooling structures - if needed - are less critical. Still the low average power suggests that air cooling is sufficient.

5 Test Results

5.1 Laboratory Test

The DEPFETs are known for very low noise. Noise values as low as 1.6 electrons have been measured with linear, ILC like DEPFETs, albeit at long integration times (10 μs). The noise depends on the integration time τ like

$$ENC = \sqrt{\alpha \frac{8kTg_m}{3g_q^2} \frac{1}{\tau} + 2\pi a_f C_{tot}^2 + qI_{Leak}\tau} \qquad (1)$$

The first term corresponds to the thermal noise of the DEPFET FET, α is a factor, appr. unity, depending on the exact shaping of the amplifier, g_m is the transconductance, g_q the charge amplification, and kT the thermal energy. The second term is the 1/f noise (with a process dependent normalisation factor a_f, C_{tot} the effective capacitance) and the third term is the shot noise due to the DEPFET leakage current I_{leak}. Hence an increased noise is expected at a bandwidth of 50 MHz as needed at ILC[10]. From calcu-

[10] The line rate of 40 MHz as required by the occupancy is reduced to 20 MHz due to the

lations and extrapolations of the measurements obtained with long shaping times we expect that the intrinsic noise is well below 100 electrons at 50 MHz, dominated by the thermal noise. Unfortunately problems running a DEPFET/CURO system at high speed made it impossible to measure this noise directly. Therefore we used a single pixel with a high bandwidth amplifier to measure this intrinsic noise. The result is shown in Figure 9. At full ILC speed the intrinsic noise of a DEPFET is still below 40 electrons.

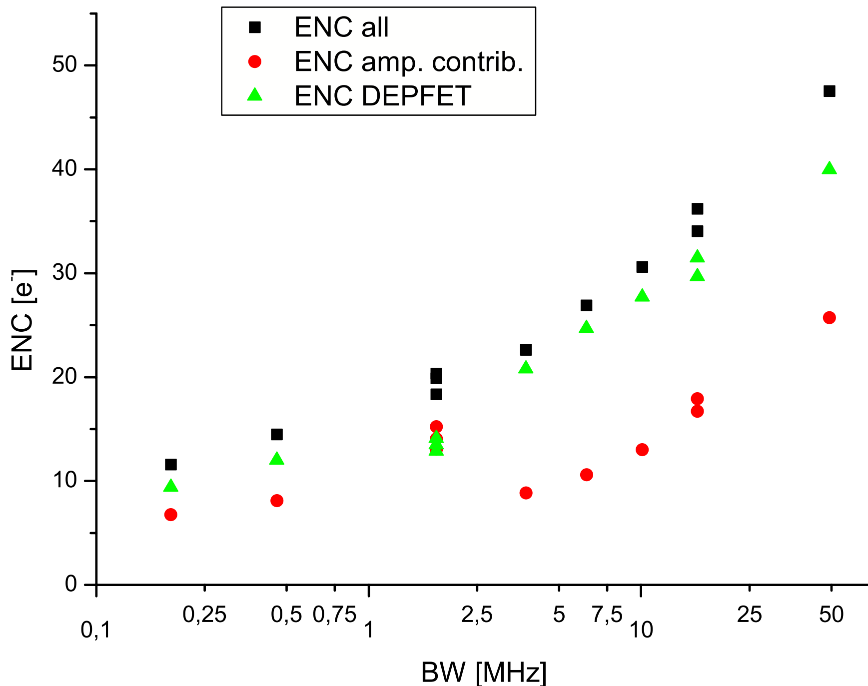

Figure 9: Noise of a DEPFET structure as function of the bandwidths of the readout node.

A Fe^{55} spectrum obtained at 50 MHz bandwidth is shown in Figure 10.

In system tests and beam tests the best noise obtained was 250 electrons, albeit at lower speed. One reason for this is a non-optimized design of the CURO. Further noise sources have been pick up (internally in the CURO and of external amplifiers). Measurements of the CURO noise as a function of the readout speed and the load capacitance have been performed, see Figure 11. At zero load capacitance the system has an acceptable noise, independent of the frequency of about 100 nA (with a g_q of 0.4 nA/e this corresponds to an S/N of 16/1 for 50 μm sensors). However, at higher capacitances the noise increases dramatically, especially at high frequencies reaching 500 nA at 33pF and 50 MHz. This would correspond to an unacceptable S/N of 3/1. A capacitance of $\approx$ 40 pF is expected for a full size module of 5 cm

double pixels. However, each readout cycle requires two samplings and a clear in between, hence an effective sampling bandwidth of 50 MHz is needed

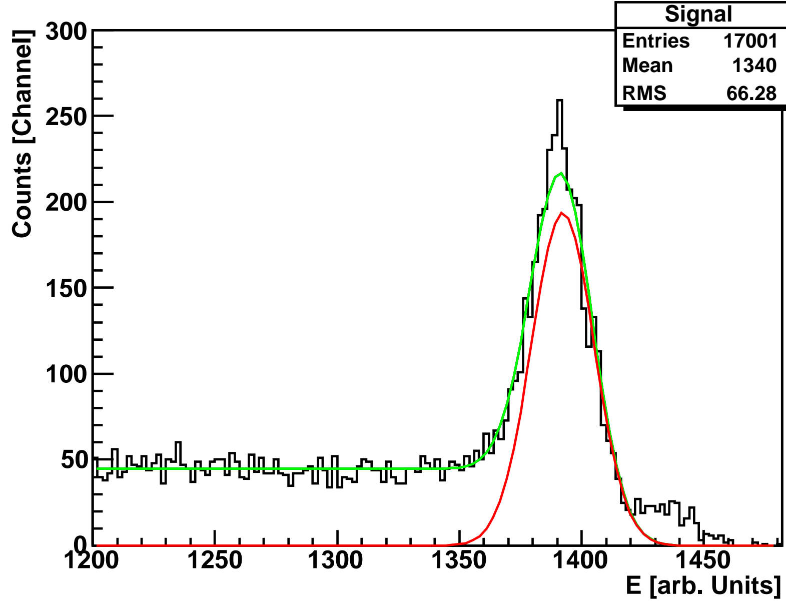

Figure 10: Fe55 spectrum measured with a DEPFET using a fast amplifier with 50 MHz bandwidth.

Type	protons 30MeV	neutrons 1-20MEV	$Co^60\ \gamma$
DOSE	1.2×10^{12} n/cm^2	1.6×10^{11} n/cm^2	913 kRad
1MeV n eq.	3×10^{12} n/cm^2	2.4×10^{11} n/cm^2	
years ILC	2	35	30

Table 4: Irradiation tests of DEPFETs

length. It should be mentioned that the CURO chip was not designed for large matrices. However, for the next generation of the readout ASICs this has been taken into account.

5.2 Radiation Hardness Tests

The gamma irradiations reported in the PRC review 2005 were completed with neutron and proton irradiations performed at the LBNL in Berkeley (table 4).

Different radiation leads to different damage:

- ▷ Ionising radiation (γ, charged particles) leads to oxide damage, due to creation of positive oxide charges at the $SiO_2 - Si$ interface. In FET transistors this leads to a shift of the threshold to negative values (compensation of the positive charges) In addition interface traps reduce the mobility and hence the transconductance of the device.

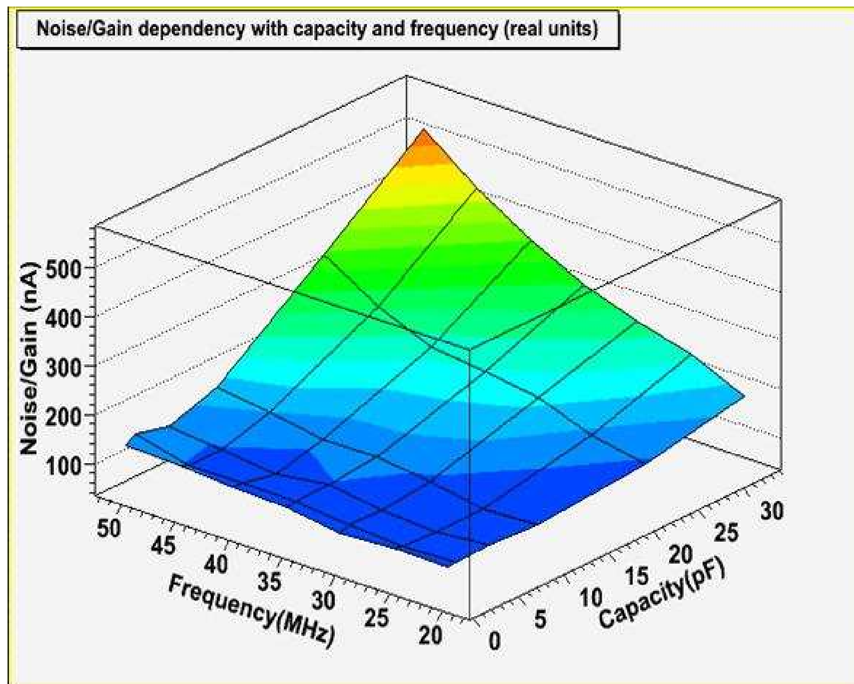

Figure 11: CURO noise as function of frequency and load capacitance.

- ▷ Bulk damage by NIEL (non ionising energy loss) from neutrons and charged hadrons (to a lesser extend also from electrons) leads to an increase of the bulk leakage current. Further damage, like a change of the effective doping concentration is not expected at the doses relevant for ILC.

The irradiation results can be summarized (Figure 12):

- ▷ Gamma irradiation leads to a shift of the threshold voltage. The shift is approx 4V and can be compensated. No other significant effects are observed.
- ▷ Neutron irradiations should lead only to bulk damage by NIEL, no oxide damage should be observed. Indeed no shift of the threshold voltage and no significant change of the subthreshold slope could be observed. A slightly increased noise at higher temperatures indicates additional shot noise due to higher leakage currents.
- ▷ Proton irradiation lead both to oxide and bulk damage. Threshold voltage shifts of 5V were observed and an increase of the subthreshold slope indicates and increase of 1/f noise. g_m is reduced by 15%. The bulk damage - an increase of the leakage current - leads to an increase of the shot noise, especially at large integration times. Reducing the sensor temperature reduces this contribution significantly.

At ILC the shot noise contribution will be proportional to the readout time of a complete matrix. Between two consecutive readouts the cell accumulates leakage current. This will lead to an offset which can be corrected for. However, the fluctuations of this contribution lead to noise. For a readout cycle of 50 μs as planned for the inner layer the noise contribution would be 95 electrons. Cooling to 0^0C reduces this to 22 electrons. However, it must be kept in mind that the dose of the tested device corresponds to 35 years of ILC operation.

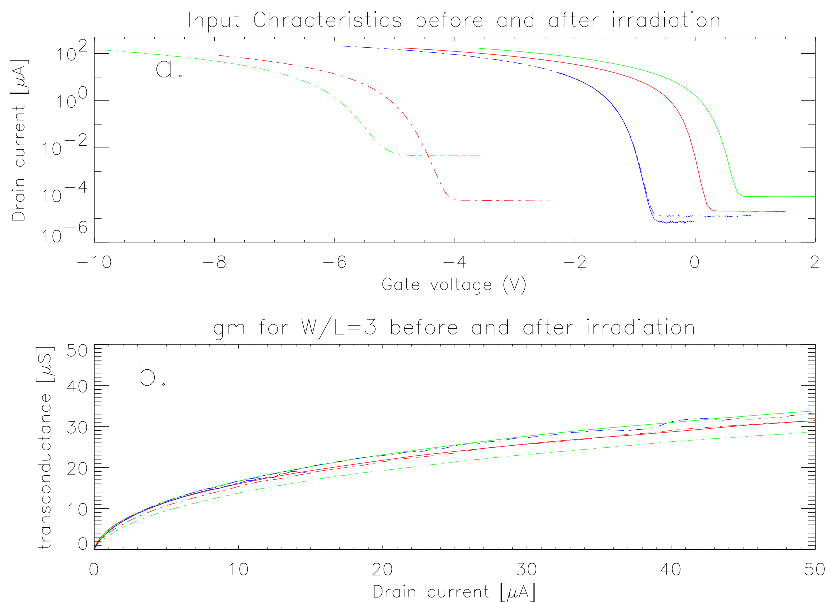

Figure 12: Transistor characteristics (upper figure) and transconductance (lower figure) of DEPFETs before (solid lines) and after (dashed dotted lines) γ (red), proton (green) and neutron (blue) irradiations.

5.3 Test Beam Results

During the period 2005-2006 beam tests have been performed at DESY and later at CERN (SPS). At the DESY beam test the main goals were a comparison of different DEPFET types, different operational settings, efficiency and purity studies, angular scans and an initial position resolution.

At DESY, the electron beam energy is limited to 6 GeV. Due to multiple scattering and the limited precision of the telescope used, the uncertainty on the predicted position was limited to about 5-6 μm. This was corroborated using a GEANT simulation [30].

At CERN a high energy beam consisting of typically 180 GeV π's was used. To improve the precision on the predicted position a telescope consisting of five DEPFET planes was built. This resulted in an uncertainty on the

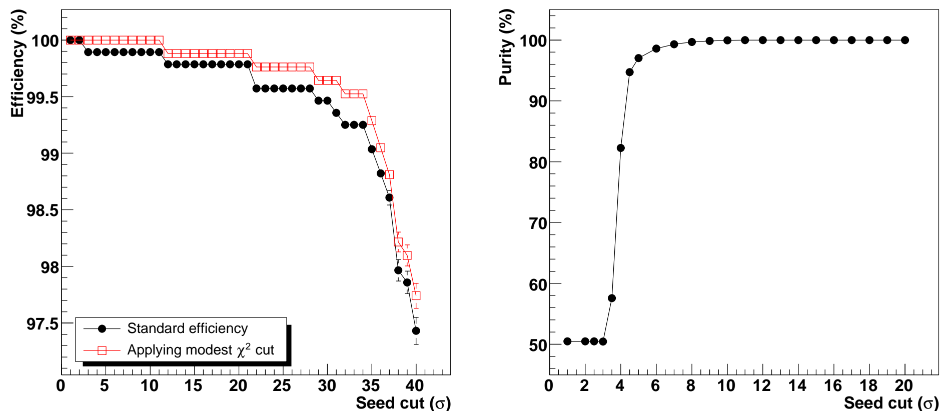

Figure 13: Efficiency ($left$) and purity ($right$) as a function of the seedcut for a CCG-HE DEPFET.

predicted position of less than 1 μm and a single hit resolution better than 2 μm at a DEPFET S/N>110. At CERN also the zero-suppression capability of the CURO was tested, see section 5.3.4. The last CERN beam test was finished on the 1st of November, hence the analysis of the CERN data is still in progress.

5.3.1 Device and Parameter Studies

DEPFET devices are available in different pixel sizes (Y×X): 22×36, 28.5×36 and 24×36 μm^2. In some DEPFET types, it was necessary to pulse the $CLEAR\ GATE$ contact. This has as disadvantage that extra control lines are required. It is also possible to keep the $CLEAR\ GATE$ contact at a constant potential. This is referred to as a Common-Clear-gate (CCG) matrix. The improve the clear behavior, an extra high energy implant (HE) was implemented in some matrices. DEPFETs using the CCG-technology with the HE implant display the same S/N (112.0±0.3 and 114.2±0.2) as a DEPFET without HE implant but with a clocked $CLEAR\ GATE$ (112.7±0.2). DEPFETs with CCG-technology but without the HE implant perform worse, most likely due to extra noise by an incomplete clear.

5.3.2 Efficiency and Purity Studies

Efficiency

$$E = \frac{\#clusters}{\#good\ tracks} \quad (2)$$

and purity

$$Purity = \frac{\#good\ clusters}{\#all\ clusters} = \frac{\#good\ clusters}{\#good + bad\ clusters} \tag{3}$$

is shown in Figure 13. The main result of the efficiency and purity measurement is that we can run with almost 100% purity and efficiency when using a seed cut of $\approx$5-7σ. Note that this is a very low cut at only $\approx$5% of the most probable MIP signal.

5.3.3 Angular Scans

During one of the beam tests, the angle of incidence was varied. Rotations around both the X-axis (ϕ) and the Y-axis (θ) were made, between 0 and 40°.

At large angles, tracks traverse the silicon underneath many pixels. Hence, the signal per pixel is very low. This allows the study of charge generation in thin layers and the charge collection directly underneath the DEPFET pixel where the field lines are non-trivial. These studies are very important for the tuning of the GEANT simulation for the 50 μm thick DEPFETs foreseen for ILC operation. The comparison is shown in figure 14. The correspondence is excellent. The small difference at large angle is due to incomplete clustering in the data. In the data it is demanded that the neighbors carry a signal larger than threshold. At large angle some clusters are therefore terminated too early. These data provide a basis for the GEANT4 simulation of thin sensors (see section 6)

5.3.4 Zero-Suppression

In case that the background rates at the ILC are low, 0-suppression can be used to reduce the data volume. Therefore, a 0-suppression capability was implemented in the CURO. At CERN also the 0-suppression capability was tested in a beam test. In figure 15 cluster signal distributions using a low, a medium and a high threshold are shown. The distributions follow the expected behavior. For low thresholds some noise fluctuations are (falsely) identified as signal clusters. Furthermore, many neighbors are included in the cluster. Both effects lead to a wide signal distribution with a tail to lower signals. When the threshold is increased, the background clusters are excluded, removing the tail on the lower signal side. At even higher threshold, the signals on the neighbors are not included anymore in the cluster, leading to a narrow cluster signal distribution. The analysis is still in progress. But the result demonstrates that the CURO can be read out 0-suppressed.

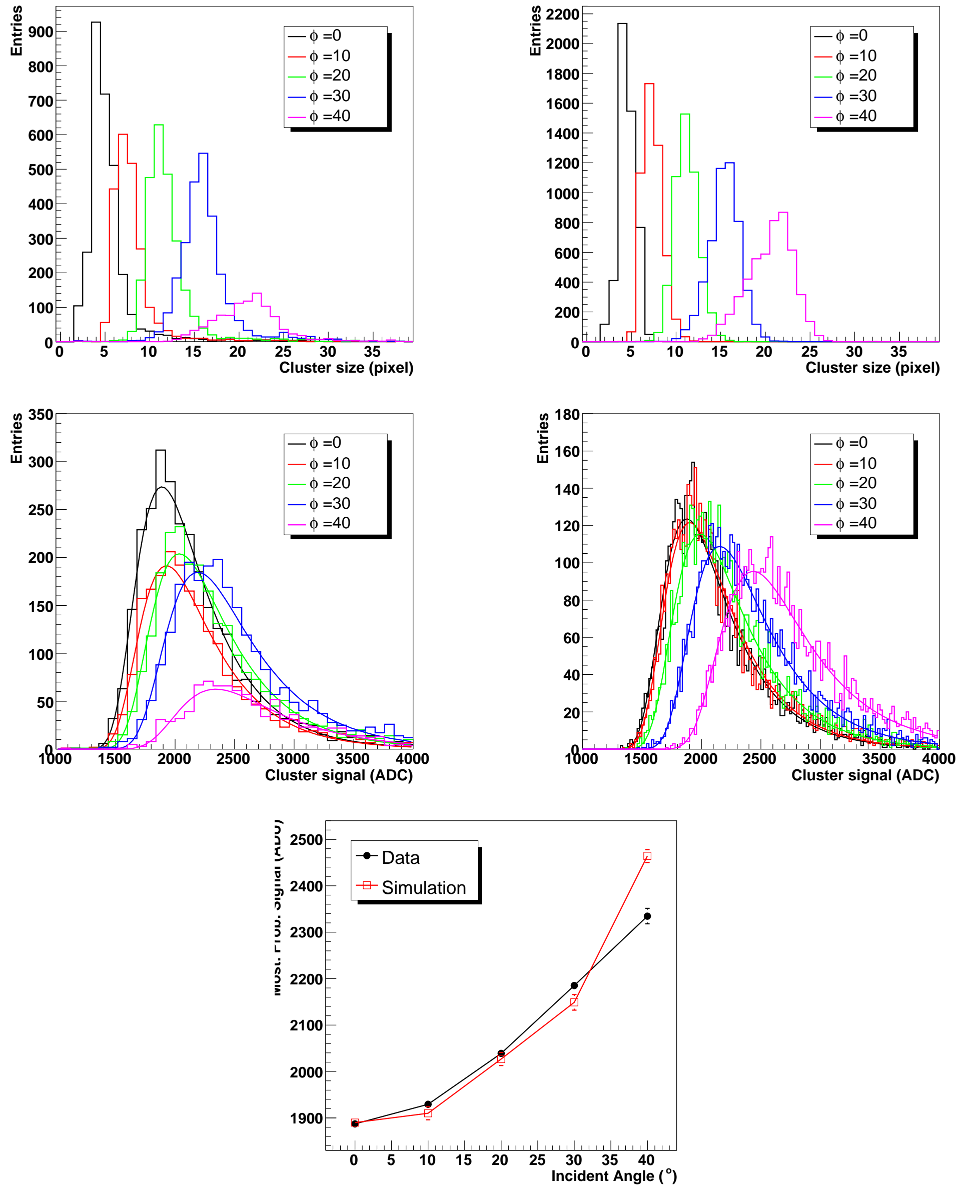

Figure 14: Comparison between data and GEANT simulation for the 450 μm DEPFET prototype. On the left cluster size and signal as a function of ϕ, on the right the corresponding simulation results. Also shown is the most probable signal as a function of the angle of incidence in both data and simulation.

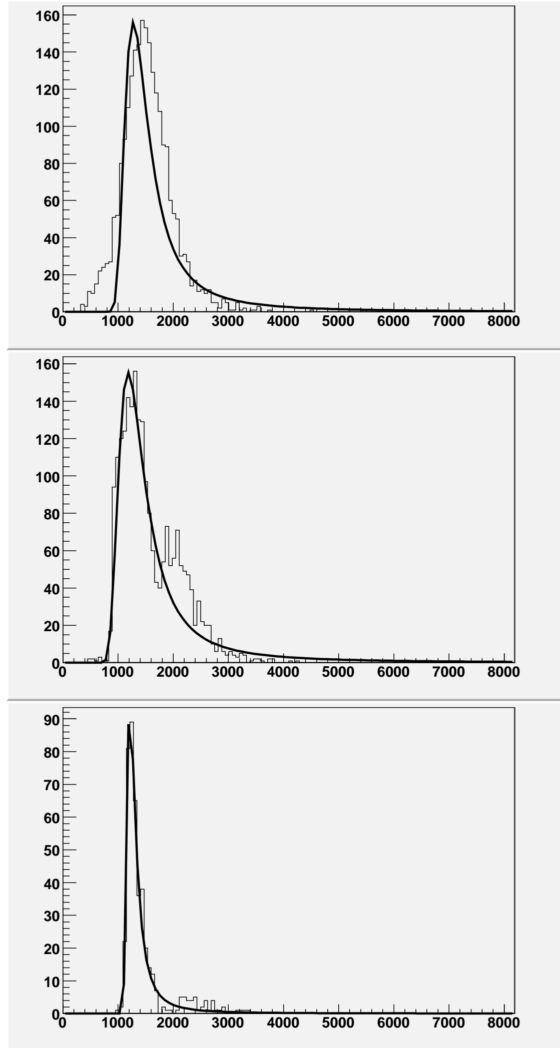

Figure 15: Cluster signals running the CURO with zero-suppression using a low (*top*), a medium (*middle*) and a high (*bottom*) threshold.

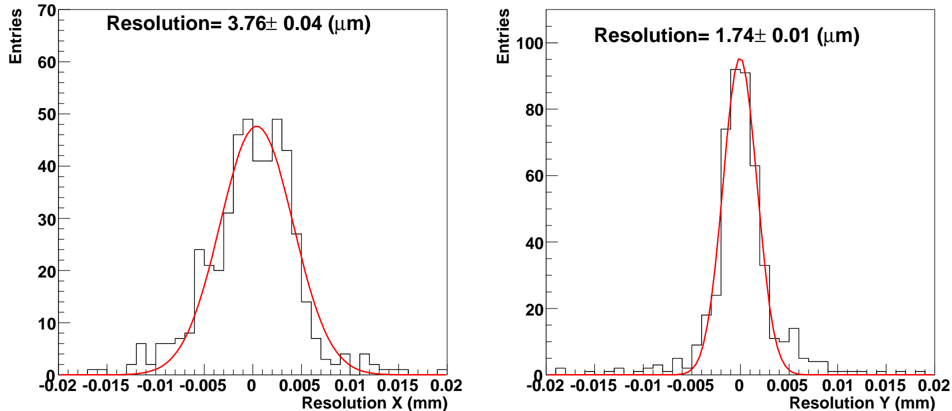

Figure 16: Residual width for a 36×22 μm (X×Y) DEPFET. The positions are reconstructed using the η algorithm.

5.3.5 High Precision Resolution Studies using a DEPFET Telescope

At DESY the tracking was limited by the precision of the telescope and multiple scattering. This telescope [26] has an intrinsic resolution of about 4-5 μm. From the GEANT4 simulation [30], it was known that the DEPFET position resolution was better than 2 μm. Optimally a telescope should have an extraplolation precision in the DUT plane better than the intrinsic resolution of the DUT. To improve the precision of the tracking, a DEPFET based telescope was developed and successfully operated.

Five DEPFETs were placed as close as possible to each other. Next to the improved precision, this also has the advantage that much more data on DEPFETs is collected. For the very high precision studies the middle DEPFET is used as DUT while the others are used as telescope planes. One edge DEPFET was also used for 0-suppression studies.

The hit positions are reconstructed using the η-algorithm. The residual distributions are displayed in figure 16. The position resolutions are quite good and still include a tracking and multiple scattering error. The resolution in direction with smaller pitch (22 μm) is 1.74 μm. Of course, this is for 450 μm thick sensors, the resolution of the 50 μm sensors will be worse (lower S/N, less charge sharing).

Using the software developed for [30], the uncertainty on the predicted position was studied. In figure 17 the error on the predicted position for this module is plotted as a function of the observed residual width for various beam energies. The plot demonstrates that the error on the predicted position is approximately 0.77 μm! These results are still preliminary. There is still room for improvement in the reconstructed position.

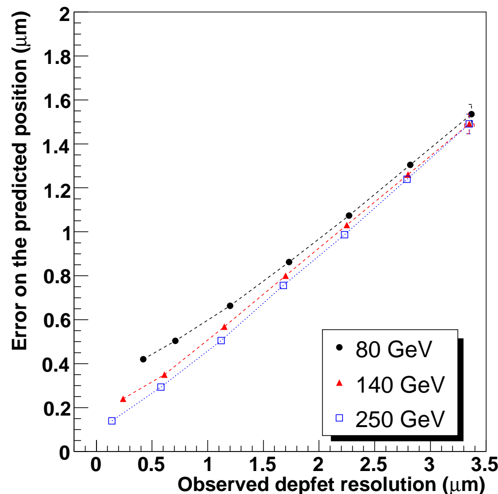

Figure 17: Error on the predicted position as a function of the observed residual width for various beam energies.

6 Software Development

Simulation and reconstruction software is the key ingredient for the ILC Detector optimisation and performance studies. As the ILC community entered the phase of intensive detector R&D, a need has arisen to have coherent and consistent software tools allowing to perform

- ▷ Detailed GEANT4 based modeling of particle interactions with the ILC detector.
- ▷ Realistic signal digitisation accounting for specific properties of readout sensors in various sub-detectors.
- ▷ Full event reconstruction, including track finding, calorimeter clustering, individual particle identification, jet reconstruction and calculation of event shape variables.

Over recent years much effort has been invested to create a software standard and data model for the ILC detector performance and physics studies. An example of software organization used in the study of the Large Detector Concept (LDC) and Global Linear Collider Detector concept (GLD) is illustrated in Figure 19. The detector simulation is performed with the GEANT4 based program Mokka [27]. The package Marlin [28] facilitates implementation of the signal digitisation procedure in various sub-detectors and different steps of event reconstruction in a modular way. The data flow is realized via the persistent LCIO (Linear Collider Input-Output) data model [29].

A detailed description of the DEPFET based vertex detector has been implemented as separate sub-detector driver within Mokka. The default layout of the device is as described in section 4. The geometry related parameters, namely

- ▷ number of layers,
- ▷ number of ladders in each layer,
- ▷ geometrical parameters defining support frames, electronics, cabling etc,
- ▷ length, width and thickness of the active silicon wafers in each ladder,

are stored in a mySQL database and read in on-the-fly when running Mokka. By modifying the content of the database the impact of the vertex detector geometry on the performance of the device can be studied.

The default geometrical parameters used in the simulation are detailed in Table 2.

The simulation of particle interactions with the material of the micro-vertex detector has been complemented with the detailed DEPFET sensor response modeling, accounting for

- ▷ fluctuation of energy loss along the particle trajectory within the active layer;
- ▷ diffusion of the released charge during its drift to the collection plane;
- ▷ Lorentz shift in the presence of the magnetic field;
- ▷ charge sharing across neighbouring pixels on the collection plane;
- ▷ electronic noise effects.

Simulation of the DEPFET sensor response is implemented as a separate Marlin module. Using the entry and exit points of a charged particle in the active layer as input, the module produces an output in terms of a list of fired pixels, characterized by their position within the wafers and induced charge. The simulation is controlled by steering parameters, including

- ▷ diffusion coefficient,
- ▷ factor converting energy lost into released charge,
- ▷ magnetic field,
- ▷ pixel dimensions,
- ▷ passive material.

The simulation code has been tuned and validated using DEPFET beam test data taken at DESY in fall 2005. The 450 μm thick DEPFET matrices have been exposed to a positron beam with an energy up to 6 GeV and their response have been studies as a function of particle incident angle. The parameters steering the simulation have been adjusted to ensure good agreement of simulation and beam test data (see sect. 5.3.3).

The validated software is used to study the performance of the DEPFET based ILC micro-vertex detector in terms of single point and impact parameter resolutions. Figure 20 demonstrates the single point resolution in $r-\phi$ and z as a function of the track polar angle for different thicknesses of the active sensor and pixel size. The noise is assumed to be 100 electrons, the silicon thickness to 50 μm corresponding to a S/N of 40:1 (for comparison simulations with 75 μm thick silicon were done as well). Dead material like the reinforcement frames and ASIC chips and beam pipe is implemented. The $r-\phi$ impact parameter resolution as a function of particle momentum for normally incident tracks and tracks at a polar angle of 45 degrees is shown in Figure 21. The $r-\phi$ impact parameter resolution is well described by the relation

$$\sigma(IP_{r-\phi}) = a \oplus \frac{b}{p \cdot \sin^{3/2}\theta},$$

where p and θ are particle momentum and polar angle, respectively. The constant term is found to be $a \sim 4.5$ μm independent of the active silicon wafer thickness and a multiple scattering term $b = 8.7(9.4)$ μm for the thickness of active silicon wafer of 50(75) μm. Thus, the DEPFET based vertex detector is expected to meet ILC requirements ($a < 5\mu$m, $b < 10\mu$m·GeV) [1], provided that pixel dimensions are smaller than 25x25 μm^2 and the thickness of the sensitive layer is smaller than 75 μm. It is worthwhile mentioning that the thicker Silicon results in an improved point resolution due to a better S/N. However, the impact parameter resolution gets slightly worse due to multiple scattering.

The simulations were done assuming a 4T magnetic field. The dependence of the $r-\phi$ resolution on the field is shown in Figure 18 and varies from 3-4.3 μm for 3 - 5 T.

To enable large scale detector optimisation and physics studies, a stand-alone pattern recognition procedure in the micro-vertex detector has been developed and integrated into the entire reconstruction chain within the Marlin framework. The stand-alone pattern recognition procedure in the vertex detector is applied to evaluate an impact of beam-induced backgrounds on the performance of the vertex detector.

At the ILC, the micro-vertex detector will operate in severe beam background conditions. The primary source of the background is beamstrahlung, i.e. a radiation of photons of the colliding electron/positron in the electromagnetic field of the opposite positron/electron bunch. The photons can in

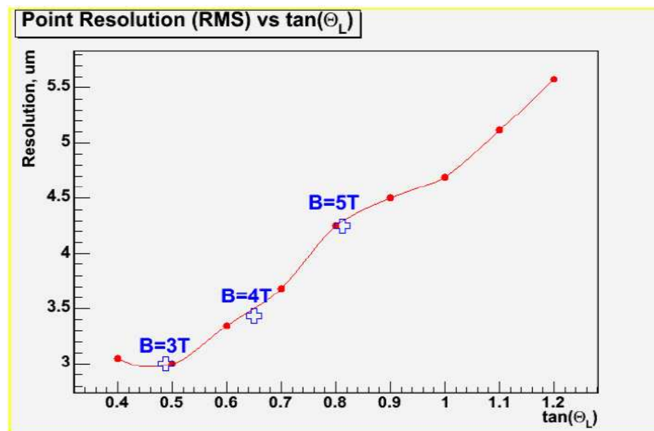

Figure 18: $r - \phi$ resolution as function of the Lorentz angle. The values for B=3, 4 and 5 T are indicated

turn produce e^+e^- pairs or crash into forward detectors, creating secondary particles. Both e^+e^- pairs and secondary particles, backscattering from the forward region, may hit the vertex detector, thus contaminating the hit pattern produced by the physics events. Recent Monte Carlo studies showed that in the innermost layers of the vertex detector one should expect several hundred background hits per bunch crossing [3]. The total amount of accumulated background strongly depends on the readout speed which directly translates into an integrated number of bunch-crossings. Three scenarios have been studied:

1. no background;
2. integration time of 25μs in the innermost layer and 50μs in the layers 2$-$5, this corresponds to 75(150) integrated bunch crossings in the layers 1(2$-$5); (optimistic)
3. integration time of 50μs in the innermost layer and 100μs in the layers 2$-$5, this corresponds to 150(300) integrated bunch crossings in the layers 1(2$-$5) (default).

For the nominal set of the ILC machine parameters the expected number of background hits in the vertex detector is given in Table 5. The parameters steering the pattern recognition procedure are optimized separately for each of the three scenarios considered to minimize fake track rate while maintaining track finding efficiency at reasonably high level. Hence, the track quality requirements get more stringent with deterioration of the background conditions i.e. moving from scenario 1 to 3. The impact of beam-induced backgrounds on the pattern recognition performance is quantified using a reference sample of the $t\bar{t} \rightarrow 6 - jets$ at the centre of mass energy of 500

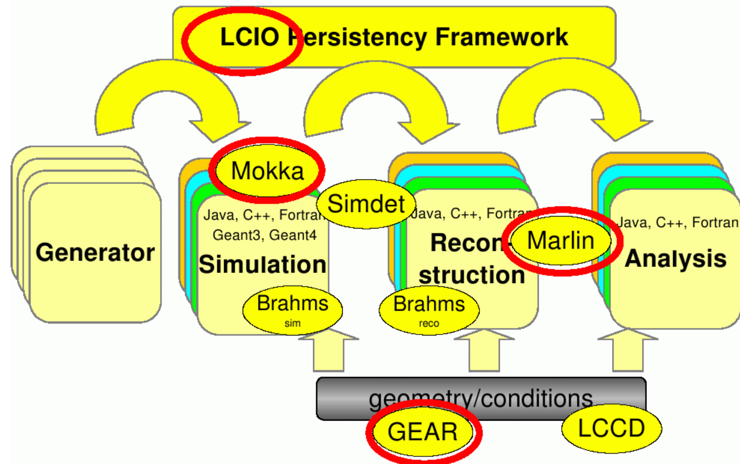

Figure 19: Organization of the simulation and reconstruction Software.

GeV. In scenarios 2 and 3, the hit patterns produced by physics events have been superimposed with the hit pattern expected from beam-induced backgrounds for a given detector integration time. Figure 22 shows the fake track rate and the track finding efficiency as a function of the transverse track momentum. Overall track finding efficiency and fake track rate for each of the three scenarios considered are presented Table 6. The study emphasizes the importance of having a device with high readout speed, which would allow to minimize effects of beam-induced background. It should be noted at this point that this is not DEPFET specific and applies to any technology employed for the ILC micro-vertex detector.

7 New Developments

7.1 PXD5 Pixel Production

A new production of DEPFET matrices, dubbed PXD5, started in 2006. After the proof of principle of the newly developed DEPFET technology and the linearly shaped compact designs in the first detector production PXD4 the first goal of PXD5 is to reproduce these features e.g. reliable transistor operation, radiation hardness, internal amplification, selective access within an array etc. In this sense PXD5 runs with an almost unchanged technology focusing on more reliable processing. While the PXD4 wafer hosts designs for Xray and vertex detectors the PXD5 batch was split into wafers containing either Xray or ILC designs both processed with almost the same technology. Thus the area of a full 150mm wafer is available for each project. For the ILC wafers a simpler and more robust backside processing was in-

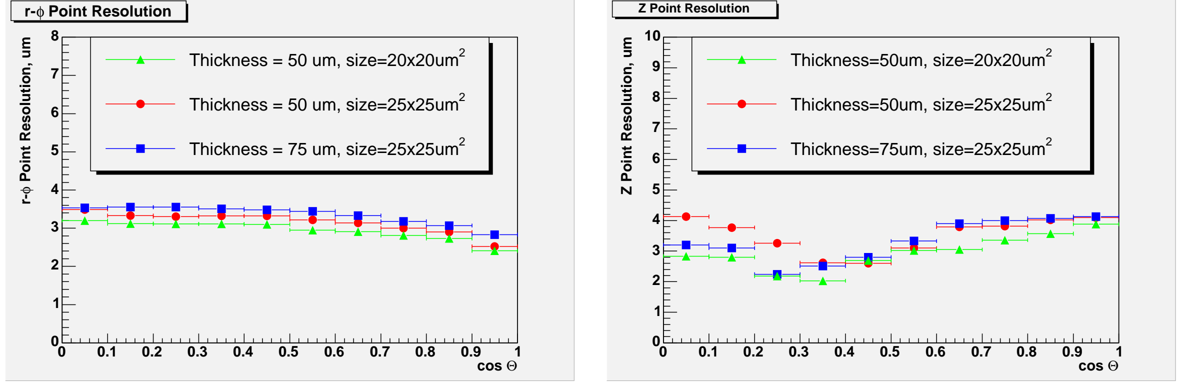

Figure 20: The spatial point resolution in $r-\phi$ (left plot) and z (right plot) as a function of particle polar angle θ.

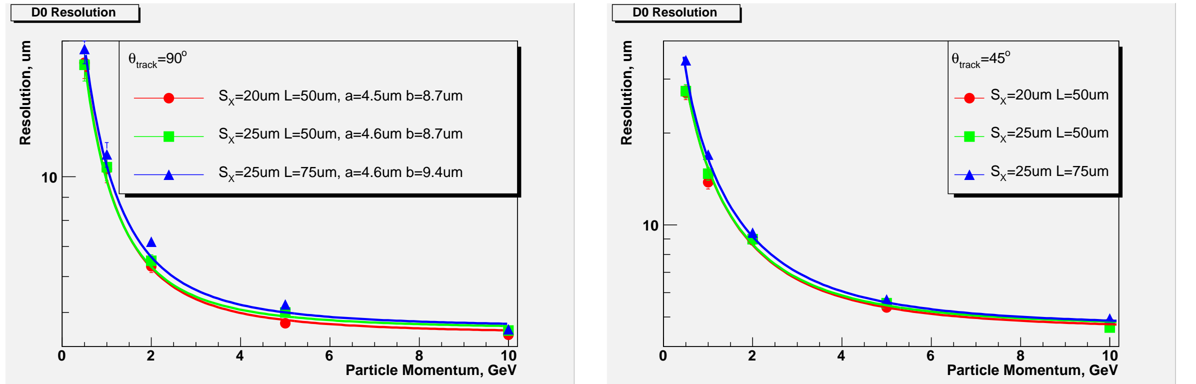

Figure 21: The $r-\phi$ impact parameter resolution as a function of particle momentum for the polar angles θ=90° (left plot) and θ=45° (right plot).

Layer	background hits per bunch crossing	Background hits Scenario 2	Background hits Scenario 3
1	400	30000	60000
2	200	30000	60000
3	100	15000	30000
4	50	7500	15000
5	20	3000	6000

Table 5: The number of background hits per bunch crossing and the total number of accumulated background hits in scenarios 2 and 3 (see text) for the nominal set of the ILC machine parameters. The beam crossing angle is 14 mrad. The ILC detector includes the integrated dipole magnet. The numbers are taken from Reference [3].

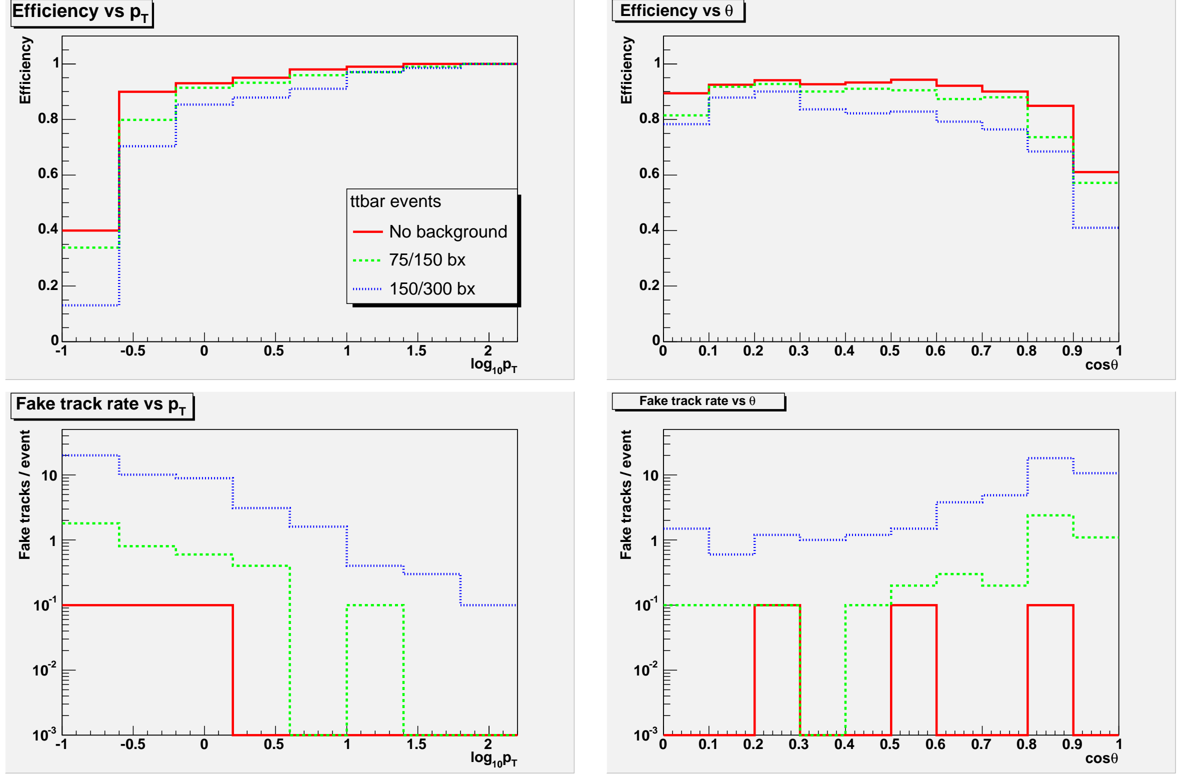

Figure 22: Track finding efficiencies (upper plots) and fake track rates as a function of track transverse momentum (left plots) and polar angle (right plots). Solid lines corresponds to a no background scenario, dashed lines to the scenario characterized by an integration time of 75(150) μs and dotted line to the scenario characterized by an integration time of 150/300 μs (see text).

Scenario	Fakes per event	Track finding efficiency, %	
		$p_T > 0.1$GeV	$p_T > 0.5$GeV
1	0.3	88	94
2	4.2	84	91
3	45	79	86

Table 6: The fake track rate and track finding efficiencies in the vertex detector for the three scenarios of beam-induced backgrounds (see text). The reference physics process used is $t\bar{t} \rightarrow 6 - jets$. In the case of scenarios 2 and 3 hit patterns produced by physics events have been overlaid with hit patterns expected from background for a given scenario.

troduced since there is no need for an 'ultra thin' entrance window as it is necessary for Xray detectors. The use of separate wafers also provides the space for yield evaluations on larger pixel arrays.

7.1.1 Array and Pixel Sizes

The large 512 × 512 matrices address already the inner layer geometry of the ILC vertex detector. Wide format detectors with 1024 readout channels × 256 switcher channels (array size = 16.38 × 12.29 mm^2) are implemented to study the influence of long access lines (Gate, Clear) on the readout speed. For the other dimension very long arrays with 256 readout channels × 1024 switcher channels (array size = 3.07 × 49.15 mm^2) are designed to measure the effect of the matrix input load on the readout chip. The pixel sizes vary from 32 ×24 μm^2 (as in PXD4), over 24×24 μm^2 (base line) to 20x20 μm^2 (technology limit). An overview is given in table 7.

7.1.2 Internal Amplification and Clear Optimization

Electrons are drained into a highly n-doped Clear contact by applying a high positive voltage. Much desired is a complete Clear (no electrons left in the internal gate) by which reset noise is totally canceled. The voltage difference between Clear high and Clear off state is limited to 10V, which is a requirement given by the new rad hard Switcher III (7.2). In principle the Clear voltage can be significantly lowered by clocking the clear gate simultaneously with clear contact. In this way the potential barrier between the clear region and the internal gate is further reduced. However, this option leads to a less compact design and even worse implies a third control line, switcher channel etc. Therefore for ILC the Clear gate is on a fixed (non clocked) potential common for the whole matrix - common Clear gate design. To find another way to facilitate the Clear process some wafers of PXD4 contained a high energy phosphorous implantation. By this means the path of the removed electrons is shifted into the depth of the bulk and the lateral fringing field gets larger. In the 'common Clear gate mode' complete Clear at voltages down to about 7V was measured on DEPFETs fabricated with this technology option (see PRC report 2005 [25]). However, the vertical position of internal gate is also deeper resulting in a 25% lower internal amplification (g_q). In PXD5 the energy of the deep phosphorous implantation is set to the same value applied for the internal gate formation thus the depth of the internal gate and hence the internal amplification remain unchanged. According to simulations the Clear efficiency will be slightly worse than that of the high energy version but significantly improved compared to the standard technology.

Using the Clear gate in a passive way is another idea to improve the Clear behavior. By increasing the coupling capacitance between the Clear contact

and the potentially floating Clear gate contact the latter one is pulled high during each Clear process. The Clear gate off potential is connected row wise via a high ohmic resistor. Various test structures and matrices are implemented on PXD5 to study the 'capacitive coupled Clear' option.

Since the main noise contribution still comes from fast readout electronics an increase of the internal DEPFET amplification g_q transforms directly into S/N. The DEPFET still offers a large scaling potential. As illustrated in Figure 23 g_q can be easily doubled by reducing the channel length from currently used 4.5 μm to 2 μm. This range will be investigated on test structures and arrays. However a reliable production of devices of short channel DEPFETS will require plasma etching techniques which have still to be installed at the HLL.

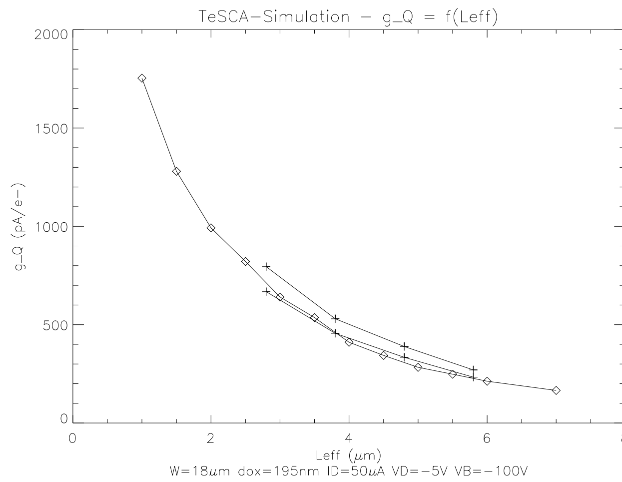

Figure 23: Dependence of the charge amplification g_q on the gate length. $\diamondsuit$: 2D TesCA simulation (50 μA drain current); + measurements with 50 μA (lower) and 100 μA (upper) drain current.

7.1.3 Charge Collection

An eventual discrepancy between g_q values measured on single DEPFETs and small arrays with a Fe^{55} source to that obtained on larger arrays in beam tests can be explained by charge losses in the latter arrays. The amplification achieved in beam test where the averaged charge is considered is by 20-30 % lower than that derived from the spectra. Results of 3D device simulations obtained in collaboration with Dr. K. Gärtner from WIAS Berlin suggest that there are charge losses in the Clear gate region due to very weak lateral drift fields near the surface. The DEPFET current response to 1600 e^- generated at different bulk positions was simulated. Slow charge collection and losses can be avoided by additional lateral drift fields and optimized doping profiles which were implemented in the PXD5 design.

type	pixels	readout channels	switcher channels	pixel size $(\mu m)^2$	array size $(mm)^2$
large matrix	512 × 512	1024	256	32 × 24	16.4 × 12.3
long matrix	128 × 2048	256	1024	24 × 24	3 × 49
standard	64 × 256	128	128	32 × 24	2.0 × 6.2
				24 × 24	1.5 × 6.2
				20 × 20	1.3 × 5.1
PXD4 standard	64 × 128	128	64	32 × 24	2.0 × 3.1
				24× 24	1.5 × 3.1

Table 7: Matrix sizes of the PXD5 production. The standard and mini matrices will exist in several design variations. For backwards compatibility standard matrices as in PXD4, compatible with the old switcher and CURO exist as well.

7.1.4 Other Features

An ILC DEPFET array will be connected to the Switcher and readout chips via bump bonds. A test array for bump bonding is included.

Most of the test matrices are designed for the new Switcher III and a 128x128 pixel layout. For backwards compatibility some smaller devices (128x64) will work with the old Switcher II chip on old hybrids.
Better testability is obtained by new biassing schemes: This saves chips allowing preselection of matrices by probing on the wafer.
Furthermore various different pixel designs have to be compared in terms of reliable operation (yield), internal amplification, clear behavior, charge collection efficiency.
PXD5 will be produced on high resistivity 6" FZ wafers of 450 μm thickness. Production should be finished in Summer 2007.

7.2 The Switcher III Chip

The Switcher II can deliver high voltages (up to 30V) at the expense of high power consumption. The HV-CMOS process used is know to be not radiation hard (Indeed, the device stops working after 30 krad). This choice was needed for the early prototype matrices when especially clear voltages needed for a complete clear were not known exactly. Now it is confirmed that maximally 10V are needed for a complete clear.
Hence a new switcher chip (Switcher III) was developed with following features:

- ▷ Switch up to 10V very fast (4ns settling time).
- ▷ Radiation hard design (0.35 μm).
- ▷ Ready for bump bonding.

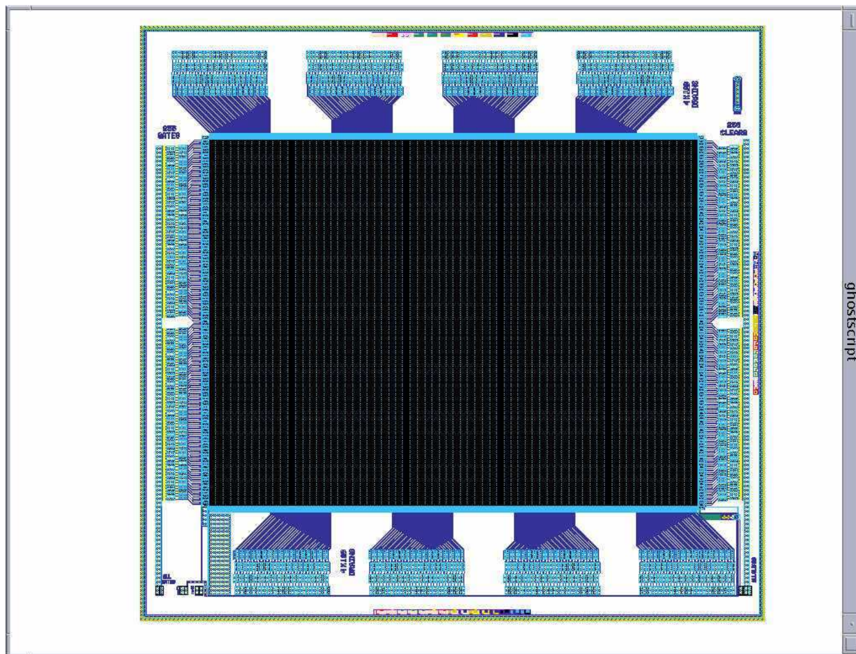

Figure 24: Large matrix with 512 × 512 pixels. The sensitive area of the array measures 16.38 × 12.29 mm^2

- ▷ 128 channels (less chips needed).
- ▷ Reduced chip area (1.24 × 5.8 mm^2)
- ▷ Reduced number of control signals.
- ▷ Flexible sequences instead of the simple row-by-row logic. This offers the possibility for an ROI readout.
- ▷ Low power consumption.

The switching voltages of 10 V is achieved by staggering 3 transistors, each switching maximally 3.3 V [23]. The chip will fit well on the reinforcement frame of the DEPFET sensor.

Test chips have been submitted and functionality and radiation hardness (up to 600 krad)has already been demonstrated [23]. A production of complete chips has been submitted.

7.3 The DCD1 Readout Chip

A new readout chip DCD1 (Drain Current Digitizer) has been developed which will overcome some shortcomings of the CURO:

- ▷ The CURO chip was designed for small matrices with low capacitance. In order to operate full size matrices the regulated cascode has to

be optimized for larger capacitances (about 40-50 pF for 5 cm long columns). From simulations a noise of 34 nA at 50pF is expected.

- ▷ An 8 bit, 16 MHz ADC will be added to each channel.
- ▷ Data is send out without 0-suppression. In test systems 0-suppression can be emulated using a FPGA. This will give a higher flexibility testing different 0-suppression and clustering algorithms. In case of very high occupancy 0-suppression is less attractive anyway.
- ▷ Power consumption should be 5 mW per channel.
- ▷ Improved timing.
- ▷ The chip will be prepared for bump bonding, wire bonding is possible using adaptor cards.

The chip will be made in a potentially rad hard UMC 0.18 μm technology and will read 144 channels. The connection to the DEPFET is done using an 18×8 array for bump bonding. The width of the chip is only 1.5 mm, much smaller than the 1.8 mm required for 144 lines of 12.5 μm pitch. Hence all chips servicing a DEPFET can be arranged in one row without staggering. A small 72 channel test chip has been submitted in March 2007.

The new ASICs require new hardware (hybrids) for building test systems which are presently being designed in Bonn. Furthermore a multichannel programmable power supply is developed simplifying considerably the setups used in the lab and test beams.

7.4 Bump Bonding Studies

For all test systems made so far the electrical connections between sensor and electronics were made by wire bonds. However, in a compact, low material ILC module the use of bump bonding is mandatory. Therefore we want to employ a bump bond technology which

- ▷ can be used for low volume production of test systems in the lab,
- ▷ is suitable for single chip bonding,
- ▷ can be extended towards industrial high volume production.

Mannheim started to study flip chip bonding with gold stud bumps connected with solder paste or conductive glue. The procedure is:

- ▷ Formation of a gold ball (free air ball) from a gold wire.
- ▷ Placement of the gold ball onto a the bondpad using ultrasonic bonding.

- ▷ The wire is ripped off.
- ▷ Glue or solder is applied.
- ▷ Flip chip bonding applying pressure and temperature.

Using a manual bonder first tests were made forming balls of 50 μm diameter from a 17.5 μm gold wire. These give studs of 60 μm diameter fitting on 80 μm bond pads. The bond pitch can be 100 μm. The yield obtained with a 64 bonds test device was 100%. The contact resistance was below 1 Ohm and a very good mechanical connection could be obtained. The next steps will be an optimization of the procedure in order to obtain lower bond forces and temperatures. The manual bonder will be modified to allow semiautomatic placement of the bumps. A test chip with 160 will be made. In order to transfer this procedure quickly to the DEPFETs the next generation of ASICS (Switcher III and DCD1) is already equipped with bump bonding pads. The PXD5 production has a number of test matrices prepared for bump bonding.

8 Summary and Outlook

We believe that most R&D goals expressed in the PRC 2005 have been met:

- ▷ The thinning technology has been demonstrated
- ▷ Single DEPFET pixels have a low intrinsic noise of 40 electrons at a bandwidth of 50 MHz.
- ▷ The radiation tolerance of the sensors up to 1 Mrad has been demonstrated. This is well above the requirement of at most 200 krad for ILC
- ▷ Prototype readout and steering chips are close to ILC specifications Improved version have been designed and submitted. These second generation chips should be sufficiently radiation hard and show significant improvements of system noise and readout speed.
- ▷ A prototype module and system demonstrator with 64 × 128 pixels including all system components has been built and has been operated successfully in a test beam.
- ▷ In the CERN test beam a five plane telescope made using DEPFET detectors was successfully operated. Preliminary results show that the error on the extrapolated position in the DUT is smaller than 0.8 μm.
- ▷ Simulation studies started and demonstrated that a DEPFET vertex detector as proposed fulfills ILC requirements.
- ▷ The technology to make low mass modules ($\approx 0.1\% X_0$) has been established.

- ▷ The estimated power consumption of a full five layer detector is low enough (6.4W) that it can be cooled by air flow. Hence the material budget can be kept very low.
- ▷ New collaborators from Aachen, Karlsruhe, Prague and Valencia have been found.
- ▷ Members of the DEPFET collaboration (Bonn, Mannheim, MPI) joined the EUDET JRA1 activity, which will provide a precision telescope for ILC detector (especially vertex detector) development. The experience from the DEPFET testbeam system is an input to the design of the EUDET system. Furthermore DEPFET matrices will be used for the evaluation of the EUDET telescope.

Simulation studies need to be continued. Especially the large fake rates at large $|z|$ need studies. Alternative geometries like forward discs instead of the long barrel geometry should be studied. The impact of a combined tracking with external tracking detectors needs to be studied, too.
Studies of EMI (electromagnetic interference) need to be done as soon as a facility becomes available.
Special effort should go in the understanding of the limitations of noise and readout speed experienced with the CURO chip. A second generation chip has been designed (DCD1) which should show significant improvements. Another strategy to decrease system noise is to increase the internal gain of the DEPFET. By minimizing the gate length the g_q can be increased. Since g_q determines the first amplification step secondary noise sources, which are dominant at present, become less important. The next pixel production has test matrices with reduced gate length and increased g_q. We are confident that we will be able to go to the next step of a system closer to ILC specs with respect to size (close to full size module), thickness and readout speed.

9 Acknowledgements

This work is supported by the German Ministerium für Bildung, Wissenschaft, Forschung und Technologie (BMBF) under contracts no. 05HS6VK1, no. 05HS6VM1 and no. 05HS6PD1,
by the Humboldt Foundation,
by the Spanish Ministry of Science and Education, project FPA2005-02935,
by the Czech Science Foundation, project Nr. 202/07/0740.
We would like to thank Devis Contarato (LBNL), Marco Battaglia (LBNL UC Berkeley) and Piero Giubilato (LBNL INFN Padova, Italy) for their help with irradiations at LBNL.

References

[1] F. Richard, J.R. Schneider, D. Trines and A. Wagner, *"TESLA : Technical Design Report"*, DESY 2001-01, ECFA 2001-209, TESLA Report 2001-023, TESLA-FEL 2001-05 (2001).

[2] G. Aarons et al., *International Linear Collider Reference Design Report*, ILC-REPORT-2007-1, DESY-07-046 (April 2007)

[3] A. Vogel, *Beam-Induced Backgrounds in the ILC Detector*, talk presented at the ECFA ILC Workshop, Valencia 09/11/2006

[4] J. Kemmer, G. Lutz, *New semiconductor detector concepts*, *Nucl. Inst. & Meth.* **A253** 356 (1987)

[5] J. Kemmer, G. Lutz et al., *Experimental confirmation of a new semiconductor detector principle*, *Nucl. Inst. & Meth.* **A288** 92 (1990)

[6] P. Klein et al., *Study of a DEPJFET pixel matrix with continuous clear mechanism, Nucl. Inst. & Meth.* **A392** 254 (1997)

[7] P. Fischer et al., *First operation of a pixel imaging matrix based on DEPFET pixels*, *Nucl. Inst. & Meth.* **A451** 651 (2000)

[8] W. Neeser et al., *The DEPFET Pixel BIOSCOPE*, *IEEE Trans. Nucl. Sci.* **47** No.3 (2000).

[9] E. Gatti, P. Rehak, *Semiconductor drift chamber - An application of a novel charge transport scheme*, *Nucl. Inst. & Meth.* **A225** 608 (1984)

[10] G. Cesura et al., *New pixel detector concepts based on junction field effect transitors on high resistivity silicon*, *Nucl. Inst. & Meth.* **A377** 521 (1996)

[11] M. Porro et al., *Spectroscopic Performances of DePMOS Detector/Amplifier Device with Respect to Different Filtering Techniques and Operating Conditions*, *IEEE Trans. Nucl. Sci.* **53** No.1 (2006).

[12] C. Sandow *et al.*, *Nucl. Inst. & Meth.* **A568** 176 (2006)

[13] J. J. Velthuis *et al.*, *Nucl. Inst. & Meth.* **A569** 57 (2006)

[14] L. Andricek *et al.*, *Nucl. Inst. & Meth.* **A565** 165 (2006)

[15] M. Trimpl *et al.*, *Nucl. Inst. & Meth.* **A560** 21 (2006)

[16] M. Trimpl, *Design of a current based readout chip and development of a DEPFET pixel prototype system for the ILC vertex detector*, PhD Thesis, University Bonn (2005)

[17] ISE TCAD Realease 7.0 V01.2b, DIOS 2001

[18] H. Gajewski et al., *TESCA - Two Dimensional Semiconductor Analysis Package*, Handbuch, WIAS, Berlin, 1997

[19] T. Behnke, S. Bertolucci, R. D. Heuer and R. Settles, *TESLA: The superconducting electron positron linear collider with an integrated X-ray laser laboratory. Technical design report. Pt. 4: A detector for TESLA'*, DESY-01-011.

[20] L. Andricek et al., *Processing of ultra-thin silicon sensors for future e^+e^- linear collider experiments*, *IEEE Trans. Nucl. Sci.* **51** No. 3, pp. 1117–1120 (2004).

[21] W. Cooper, Fermilab, private communication

[22] C. Sandow: *Ladungssammlung und Löschvorgang von DEPFET Pixelsensoren*, Diploma Thesis, Bonn University, (April 2005)

[23] P. Fischer et al., *Progress towards a large area, thin DEPFET detector module*, Presentation at the vertex 2006 conference (Perugia) by P. Fischer, submitted to NIM in December 2006

[24] P. Fischer et al.: DESY PRC report 4/2003

[25] P. Fischer et al.: DESY PRC report 4/2005

[26] J.Treis, P. Fischer, H. Krüger, L. Klingbeil, T. Lari, N. Wermes, *A modular pc based silicon microstrip beam telescope with high speed data acquisition*, *Nucl. Inst. & Meth.* **A490** 112 (2002)

[27] Mokka web page http://polywww.in2p3.fr/geant4/tesla/www/mokka/mokka.html

[28] F. Gaede, Nucl. *Nucl. Inst. & Meth.* **A559** 177 (2006)

[29] F. Gaede, T. Behnke, N. Graf, Tony Johnson, physics/0306114

[30] D. Scheirich,*Testing Semiconductor Detectors Using Beam of Charged Particles*, Bachelor Thesis, Charles University Prague, Faculty of Mathematics and Physics, Prague, 2006.