

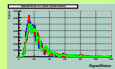


R&D on CMOS Sensors for the ILC Vertex Detector

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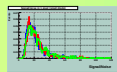
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OUTLINE

- Refining the constraints from beamstrahlung
- Progress on fast sensors adapted to the inner and outer layers
- Detector geometry optimisation
- Exploration of fabrication processes
- Issue of radiation tolerance
- Progress on thinning, cooling and mechanical support design
- Outlook
- Summary



► 1st layer: $\gtrsim 5 \text{ hits/cm}^2/\text{BX}$ (4T; 500 GeV) $\longrightarrow \lesssim 1.8 \cdot 10^{12} \text{ e}^\pm/\text{cm}^2/\text{yr}$ (safety factor: 3)

• 2nd layer: 8 times less

• 3rd layer: 25 times less

► Consequences on Occupancy in 1st layer (L0):

$\lesssim 0.9 \%$ hit occ. in $50 \mu\text{s}$ (r.o. time of TESLA TDR)

$\hookrightarrow$ signal spread on $\lesssim 4.5\text{--}9 \%$ pixels (cluster multiplicity $\sim 5\text{--}10$)

$\hookrightarrow$ 1) aim for shorter read-out time in L0 than in TDR: $\lesssim 25 \mu\text{s}$

(compromise with power dissipation, multiple scattering, ...)

2) aim for shorter read-out time in L1 than in TDR: $\sim 50 \mu\text{s}$ (vs $250 \mu\text{s}$)

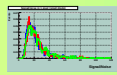
(use tracks extrapolated from L1-4 down to L0)

3) aim for relaxed read-out time in L2, L3, L4: $\lesssim 200 \mu\text{s}$ (vs $250 \mu\text{s}$)

► Consequences on Radiation Tolerance in 1st layer (L0):

• dose integrated over 3 years: $\lesssim 5.4 \cdot 10^{12} \text{ e/cm}^2 \longrightarrow \lesssim 2 \cdot 10^{11} \text{ n}_{eq}/\text{cm}^2$ (NIEL $\sim 1/30$)

$\gg$ n dose integrated over 3 years much smaller: $\longrightarrow \lesssim 3 \cdot 10^{10} \text{ n}_{eq}/\text{cm}^2$ (safety factor: 10)



► $\lesssim 25 \mu s$ in L0:

columns of 256 pixels ($20 \mu m$ pitch) $\perp$ beam axes
read out in // at ~ 10 MHz $\rightarrow$ 5 mm depth

► $\sim 50 \mu s$ in L1:

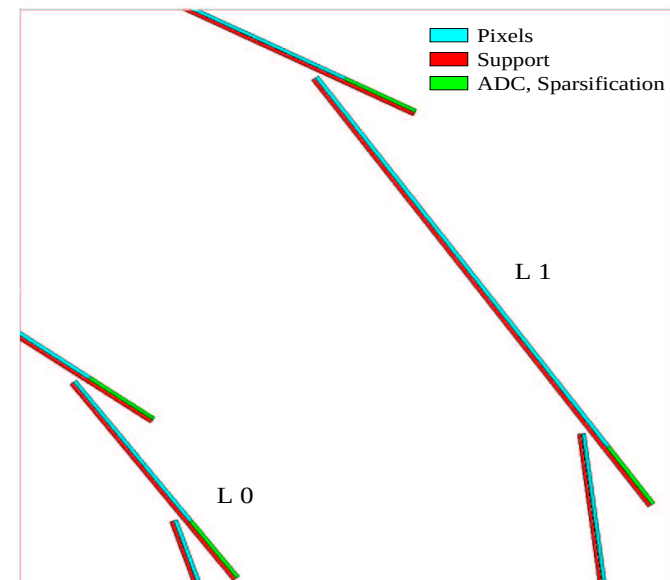
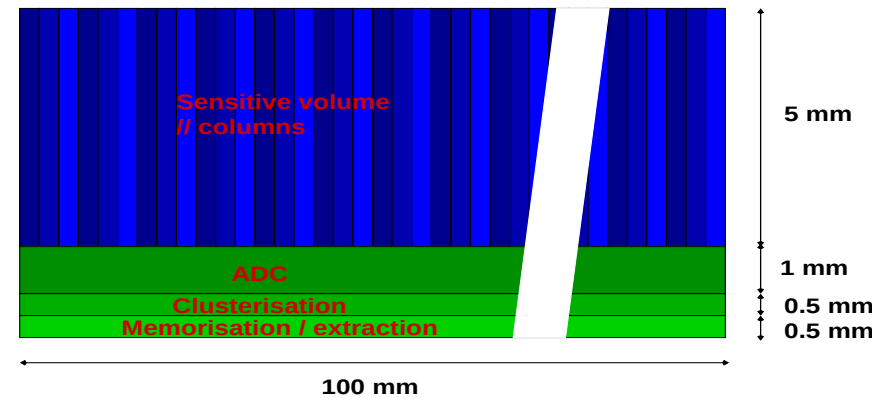
columns of 512 pixels ($25 \mu m$ pitch) $\perp$ beam axes
read out in // at ~ 10 MHz $\rightarrow$ 13 mm depth

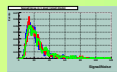
► ~ 2 mm wide side band hosting ADC, sparsification, ...

↪ effect on material budget SMALL:

b increases by $\sim 5-10 \%$

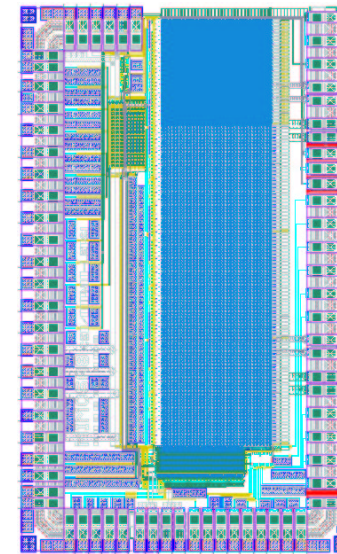
$$(\sigma_{i.p.} = a \oplus b/p \cdot \sin^{3/2} \theta)$$



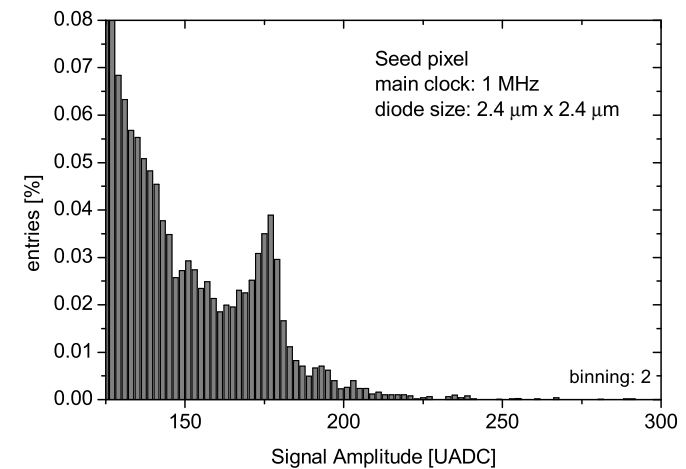


► MIMOSA-8:

- TSMC 0.25 μm digital fab. process (8 μm epitaxy)
- 32 // columns of 128 pixels (pitch: 25 μm)
- 4 sub-arrays featuring AC and DC coupled on-pixel voltage amplif.
- on-pixel CDS
- discriminator at end of each column

► tests with ^{55}Fe source:

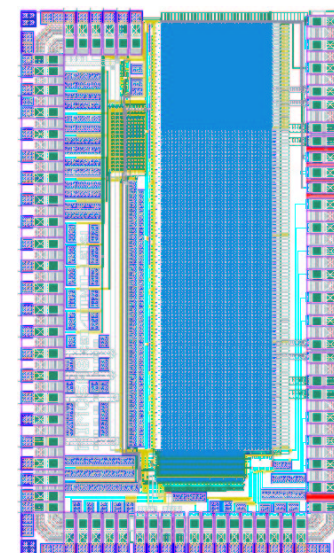
- ◇ conversion factor: 50-110 $\mu V/e^-$,
- ◇ pixel noise (including CDS): $\sim 13 - 18 e^- \text{ ENC}$!
- ◇ little pixel-to-pixel dispersion ($< 10 e^- \text{ ENC}$)!



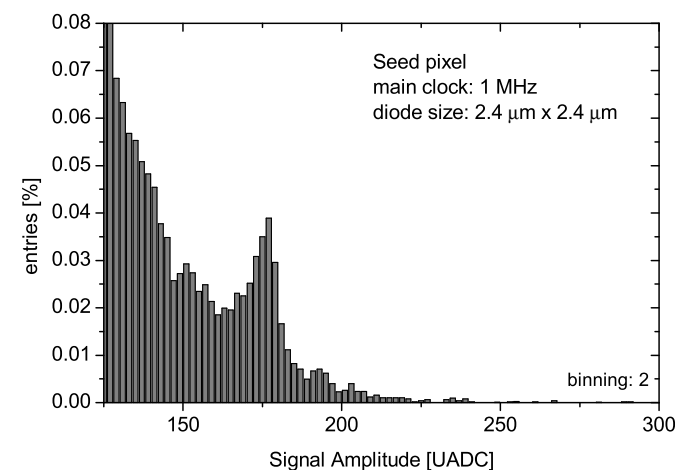


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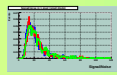
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■ Architecture seems worth extending with integrated ADC, a.s.o.

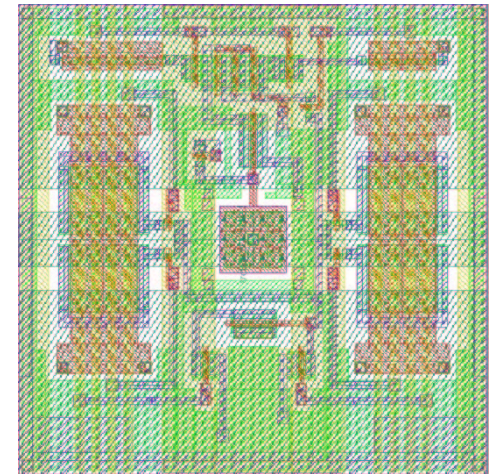


► Two phase micro-circuit architecture, reducing the data flux:

- 1) charge sampled and stored inside pixel during train crossing $\mapsto$ 5 capacitors integrated in each pixel
- 2) signal transfered and processed inbetween trains

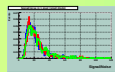
► MIMOSA-12: proto. exploring various types & dimensions of memory cells
(sent for fab. on 25 March)

- AMS-0.35 μm technology
- 4 capacitors/pixel (35 μm pitch) $\longrightarrow$
- 6 sub-arrays, exploring various MOS capacitors: 50, 100, 200 fF
- aim for minimal size capacitors providing satisfactory precision (τ),
depending on pitch, i.e. layer, ($\sim 4.6 \text{ fF}/\mu m^2$)



► MOS capacitors mandatory:

$\sim$ 4-5 smaller than poly based ones (cf MIMOSA-6)



► Geometry close to TESLA TDR: 5 cylindrical layers ($R=15 - 60$ mm), $\|\cos\theta\| \leq 0.90 - 0.96$, BUT:

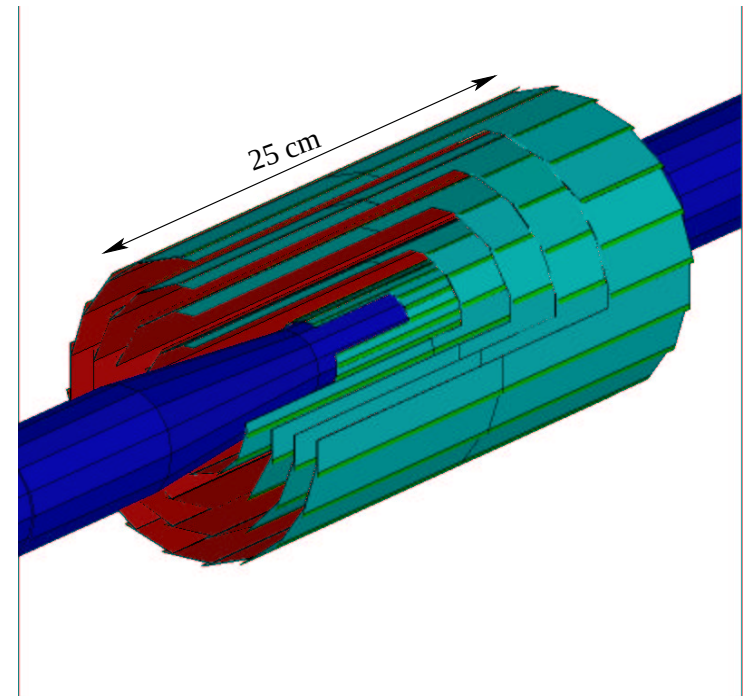
1) variable pixel pitch: $20 \mu\text{m}$ (L0) $\longrightarrow$ $40 \mu\text{m}$ (L4)

$\hookrightarrow$ reduced Nb of pixels (300 M) $\longrightarrow$ i.e. reduced data flux and power dissipated

2) shorter read-out time: $\rightarrow 25 \mu\text{s}$ in L0 (instead of $50 \mu\text{s}$) $\rightarrow 50 \mu\text{s}$ in L1 (instead of $250 \mu\text{s}$)

$\hookrightarrow$ improved capability to cope with beamstrahlung rate

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	W_{lad} (mm)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	15	20	25	7	20	25	<100	<5
L1	25	25	50	15	26	65	<130	<7
L2	37	30	<200	24	24	75	<100	<5
L3	48	35	<200	24	32	70	<110	<6
L4	60	40	<200	24	40	70	<125	<6
Total					142	305	<565	<29



► Average power dissipation $< 3 - 30$ W (depends on duty cycle: $1/200 - 1/20$)

$\hookrightarrow$ compatible with light cooling system



- 13 MIMOSA prototypes designed and fabricated since 1999, in 6 different fab. processes:

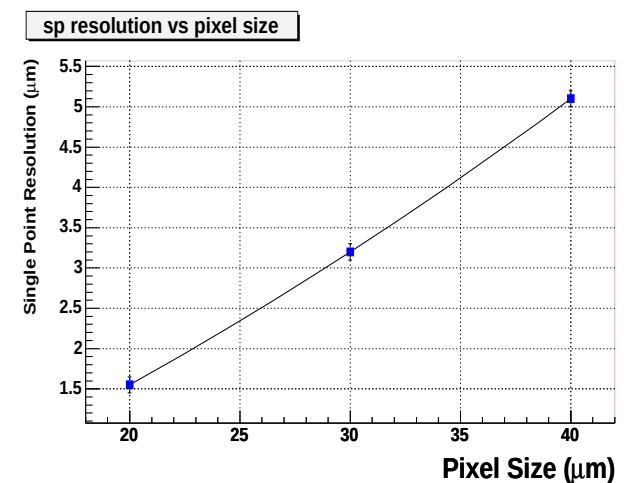
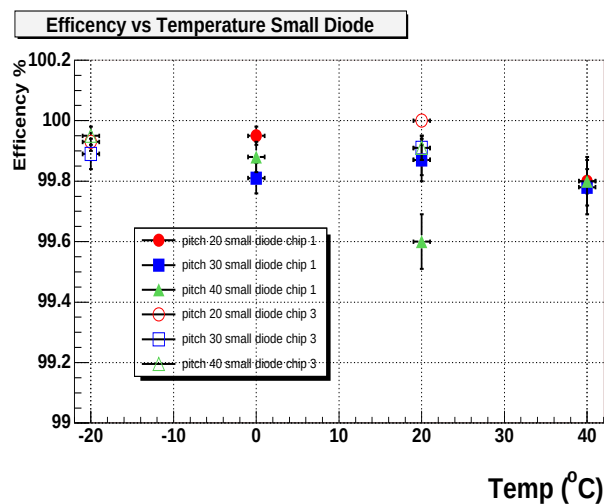
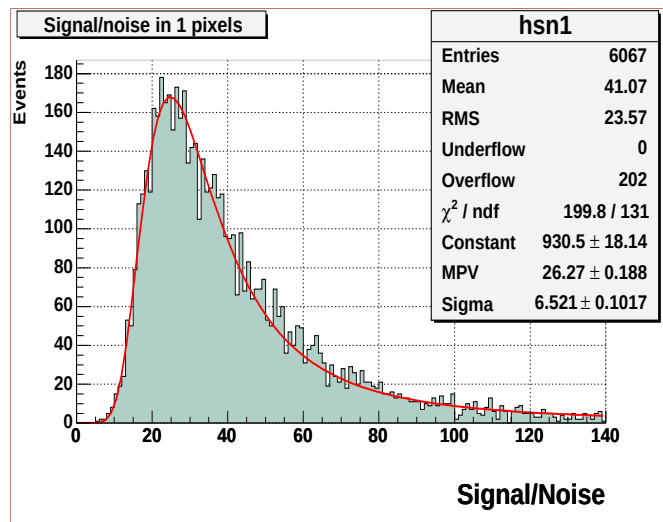
AMS-0.6 μm , AMI-0.35 μm , AMS-0.35 μm (opto & ordinary), IBM-0.25 μm , TSMC-0.25 μm

- AMS-0.35 OPTO process tested in 2004 (MIMOSA-9):

◇ pitch: 20, 30, 40 μm ◇ diode size: 3.4x4.3, 5x5, 6x6 μm^2

- Excellent m.i.p. detection performances (assessed with 120 π^- at CERN-SPS):

◇ $S/N \sim 20-30$ (MPV) $\rightarrow \epsilon_{det} \sim 99-99.9\%$ ◇ $\sigma_{sp} = 1.5 \mu m$ (20 μm pitch) $\rightarrow 5 \mu m$ (40 μm pitch)



■ AMS-0.35 μm OPTO: most attractive process tested up to now

→ baseline for further sensor R&D

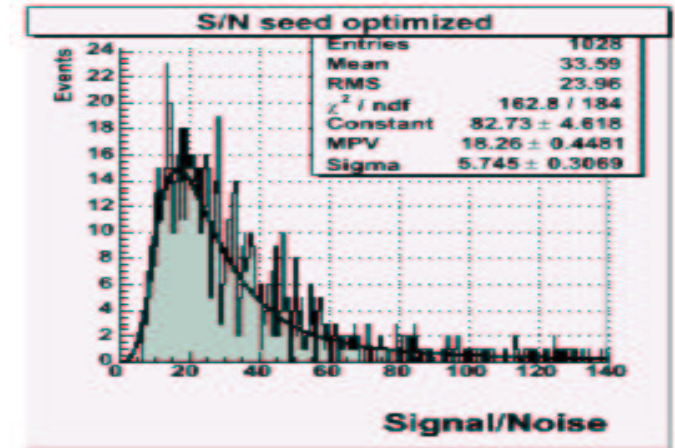


► Non-ionising radiation → requirement: $\lesssim 3 \cdot 10^{10} n_{eq}/cm^2/3 \text{ yrs}$

1) MIMOSA-9 exposed to $10^{12} n_{eq}/cm^2$ in Dubna

2) Irradiated chip tested with $\sim 6 \text{ GeV } e^-$ at DESY

→ Preliminary results: $S/N \sim 18 \rightarrow \epsilon_{det} = 99.5 \pm 0.3 \%$

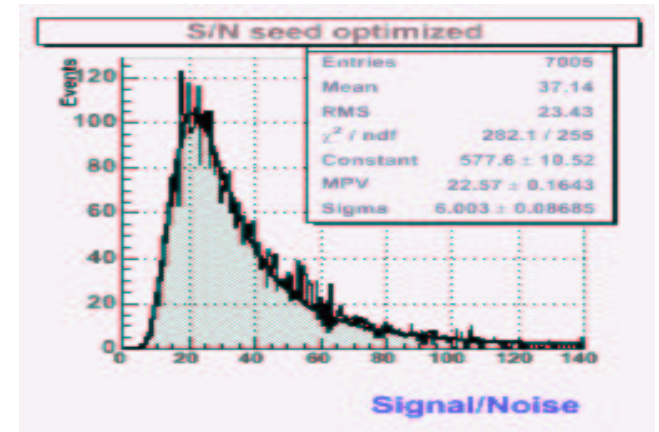


► "Ionising" radiation → requirement: $\lesssim 5.4 \cdot 10^{12} e_{10MeV})/cm^2/3 \text{ yrs}$

1) MIMOSA-9 exposed to $10^{13} e_{9.4MeV}^-/cm^2$ in Darmstadt

2) Irradiated chip tested with $\sim 6 \text{ GeV } e^-$ at DESY

→ Preliminary results: $S/N \sim 23 \rightarrow \epsilon_{det} = 99.3 \pm 0.1 \%$

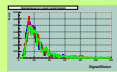


► S/N drops but detection efficiency is still very high

(before irradiation: $S/N \sim 28$ and $\epsilon_{det} = 99.93 \pm 0.03 \%$)

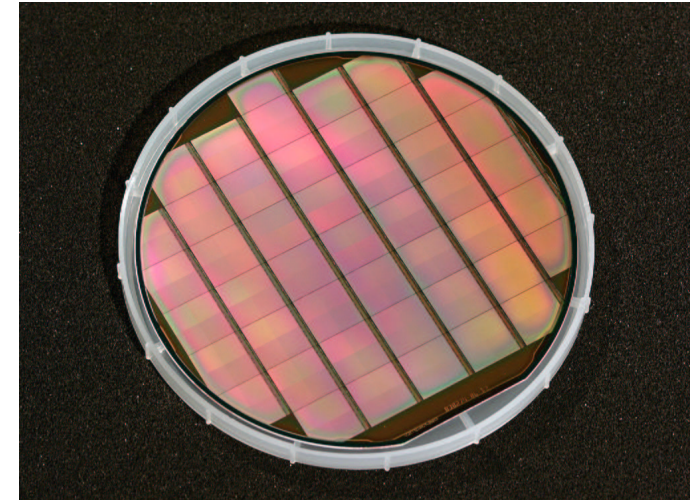
→ Sensors seem adapted to ILC irradiation doses (with safety margin !)

► Sensors should be operated at $T \lesssim -10^\circ \text{C}$ (compatible with light cooling system)



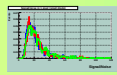
► Thinning of MIMOSA-5 sensors (3.5 cm^2) for STAR detector upgrade:

- ◇ 3 wafers thinned via LBNL to $50 \pm 5 \mu\text{m}$
- ◇ result satisfactory (after pre-dicing):
sensors don't brake or wrinkle (but are quite fragile ...)
- ◇ 3 ladder prototypes fabricated ($\gtrsim 0.25 \% X_0$)
→ up to 9 sensors mounted on ladder
- ◇ ladder tests under way (with powered sensors and signal read-out)
- ◇ studies will presumably be extended to ILC vertex detector (including cooling) via LBNL-ILC team



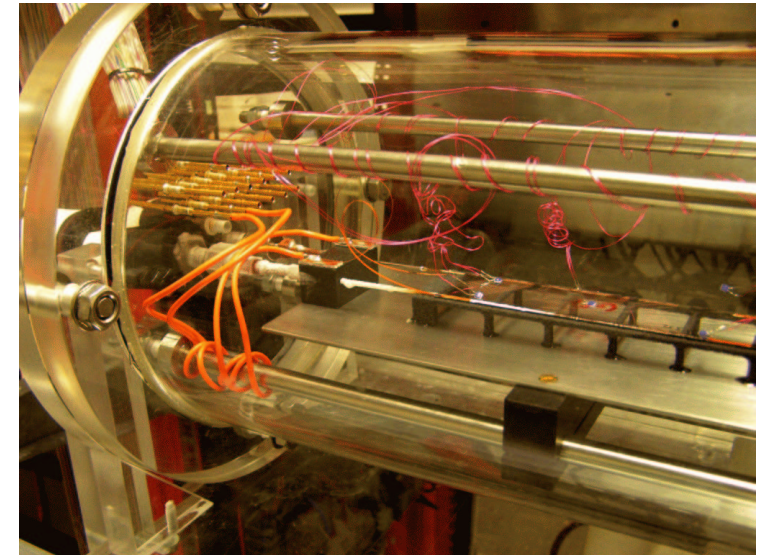
► Thinning trials in Europe:

- agreement with TRACIT (near Grenoble) to try thinning MIMOSA-5 to $50 \pm 5 \mu\text{m}$
- procedure adjustments under way: first results in May/June



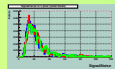
► Set-up installed at DESY for cooling and pulsed powering studies:

- ◇ cooling agent: compressed gas (ex: R134a) close to boiling point
- ◇ fluid flowing through 0.6 mm diameter pipe (0.05 mm wall)
in contact with ladder underneath the sensor 2 mm side band
- ◇ heat transfer from ladder to pipe → evaporation (T constant)
↳ gas content of fluid rises to 80–90 %
- ◇ next: cooling agent gets compressed and recirculated
- ◇ ladder simulated by glass plate (30 μm thick)
- ◇ side band power source simulated by 2 Al strips evaporated on the glass
↳ possibility to generate up to 10 W
- ◇ present status: set-up under completion (T down to -12°C already achieved)



► Cooling studies supported by finite element simulation → ladder temperature profile

► Pulsed powering tests of MIMOSA-5 under preparation



► Fast column // read-out for 2 inner layers:

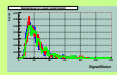
- ◇ Complete MIMOSA-8 tests by Fall 2005: full chain in lab., m.i.p. detection at DESY, rad. tol. (n, e)
- ◇ Start designing ADC → fabricate 1st test structures < end (2005)
- ◇ Next generation (with ADC) early 2006 : 2 versions (TSMC-0.25 and AMS-0.35) – tests through 2006
- ◇ Early 2007: fabricate macroscopic sensors with digital output (optimistic)
 - ↪ EQUIP EUDET TELESCOPE (1st prototype with MIMOSA-5)

► Multi memory-cells for 3 outer layers:

- ◇ MIMOSA-12 back from foundry in June → tests (lab) until Autumn '05
- ◇ Next design by end of 2005/ early 2006 → tests till Summer 2006
- ◇ First design with integrated ADC by end 2006

► Miscellaneous:

- ◇ Adapt design of micro-circuits to pulsed power operation
- ◇ Start studying sparsification algorithm and design
- ◇ Explore very deep sub-micron processes: IBM-0.13, UMC-0.18, AMS-0.18, ATMEL-0.18 (?), ...
- ◇ Investigate potential effects of beam pick-up → protections ?



► Radiation tolerance:

- ◇ Finalise analyses of MIMOSA-9 irradiated with n and e
- ◇ Assess radiation tolerance (n , e) of each new prototype
- ◇ Continue investigation of optimal operating temperature (T vs S/N and cooling/mat.budget)

► Thinning, mechanical support, cooling and pulsed power operation:

- ◇ Consolidate 50 μm thinning of MIMOSA-5 (LBNL, TRACIT, others ?)
- ◇ Try thinning MIMOSA-5 $\gtrsim 20\text{-}25 \mu m$ (2006)
- ◇ Elaborate on ladder design of LBNL/STAR $\rightarrow$ LBNL/ILC team
- ◇ Design 1st ladder prototype (DESY ?, DAPNIA ?, ... $\mapsto$ EUDET)
- ◇ Continue cooling and pulsed power studies and tests in DESY

► Other projects with part of similar requirements:

- ◇ Vertex detectors: STAR (2008), CBM, etc. ◇ (EUDET)
- ◇ Imaging: HPD-CMOS ($\lesssim$ 2007), electron microscopy ($\lesssim$ 2007)



► Work packages:

- ◇ sensor design (pixel and read-out, inner and outer layer)
- ◇ sensor performance assessment (speed, m.i.p. detection, rad.tol., thinning, power diss., etc.)
 - ↪ relies on 4–6 weeks beam tests per year (DESY, CERN)
- ◇ sensor thinning: 1) $50\ \mu m$ 2) $20\text{--}25\ \mu m$? stitching ?
- ◇ design and assessment of mechanical support: aim for $< 0.1\ \% X_0$
- ◇ design of light cooling system and certification of pulsed power operation mode

Laboratory	IReS	DAPNIA	DESY+Univ. Hb	Others
Sensor design	■	■	—	IN2P3, ...
Sensor characterisation	■	▲	▲	IN2P3, ...
Radiation Tolerance	■	▲	▲	—
Thinning	■	—	△	LBNL
Mechanical Support	—	△	▲	LBNL, (LCFI)
Cooling & pow. pulsing	▲	—	■	—

- Substantial benefit from other groups developing/integrating CMOS sensors on Vertex Detector:
LBNL for STAR and ILC, RAL, Hawaiï, BNL, INFN, ...



- ▶ Rate of e_{BS} revisited $\mapsto$ faster read-out and enhanced radiation tolerance required (w.r.t. TESLA TDR)
- ▶ Vertex Detector concept exploiting CMOS sensor advantages:
 - ◇ fast col. // r.o.: $25 \mu s$ in L0, $50 \mu s$ in L1 $\mapsto$ small mat. budget penalty: b $\nearrow$ by $\sim 5\text{--}10\%$
 - ◇ multi memory-cell pixels with delayed signal transfer and processing in L2, L3, L4
 - ▷ variable pitch: $20 \mu m$ (L0) $\mapsto$ $40 \mu m$ (L4) ▷ mean power dissipated $\lesssim 3\text{--}30 W$
- ▶ Status of sensor R&D:
 - ◇ fast col. // architecture found, with low noise & small pixel-to-pixel dispersion
 - ◇ prototype with 4 memory-cells per pixel being fabricated $\rightarrow$ explore cell precision vs size
 - ▷ tolerance to $10 \text{ MeV } e^-$ (and $1 \text{ MeV } n$) very satisfactory ▷ thinning to $50 \mu m$ seems OK



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 - ▷ tolerance to $10\text{ MeV } e^-$ (and $1\text{ MeV } n$) very satisfactory ▷ thinning to $50 \mu m$ seems OK
- ▶ Next important steps:
 - ◇ fast col. // sensor with digital output (low power, fast and compact $\sim 4\text{-bit ADC}$)
 - ◇ continue R&D on multi memory-cell sensor adapted to L2–4
 - ◇ explore fabrication processes with feature size $< 0.25 \mu m$
 - ◇ complete study of MIMOSA-5 thinning to $\sim 50 \mu m$ and try $20\text{--}25 \mu m$
 - ◇ complete cooling studies (and pulsed powering)
 - ◇ start designing/making a ladder prototype (equipped with MIMOSA-5 sensors)
- ▶ Crucial to assess sensor m.i.p. detection performances with beam tests at DESY (and CERN)