2001 - 2004 R&D on CMOS sensors for Charged Particle Tracking at a Future Linear Collider Vertex Detector

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Outline

- Principle of operation of CMOS sensors
- Performances of first CMOS sensor prototypes
- R&D motivations for a future Linear Collider
- Major steps of R&D: Sensor & System Developments
- Schedule, Task Distribution, Costs and Funding
- Summary

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Advantages of Monolithic Active Pixel Sensors:

⋆ **MAPS combine advantages of CCDs and of Hybrid Pixels:**

♡ they provide as good spatial resolution as CCDs & can be thinned down to the same level

♡ they are much more resistent to neutron radiation and are potentialy much faster than CCDs

Principle of Operation:

- ⋆ **p-type low-resistivity Si**
- ◇ signal is generated in the epitaxial layer (low doping)
- ◇ charge collected by diode
- ◇ excess carriers propagate to diode with help of reflection on boundaries with p-well and substrate (high doping)

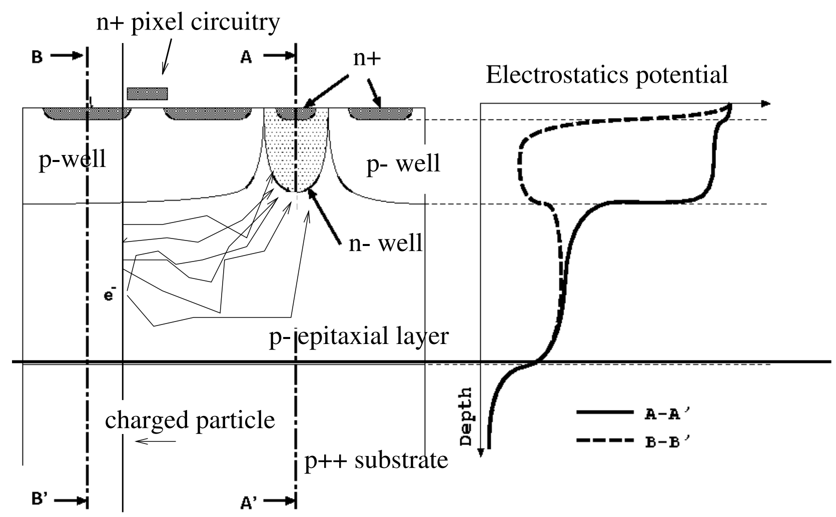

Figure 1: Schematic representation of the internal structure of a pixel designed for charged particle tracking.

Present MAPS Performances:

- **2 small proto. fabricated in 1999-2000 (0.6 and 0.35 μm techno.):**
  - ♡ 20 x 20 μm^2 pixels $\rightarrow\ \sigma_{pt}\ \sim\ 1.5\ \mu m$
  - ♡ $\epsilon_{det}\ \sim\ 99\ \%$
  - ♡ S/N up to $\sim$ 40
  - ♠ rad. tolerance up to few 100 kRad and few 10^{11} p (33 MeV/c)
- **2 small prototypes fabricated in 2001 (0.25 and 0.35 μm techno.):**
  - ♡ tests under way (prelim. result: substrate contributes to signal)
- **large prototype (ladders of 5–7 2x2 cm^2 chips) under fabrication:**
  - ◇ first experience with read-out of 1 million pixels and stitching

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Motivations for Further R&D

- **Beam backgrounds:**
  - ◇ e^+e^- pairs from beamstrahlung: 5 hits / cm^2 / BX in layer 1
    - $\Rightarrow$ 0.6/1.2 % occupancy in 100 μs at 500/800 GeV
    - $\Rightarrow$ aim for $<$ 100 μs read-out time in layer 1 ($<$ 1500 hits/cm^2)
  - ◇ neutrons: $\sim 5.10^9$ n / cm^2 / 5 yrs
  - ◇ e.m. bg: $\sim$ 100 kRad / 5 yrs
    safety factors $\Rightarrow$ 500 kRad and 5.10^{10} n/cm^2
- **Material budget:**
  - ◇ backthinning ($\leq 50\ \mu m$, handling ?)
  - ◇ mechanical support (with/without springs ?)
  - ◇ thermal control system (which temperature ?)

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R&D Plans : Sensor Developments

- **Intrinsic sensor performances:**
  - ◇ explore sensing devices → noise reduction
  - ◇ explore manufacturing processes, T dependence, role of substrate, etc.
- **Fast read-out micro-circuits with sparsification:**
  - ◇ reduce kTC and FPN (mainly pixel) noise
  - ◇ develop parallel (= fast) read-out architecture
    - → explore various architecture alternatives in parallel
- **Radiation tolerance:**
  - ◇ understand present limits ($<$ 1 MRad) → simulations
  - ◇ push rad. hardness to its best (chip design, manufact. proc., T ?)

R&D Plans : System Developments

- **DAS made of 2 steps in order to reject bg clusters:**

  1 - a) 100 μs r.o. time $\Rightarrow$ 300 MB/s – b) Integrate $\sim$ 10 frames / ms

  2 - internal tracking between trains $\rightarrow$ reject bg in layer 1

- **Backthinning:**

  $\rightarrow$ explore mechanical polishing & chemical (plasma ?) etching

- **Mechanical support:**

  $\rightarrow$ stitching & springs OR ultra-thin carbon fibers ?

- **Thermal control system:**

  $\diamond$ which T to operate sensors ? $\rightarrow$ P dissipation in fiducial vol. ?
  $\Rightarrow$ modest or substantial cooling ?

Organisational Aspects

- **Schedule until 2004 (see table 1):**
  - ◇ end-2002 / early-2003: viable solutions routhed out
  - ◇ 2004: quasi-final design of complete (optimised) ladder tested
- **Costs and Fundings (see table 2):**
  - ◇ chip manufact. and test equipmt: $\sim$ 700 keuros (preliminary)
  - ◇ funding is mainly to be found in home institutions
- **Distribution of tasks (see table 3):**
- **Test beams:**
  - ◇ chip tracking perfo.: $>$ 100 GeV/c hadrons or muons (CERN)
  - ◇ beam bg effects: GeV-like $e^{\pm}$ and sub-GeV γ (DESY ?)

Table 1: Major R&D steps until 2004

	end-2002/early-2003	2004
Intrinsic Perfo.	many new ideas tested (sensing dev., manufact.proc., T, epi-layer, etc.)	basic parameters chosen
R.O.Circuits	alternat. architectures tested (funct. at pixel/column level)	full ladder operationnal (optimal funct. repartition)
Rad. Tolerance	rad. tol. evaluated & simulated ($e^{\pm}$, γ vs n rad. disentangled, etc.)	rad. tol. improved (manuf.proc., chip design, T)
DAS circuits	1st circuit tested (speed & frame buffering)	full prototype tested (with internal tracking)
Thinning	various procedures explored (mecha., chemical, plasma)	full procedure established (mecha.+plasma+chemical ?)
Mech. & Cool.	stitching tested, prelim. VD design (chip handling, thin C fibers)	1st complete VD design (optimised for working T)

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Table 2: Fabrication & Test Equipment Costs

BUDGET ITEM	ANNUAL COST
3 – 5 small sensor prototypes	100 - 150 kUSD
large sensor prototypes	50 - 150 kUSD
data acquisition circuits	10 kEuros
mechanics and cooling	10 kEuros
thinning and radiation tolerance	10 kEuros
test equipment	50 kEuros
Total Annual Cost	$\sim$ 200 - 400 kEuros

Total over 3 Years $\sim$ 800 kEuros

Table 3: Distribution of Tasks

R&D Topic	Univ. Gene.	Univ. Glas.	IReS-LEPSI	Univ. Liver.	NIKHEF Amster.	RAL
Intrinsic Perfo.			X			X
R.O.Circuits			X			X
Chip Tests		X	X	X		X
Rad. Tolerance		X	X	X		X
DAS circuits	X					x
Thinning			x	x	X	x
Mech. & Cool.					X	

Summary

◇ **CMOS sensors offer a very promising technical solution for a vertex detector of unprecedented performances at a future Linear Collider**

◇ **Several requirements for this application are already fulfiled: detection efficiency, spatial resolution, radiation tolerance (∼)**

◇ **Until 2004, major remaining steps to prove the viability of the technique for this goal should be achieved and ultimate performances known**