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2001 - 2004 R&D Programme on Monolithic Active Pixel Sensors for Charged Particle Tracking at a Future Linear Collider Vertex Detector

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Abstract

The need of pixel arrays for the vertex detector foreseen at the future e^+e^- Linear Collider is well established, as the running conditions of the collider and its physics issues do not allow to use projective detection systems. The required vertex reconstruction performances represent a challenge for the existing technologies, which need to be pushed well beyond the limits of current devices. Monolithic Active Pixel Sensors (i.e. MAPS) have emerged recently as a possible alternative, suspected of a higher performance potential. This hope is based on the excellent detection and tracking performances demonstrated by the pioneering work done in the last two years with the first prototypes[4] of this new technology, and on the spectacular expansion of CMOS sensors for light imaging.

The objective of the coming years consists in making the necessary R&D steps to further explore and improve the sensor performances and to demonstrate that they can become the building blocks of a vertex detector at the future Linear Collider. The main issues of this R&D programme are exposed in this paper.

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1 Introduction

Vertex detectors are of growing importance in particle physics experiments as the knowledge of the event flavour is becoming an issue for several aspects of the most fundamental questions to investigate in the coming decades. The physics objectives of the future e^+e^- Linear Collider are a striking example where a very high performance vertex detector is mandatory to exploit the potential of the collider: excellent flavour tagging abilities are for instance required for precision measurements such as of the couplings of the Higgs boson(s) to the different fermion flavours, and for tagging efficiently high purity samples of new particles (e.g. expressing Supersymmetry) and of top-quark pairs.

Existing technologies (i.e. CCDs and hybrid pixels) exhibit high performances, but those needed to take full advantage of the collider potential may be too demanding for these techniques, despite the continuous improvements they both undergo: while CCDs reach the necessary granularity and introduce only little multiple scattering on the particle path, they still need a substantial improvement of the read-out speed and their tolerance to the neutron background needs to be ascertained at the required level; on the other hand, hybrid pixels are fast enough and stand much larger radiation doses, but their granularity and thickness may introduce substantial limitations in the physics reach of the experiment. Aiming for devices combining the specific advantages of each of these two technologies in a single unit is thus a natural goal, since they would fulfill the requirements imposed by most of the projects in the coming decade. This may be achieved with Monolithic Active Pixel Sensors (MAPS), which were initially intended to replace CCDs in visible imaging [1], a field where they have proven to be very successful [2].

Applied to charged particle tracking, MAPS concentrate actually the positive features of the CCDs and exhibit several additional advantages, some of them covering areas where hybrid pixels are better of than CCDs: radiation tolerance for instance, benefits from submicronic technology and from the conversion of the signal charge inside the pixel where it was created; read-out speed, on the other hand, benefits from the possibility to integrate many functionalities on the sensor substrate. Furthermore, MAPS are fabricated in a fully standard VLSI technology, which translates into modest production cost; they consume very little power as the circuitry in each pixel is only active during the read-out and as there is no clock signal driving large capacitances. Because of these characteristics, CMOS sensors are the favoured technology for demanding applications, which are typically encountered in space research. They are expected to be also well suited to the experimental conditions at the Linear Collider.

2 Achievments of Monolithic Active Pixel Sensors

2.1 origin of CMOS sensors

The development of VLSI image sensors goes back to the early '90s, where visible light imaging required simple, low-power, low-cost imaging devices [3]. The development found rapidly applications in a variety of fields, ranging from space devices, to medical imaging (e.g. dental imaging) and to consumer electronics (see [4] for a number of examples of different sensors for various applications).

These sensors are fabricated as micro-electronics circuits, most frequently in a CMOS technology. A photodiode is implemented in every pixel together with the signal conditioning electronics. In the baseline architecture, three transistors are integrated in a pixel: a reset switch (M1), the input (M2) of a source follower and a selection switch (M3).

The characteristics of CMOS sensors make them particularly attractive in visible light applications: the use of standard micro-electronics technologies translates into low cost, allows to implement very powerful functionalities (e.g. random access, analogue-to-digital conversion, signal processing), and turned finally into the concept of camera-on-a-chip. Existing devices illustrate how modest the power consumption can be: for example, a sensor made of about 4 million pixels with an on-chip 10-bit ADC dissipates only 700 mW at a read-out frequency of 240 frames per second [5].

This enormous growth of the CMOS sensors market for visible light imaging, driven by cost-effective - mainly - commercial applications, has however different requirements than particle physics. The main differences concern the radiation tolerance and the need for fast read-out and data sparsification. These parameters are usually not crucial for most visible light sensors. As a consequence, sensors available off-the-shelves are not adapted to m.i.p. tracking and a dedicated design and fabrication by a commercial company would lead to unaffordable expenses and serious difficulties in meeting the specifications.

Such considerations originated an R&D programme of MAPS for the detection of minimum ionising particles (m.i.p.) in 1999 and led to the design and fabrication of two consecutive prototypes, which allowed to test the basic detection concept. The principle of operation of these MAPS, as well as their major design features and test results are summarised in the next subsections. They show that the technology has been proven to suit minimum ionising particle detection, even if only at the microstructure level presently.

2.2 principle of operation for charged particle tracking

The principle of operation of MAPS for m.i.p. detection is illustrated on figure 1. The charge generated by the impinging particle, at a rate of about 80 electron-hole pairs per micron, is collected by a n-well/p-epi diode, created by n-well implantation into the epitaxial layer. The electrons liberated in the epitaxial layer diffuse towards the diode within a typical time of a few tens of nanoseconds. The active volume is underneath the read-out electronics, allowing 100% fill factor. Because of the difference[5] in doping levels of the p-epitaxial layer and of the p^{++} wells and substrate, potential barriers are created at the region boundaries, that act like mirrors for the excess electrons. The sensitive volume is thus the thin, partially depleted, epitaxial layer of low-resistivity silicon [6]. The charge collected by each diode is directly converted into an electronic signal at the pixel level. This is a major difference with CCDs, where the charge produced by the particle detected is clocked out through the bulk.

2.3 basic features of the first prototypes

In 1999, a first prototype, called MIMOSA-1[7], provided the first proof that MAPS can detect m.i.p. with 100 % efficiency. A second prototype (MIMOSA-2) followed in 2000, manufactured by MIETEC in a 0.35-μm process with less than 5 μm epitaxial layer thickness. MIMOSA-1 and MIMOSA-2 contain respectively four and six independent matrices of active elements having slightly different designs. Each matrix consists of 64 x 64, 20 μm wide, square pixels.

[5] typically about three orders of magnitude

[6] The underlying p^{++} substrate may also contribute to the total collected charge, as suspected from the results obtained with the first prototypes [6]. This appealing feature deserves however further studies.

[7] standing for Minimum Ionising MOS Active pixel sensor.

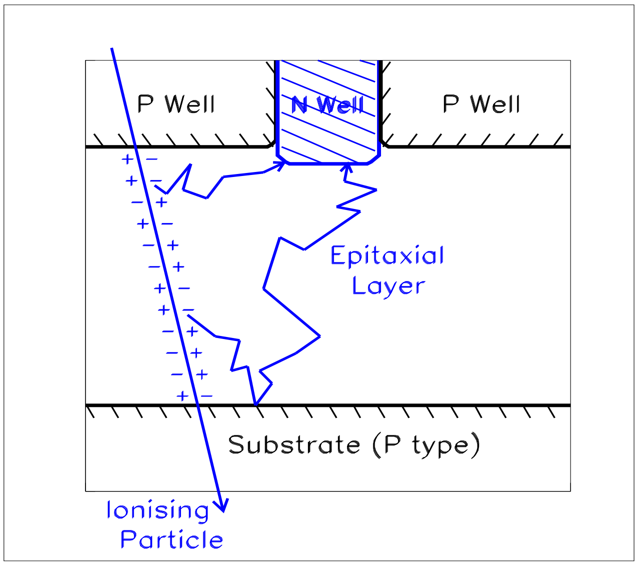

Figure 1: Schematic representation of the internal structure of a pixel designed for charged particle tracking.

Each pixel is comprised of only three MOS transistors and a floating diffusion diode, as shown on figure 2. In most of the matrices, a single diode was implemented at the center of each pixel. For one matrix of MIMOSA-1, four diodes connected in parallel were implemented in each pixel. This configuration reduces the charge dispersion and collection time at the expense of increased noise, due to the higher node capacitance and of decreased charge-to-voltage conversion gain. Several new ideas were implemented in the design of the MIMOSA-2 chip: some of the matrices were designed using radiation tolerant layout rules and the read-out frequency was increased up to 25 MHz; an option with two diodes per pixel and staggered pixels was tested as well. More details on the sensor characteristics can be found in [6].

Chips are equipped with a serial, analogue read-out, requiring only two digital signals to operate. Two 64 bit long shift registers, selecting rows and columns, are used for pixel addressing. The analogue information is read-out with consecutive clock cycles. The entire array is reset in 64 clock cycles, the reset shift register selecting an entire row at a time. This scheme was implemented for the purpose of simplicity at a stage of the development where the question of the read-out speed was not yet addressed. Its performances are therefore not representative of the MAPS potential, which will be much superior once an adapted read-out architecture is designed.

2.4 performances of the first prototypes

Basic prototype parameters, such as the total conversion gain and the pixel equivalent noise charge (ENC), were determined with a 5.9 keV X-ray source of ^{55}Fe. The charge collection time of MIMOSA-1 was measured with laser shots, and compared to the result of 3-dimensionnal simulations based on the ISE-TCAD package [7].

Both MIMOSA chips were exposed to a pion beam of 120 GeV/c at the CERN SPS, mounted on a telescope of 8 planes of high precision silicon strip detectors, which provided the impact position of the beam particles in the chip with a precision of about 1 μm.

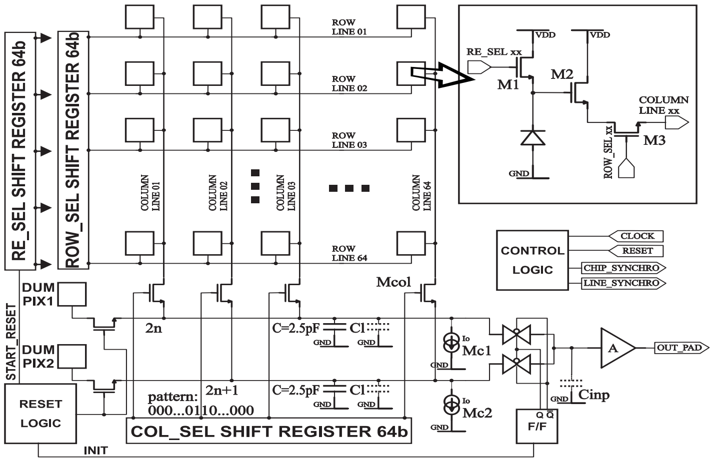

Figure 2: Basic features of the read-out electronics of the first MIMOSA prototypes.

A detailed analysis of the data collected was performed, where most of the noise was eliminated by Correlated Double Sampling (CDS). A cluster finding algorithm, using pixels with signal-to-noise ratio > 5 as a seed, reconstructed clusters matching the beam telescope prediction with an average efficiency of $\sim$ 99% for all matrices, independently of their design.

The signal-to-noise ratio (S/N) observed with MIMOSA-1 is shown on figure 3. The charge collected in each cluster was found in agreement with the simulations and was used to compute the charge center-of-gravity, which was then compared to the impact position extrapolated from the telescope. The width of the residue distribution between both impact computations was used to derive the spatial resolution of the chips. The latter ranged from 1.4 to 2.2 ± 0.1 μm, depending on the array tested. Major performances of the sensors are summarised in Table 1. More details can be found in [6].

MIMOSA prototype	fabrication process	epitaxial thickness	noise	<S/N> ratio	spatial resolution	detection efficiency
1 (1 diode)	0.6 μm	14 μm	12 e^- ENC	42	1.4 ± 0.1 μm	99.5 ± 0.2 %
1 (4 diodes)	0.6 μm	14 μm	24 e^- ENC	32	2.1 ± 0.1 μm	99.2 ± 0.2 %
2 (1 diode)	0.35 μm	4.5 μm	10 e^- ENC	22	2.2 ± 0.1 μm	98.5 ± 0.3 %

Table 1: Some main parameters and performances of MIMOSA-1 (1 and 4 diodes per pixel) and -2 (1 diode per pixel). The noise is shown after off-line CDS and pedestral subtraction.

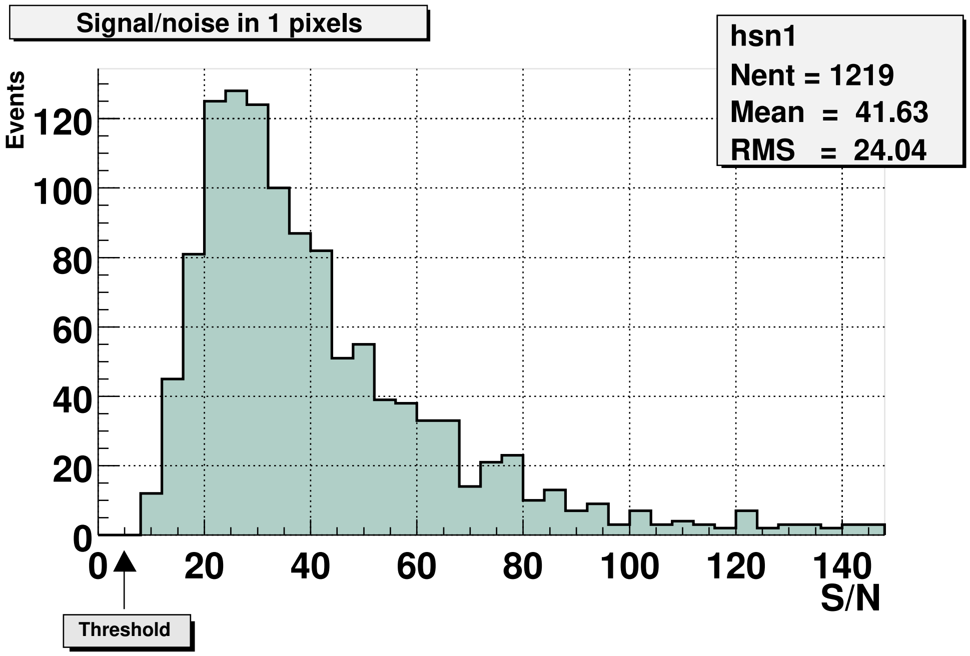

Figure 3: Distribution of the signal-to-noise ratio for MIMOSA-1. The cut applied to select pixels hit by a m.i.p. (threshold) was set at 5.

3 Motivations for the R&D programme

The proposed R&D programme aims to continue exploring the potential of the sensor technology in order to further improve its intrinsic performances, to develop a fast integrated read-out architecture including data sparsification and to design a vertex detector fulfilling the requirements exposed in the TESLA TDR [8]. The latter are summarised hereafter.

3.1 TESLA requirements

The design of the TESLA collider, based on the concept of superconducting accelerating cavities working at medium frequency (i.e. 1.3 GHz), sets experimental conditions which are rather mild in terms of duty cycle, radiation level, etc., but are nevertheless quite demanding for the vertex detector design. A duty of cycle of order 0.5% is foreseen, which is very useful for detectors being operated only during beam crossing periods. The time interval separating two consecutive bunch-crossings (BX), within a bunch train, will be close to 340 ns at a collision energy of 500 GeV and will be almost twice less once the collider is operated at 800 GeV. With increasing energy and bunch crossing rate the detector environment changes. Therefore, unless stated, all the following estimates will rely on the TESLA parameters corresponding to 500 GeV. The goal or the R&D programme is however to make the sensor performances also accommodate the more demanding running conditions expected at higher collision energies.

Detailed studies have been performed, which show that the vertex detector response will be dominated by beam background and that two-photon collisions may quite often overlap physics events. The most energetic two-photon collisions (i.e. with more than 2 GeV/c transverse momentum) are expected to be produced every 50 bunch crossings, meaning on average 6 events recorded every 100 μs.

The most disturbing background is due to e^+e^- pairs originating from beamstrahlung. It is predicted to dominate all other backgrounds and to be responsible for close to 5 tracks per cm^2 per bunch crossing for the first layer of a vertex detector at a radius of 15 mm. The occupancy generated by this background is about 0.6 % in 100 μs. Because of the strong magnetic field (4 T) in the vertex detector, most of it does not, however, reach the second vertexing layer.

The consequences on major vertex detector parameters, such as pixel size, frame read-out speed, data flow compression, material budget and radiation tolerance, are summarised hereafter.

The vertex detector design should be very similar to the one based on CCDs described in the TESLA TDR [8]. It would consist of 5 concentric layers, with radii ranging from 15 to 60 millimetres, intercepting particles produced with a polar angle such that $|cos\theta| < 0.96$ (0.90 for the two outer layers). The 4 outer layers will allow stand-alone track reconstruction, while the inner layer is essential for reconstructing track impact parameters, a crucial requirement of the TESLA vertex detector. Track reconstruction will enable internal alignment optimisation, the ability to monitor the efficiency of other tracking systems, and background rejections. Which is particularly useful in the management of the rather high occupancy expected in the first layer.

The main constrain on the pixel size originates from the capacity to resolve neighbouring tracks inside the same jet and from the reconstruction accuracy on the impact parameter. These requirements are strongest for the layer closest to the interaction point and lead to a pixel size of approximately 20 x 20 μm^2. This size is also well adapted to the width of the clusters generated by m.i.p. in the detector: the cluster multiplicity is large enough to allow particle impact reconstruction via cluster charge distribution. A typical spatial accuracy of about 2 μm, or even less, is achievable with 20 x 20 μm^2 pixels, a value well below the 5 μm required in the TDR.

Such a pixel size translates into a requirement of a total of approximately 800 million pixels for the full detector. This sets the magnitude of the frame integration time.

The latter has to be calculated with the hypothesis that individual pixels will be read serially with a typical clock cycle of 50 MHz, but also taking into account that the maximal affordable integration time will be dictated by the occupancy, which is almost entirely due to the beam background. The latter will be a potential source of hit confusion in the first layer if the integration time of the sensors is not kept short enough.

As mentioned in the next section, a typical integration time of 50-100 μs is considered as achievable for the four outer layers of the detector, and the frame read-out time may even be squeezed to 20 μs in the inner most layer.

The question arises whether this translates into an affordable occupancy due to various beam backgrounds. An occupancy of 0.6 % in the inner layer quoted earlier, which corresponds to 100 μs integration time, would be increased by an order of magnitude due to cluster multiplicity. This rate, though rather high, may still be acceptable because of the stand-alone tracking performed with the 4 outer layers. It shows however that it is desirable to keep the integration time well below 100 μs (e.g $\sim$ 20 μs), for at least in the inner most layer.

This goal would also help to keep the proportion of two-photon collision events below 6 per pixel frame read-out.

The background in the first layer will dominate the total detector signal rate and will translate into typically 1 million pixels delivering a signal per read-out frame, while the number of pixels containing physics information would seldomly exceed a typical value of 10000. The compression of the data flow is therefore a major concern.

The mechanical support and the thermal control system may introduce an amount of material which degrades significantly the detector performance. The maximum amount of radiation length one should aim for is typically 0.1 % per layer. This requires thinning the sensors to a thickness well below 100 μm, possibly down to about 50 μm. It also necessitates the design of a particularly light - but stable - mechanical support. Finally, the thermal control (or eventually cooling) system requires a thorough study, which will depend on the best operating temperature for the sensors. This relies on features (such as the S/N ratio) which are not yet fixed and need to be developed in accordance with material budget considerations.

The radiation flux has mainly two origins, which may harm the performances of a vertex detector: the electromagnetic source, which is composed of electrons and photons dominantly from beamstrahlung, and the neutron gas, due to interactions of particles in various beam elements and in the beam line surroundings. Simulations show that the vertex detector should be able to withstand an integrated electromagnetic radiation corresponding to 100 kRad in 5 years. During the same period, a fluence close to 5 10^9 neutrons per cm^2 is predicted. A safety factor of 10, a typical value for LHC issues, should be applied to these values in order to account for the limited accuracy of the simulations.

In general, one may notice that the requirements summarised reflect present points of view on the collider, and are therefore to be considered as preliminary: beam parameters and background rates may evolve, either because of more accurate background evaluations or because of a change in the collider operation. It is wise, therefore, to try to push some of the vertex parameters well beyond the level required in the TESLA TDR.

3.2 Major R&D issues

Several requirements for a vertex detector at TESLA are already fulfilled with the tested sensor prototypes. These requirements, however, still need to be ascertained with a real size detector fabricated from the prototype designs. Several other requirements are still to be met, most of which were outside of the scope of the past R&D phase, as this consisted primarily of demonstrating that the sensor technology was adequate for charged particle detection. In particular, development is required in the front-end electronics read-out speed and data sparsification, which was not a major issue for the first step of the development. The same remark applies to all system aspects.

3.2.1 Sensor developments

While the TESLA requirements directly related to the pixel size (e.g. double hit resolution power, spatial resolution) are generously fulfilled, fabricating a real size detector (e.g. 12 x 2 cm^2) is mandatory to check that the high S/N ratio and excellent detection efficiency found with the small prototypes can be reproduced with sensors of the size of vertex detector ladders. On the other hand, the established intrinsic performances of the sensor technology are likely to be subject of improvement since the technology potential is still far from being explored. Such investigations aim at, among others, reducing the electronic noise, improving the charge collection efficiency, understanding and eventually exploiting the signal production in the substrate, exploring various manufacturing processes, finding the optimal operation conditions in terms of temperature, signal-to-noise, readout speed.

These investigations will be pursued in strong connection with the successive designs of fast read-out micro-circuits incorporating sparsification. This part of the project will concentrate most of the R&D effort and will explore several possible alternative architectures. The aim will be to read-out a ladder (made of several million pixels) in less than 50-100 μs, by perhaps using the possibility of integrating various functionalities directly on the sensor substrate and subdividing the pixel array into sub-matrices read-out in parallel.

Deep sub-micron technology has been adopted for read-out electronics in the harshest radiation environments at the LHC due to its intrinsic radiation hardness. Nevertheless, this application involves exploitation of features in this technology which may not strongly influence the radiation tolerance of these micro-electronic circuits. Radiation survival of Monolithic Active Pixel sensors to the expected particle fluxes at TESLA therefore needs to be explicitly demonstrated. Preliminary results show that the radiation tolerance of the sensors already seems sufficient for the future Linear Collider, but the observed sensitivity needs to be understood and trials will be made to improve the radiation resistance well beyond the present limits.

3.2.2 System developments

The progressive definition of the read-out architecture will be propagated to the design of the data acquisition system, which will be developed and optimised in parallel. The main issue of the latter being the (potentially) large amount of data due to beam background.

Whether the ladders can be fabricated at the desired size or whether chips as large as a CMOS reticle ($\sim$ 2 x 2 cm^2) need to be assembled to form a ladder, is still an open question. At least two methods of achieving large detectors are presently used by industry, as mentionned in section 4.2. Through high precision stitching, which is now more and more often proposed by foundries, wafer size sensors are becoming a real possibility.

The thinning of sensors down to the limits set by their mechanical properties also needs to be investigated since the desired thickness (typically 50 μm) is not a straightforward operation, nor is the handling and support of very thin sensors.

The possibility to design a very light mechanical support for the vertex detector will be studied, together with the temperature monitoring system, aiming for an average thickness of less than 0.1 % radiation length per layer. This goal is easier to achieve if accurate stitching is indeed feasible. In this case, a design where the ladders are suspended with springs, as proposed for the CCD version of the detector, can be envisaged.

4 Contents of the R&D programme

This section exposes the main steps intended to follow the issues addressed in the previous section. The major concern goes to the improvement of the intrinsic detector performances and to the design of a fast read-out electronics including data sparsification. Besides these main issues, the R&D work on radiation tolerance and backthinning will carry on, and studies of the system integration will start, relying on the parameters coming out from the most advanced sensor prototype versions.

4.1 intrinsic detector performance

Despite its good performances, the sensor technology may still benefit either from improving the conventional photodiode-type design, or from investigating alternative charge collection components. A variety of such components equip light imaging devices, an application where performance improvements w.r.t. simple diode configurations were already observed. Their implantation on MAPS prototypes are also expected to translate into performance improvements. Particularly appealing are photogates [10], a current mode pixel with a photoFET element [11] and some modified versions of the n-well/p-epi diode (e.g. [12]) etc. Whilst the active element may vary, the principle of using the epitaxial layer for 100 % fill factor and a very good detection efficiency at room temperature seems essential at the current development stage. All these approaches supposed to improve the sensor performances will require extensive simulation, prototyping and test programmes.

The detailed tests of the prototypes already fabricated (see sub-section 2.3 and 2.4), for which four different CMOS processes were used, have shown that the epitaxial layer thickness should be in excess of several microns, the optimum thickness being around 10 μm in case of a 20 μm pixel pitch, with a doping level translating in the highest possible resistivity (i.e. 10 Ω·cm or more). These values account for the fraction of the total charge spread among neighbour pixels used to improve the tracking precision, as well as for the track separation capability. However, further investigation is needed before concluding on the optimum balance between the epitaxial layer thickness, the pixel pitch and the doping level as functions of the relevant signal parameters (e.g. collection efficiency, speed and spatial resolution). Moreover, the role of the substrate in the signal generation, which may be significant and depending on temperature and doping level, needs to be explored.

Each process used for prototyping the MIMOSA chips was also evaluated with respect to its genuine electronics performance. A careful noise optimisation at each step of the read-out chain translated into 6 e^- ENC for one of the prototypes. This value was obtained after off-line CDS signal processing for a 128x128 pixel array, with three MOS transistors per pixel, read-out with a clock frequency of 20 MHz. Further noise reductions are expected, for instance by decreasing the CDS processing time constant (mainly by switching to column-wise parallel read-out and including more sophisticated on-line signal processing).

The choice of the fabrication processes used for the next steps of the development requires special care: besides the performances of the technology for detector designs, the long-term accessibility of the process needs to be accounted for. Deep sub-micron technologies with minimal feature size around 0.25 μm could meet this requirement while offering great integration capability and radiation resistance, as already proven for standard CMOS electronics designed for the LHC experiments [13]. Driven by the increasingly growing market of consumer imaging for visible light, CMOS foundries offer 0.25 μm CMOS processes with low leakage current (i.e. below 0.1 nA/cm^2), thick epitaxial layer (in the order of 10 μm to provide absorption for red light), precise capacitors for mixed mode applications and up to 2 poly and 5 metal layers for compact routing.

Though not particularly needed for TESLA, attempts will be made to improve the observed radiation hardness of the sensors as much as possible. This goal will originate the design of various test structures exploring the origin of the observed radiation tolerance limits as well as the performances of potentially more resistant architectures. The development will need better understanding and extended knowledge of fabrication process details. This will propagate to the design of active element structures with reduced radiation induced leakage currents (mainly by avoiding contacts with the oxide areas in the vicinity of the charge collecting elements) and radiation harder electronics. This work will rely on the possibility to act in close collaboration with industrial technology experts.

4.2 fast read-out electronics and data sparsification

In parallel to the optimisation of the intrinsic detector performance, an important effort is needed to find an efficient solution to the problem of read-out architecture and on-chip data-processing.

Developments of CMOS sensors for visible light detection show that the different functionalities needed for the processing of the information (charge-to-voltage conversion, amplification, data reduction) can be implemented at different levels in the circuitry. Ideally, processing at the pixel level is known to give the best signal-over-noise performances and was therefore adopted by several groups working for visible light applications [14]. The aim of detecting m.i.p.s introduces one major complication due to the fact that in most of the processes available, only NMOS transistors can be integrated at the pixel level, thus reducing the flexibility of the design. Processing the data directly at the pixel level is also particularly challenging because good quality Sample-and-Hold (S/H) circuits with small capacitors are necessary and because of the restricted space available within the pixel. Various micro-circuit studies were already started in the collaboration in order to compare different sensor architectures, where functions are integrated at various physical levels of the sensor (on pixel, at the end of each column and off-chip).

The design of the sensors is complicated by the different sources of noise. They are mainly of two origins: kTC and Fixed Pattern Noise (FPN). Because of the switched-architecture, the kTC noise is of particular importance. In a baseline architecture where the reset applied biases the diode, typical input capacitances are in the order of a femto-farad, which translates into a noise value of the order of 20 - 60 e^- r.m.s. The other important source of noise (FPN) is random in space, and originates from the non-idealities of the electronic components. It can be one order of magnitude larger than kTC noise, translating into hundreds of e^- ENC. One may distinguish two origins of the FPN: the pixel level (pixel FPN) and the column circuitry (column FPN). In devices like MIMOSA, characterised by a three MOS transistor configuration combined with diode and column level amplifiers (even if reduced to simple source followers), FPN is mainly located at the pixel level. It comes from variations of the reset transistor threshold voltage, the diode dark current and the threshold voltage of the pixel source follower transistor. The column FPN results only from a dispersion of the threshold voltage of the source follower transistors or of the output offset voltage of the column amplifiers, and is therefore less important.

These noise considerations will be essential when designing the discriminators needed for sparsification, since it will be difficult to supply correct threshold levels to the chip. Solutions to this problem may be found either by setting a different discrimination level for each pixel, or by standardising the response of each channel, and reducing the kTC noise significantly before discriminating the signals.

A major parameter of the read-out architecture will be the read-out time, which needs to be as short as possible, especially in the first layer, because of the high beam background. One method to minimise integration time is to read-out sub-arrays of the detector in a column parallel fashion. In this case, the frame read-out speed is limited by the number of pixels per sub-array column, as they are most likely read serially. A typical integration time of 50-100 μs seems within reach for sub-arrays made of a few 10^5 pixels with each column being made of a few hundreds of pixels. For the specific case of the first layer, ways may be found to reduce this value to about 20 μs.

Various approaches can be considered for the organisation of the signal read-out and sparsification, based on a quite different repartition of functionalities between the pixels and the columns. The first goal is a detailed study and choice of the best suited noise reduction architecture, especially kTC and pixel-FPN, based on the two alternative schemes below:

- *In-pixel storage of the reset voltage:*

  This feature can be implemented in various ways. The simplest one consists in one additional transistor acting as a transfer gate. This transfer transistor, placed between the diode and the source follower transistor (see Fig.2), allows to store the reset level on the source follower input capacitance and the charge collected is integrated on the diode on the second switch terminal. During the read-out, each pixel is sampled twice: first with the transfer gate open to probe the reset level, second with the transfer gate closed to read-out the stored charge.

  In other schemes, on-pixel S/H circuits store the voltage after the reset as well as after the read-out trigger. The sampling switches need to be preceeded by a first stage source follower buffering a diode. During the read-out, each signal is read through the next stage source follower and each pixel is adressed twice.

  In every case mentioned above, the differential read-out of the reset and useful signal samples, provides the CDS functionnality and should allow cancellation of kTC noise and pixel-FPN. Another idea exploiting in-pixel storage capability of the reset voltage consists in realising the CDS processing directly on the pixel level by means of a switched capacitor network.

  Preliminary amplification of the signal is likely to be needed in each of these cases in order to keep the capacitor's size small enough to avoid noise degradation.

- *Alternative active resetting scheme:* Alternative active reset methods will also be investigated [15], [16], which allow a significant decrease of kTC noise levels. Since most of these techniques achieve noise reduction by bandlimiting the resetting network, special attention must be given to the time constraints when performing such a pixel reset. The goal is to reduce the kTC noise at a sub-10 e^- level, without introducing excessive degradation in FPN.

It is worth mentionning that the concern for kTC noise may find a satisfactory outcome in sensing structures intrinsically free of it. PhotoFET elements are promising candidates for this purpose. However, though the kTC noise may be eliminated with such a device, a differential read-out is still necessary for efficient FPN suppression.

The reduction of column-FPN is essential, but is likely to be of modest difficulty, since more space is available on the periphery of the sensor area to integrate different structures for local corrections. Moreover, the restriction to NMOS transistors does not apply.

The developments of light imaging CMOS sensors can be quite inspiring for solving problems appearing in the design of read-out micro-circuits of MAPS. An example is provided by a 525 x 525 pixel array designed at RAL in a 0.5-μm CMOS technology for light detection in a star tracker. This prototype implements 10-bit column-parallel analogue-to-digital conversion. The ongoing measurements of this prototype will provide useful information on issues like uniformity and column-parallel processing.

Moreover, since CCDs are also currently developed for a vertex detector at the Linear Collider, one may benefit from the common necessity to achieve column parallel read-out. Since the signal formation in both detectors presents several similarities, the data processing applied in both cases in order to get the requested data sparsification may rely on similar functionalities as well. In the CCD option, the sensors are bump bonded to a CMOS read-out circuit, running at 50 MHz. Analogue signal from the sensors are converted to a digital value, over which a threshold is applied to eliminate noise hits while preserving high efficiency for real hits. Selected pixels are used to build a cluster, with configurable size (2 x 2, 3 x 3, etc.). A further threshold is applied to the total cluster signal. After this last filter, addresses and data are stored locally, before being transferred to the outside world. This scheme, already partly experienced in previous particle physics detectors, should bring useful knowledge into the design of the MAPS read-out circuits, though most - if not all - of the functionalities of the MAPS front-end electronics will be integrated within the sensors. This feature is actually quite essential for achieving a high read-out speed: the signals can be read-out along columns parallel to the shortest dimension of a ladder (i.e. transversely to the beam lines), which allows maximal parallel data treatment. The latter may be performed with micro-circuits integrated on a narrow band of the ladder, which should be kept below 10 % of the active detector area in order to maintain its consequences on the material budget at an almost negligible level.

The basic unit in micro-electronics circuits is the reticle, whose size is about 2 * 2 cm2. In order to go towards larger sensor areas, two options are considered: "clever dicing" and "stitching". In the "clever dicing" option, sensors are designed to cover the full reticle. For a 20 μm pitch device, one of those sensors would typically have about 1 million pixels. The design of the sensors is such that minimal dead areas are kept along the side of the pixels. Typically, silicon technology requires dead areas of less than 100 μm. At the dicing operation, units of 6 or 7 reticles are kept together so to form a ladder. The mentioned dead space is perfectly tolerable in most of the cases. This technique will also not introduce any feature harming the circuitry design or any of the sensor performances. Its characteristics will be evaluated with real scale prototypes. In the "stitching" option, sensors of the required size are designed with no dead space. Given the current use of 8" (20 cm) wafers, this would allow very large area sensors to be designed. Some CMOS sensors foundries already propose this service and this route will be explored.

While designing the read-out electronics, care will be taken to keep power dissipation within a range demanding moderate cooling only. Based on current CMOS sensor performances, a total power dissipation of the order of a few tens of watts seems achievable for the full detector (i.e. $\sim$ 800 million pixels). This value accounts for the duty cycle foreseen at TESLA. Contrary to other detection techniques, for which major parts of the read-out chain are not integrated on the sensing device, the power dissipation mentioned above may cover the full read-out chain. Whether ultimate considerations will nevertheless impose extracting part of this chain outside of the fiducial volume of the detector is still subject to studies, which will benefit from the parameters of the read-out micro-circuits under development.

Finally, the question of the yield will deserve special attention. It can be estimated theoretically, in some extent, from the manufacturing parameters of the real size prototypes. The simulated yield can then be validated and eventually corrected with the results obtained from this prototype. This knowledge can then be used to improve the yield at the design stage of the next prototypes.

4.3 radiation tolerance

First results on the radiation tolerance of MAPSs look very promising, the first MIMOSA prototypes satisfying amply the requirements for the TESLA vertex detector. Irradiation with 30 MeV protons (several times more damaging in terms of non-ionising energy loss than 1 MeV neutrons) show significant changes only setting in above 10^{11}p/cm^2. Leakage current rises of about a factor of 5 and 40% loss in charge collection efficiency are seen at about 5 10^{11}p/cm^2. Studies with photon irradiation show an increase of the leakage current by more than an order of magnitude and 40% charge loss at about 600 kRad[8]. Whilst these figures represent good news, the fact that effects are seen below the levels to which LHC deep sub-micron micro-electronics show significant degradation does deserve further study. The understanding of the physics processes at the origin of the observed irradiation damages is therefore considered as necessary in order to provide final detector devices exhibiting a stable behaviour. Results obtained with light imaging devices[17] are actually very encourageing since no significant degradation of the quantum efficiency[9] is observed, even for high irradiation doses with gammas and protons. One can therefore anticipate that a careful design of the sensors could substantially enhance the overall radiation hardness.

It should be noted that the damage mechanisms for ionising particle and neutral hadron irradiation are very different. The former (at these doses) is primarily expected to influence dielectric layer and interface charge density resulting in changes in flatband voltage and increased surface currents, whilst it is the latter that primarily induces bulk damage. (Note, however, that above 200 keV electrons also start to be able to displace silicon atoms from their crystal lattice sites, but such electromagnetic induced damage always results in only point defects but not defect clusters.)

Appropriate circuit design minimises the influence of dielectric/interface charge build-up and measurements with Monolithic Active Pixel sensors taking account of standard strategies to achieve better radiation hardness do show better tolerance. The consequences of bulk damage on MAPS performances are less easy to establish. Devices have recently been exposed to a range of neutron fluences, for which results are expected shortly. Since, for this technology, the charge is not clocked out through the silicon, only effects of bulk damages on bulk leakage current, effective bulk doping and charge collection efficiency are expected to be significant. None of these are actually expected to give large effects at the doses considered, which should lead to significant advantages over vertex detector technologies for which charge transfer efficiencies pose a major obstacle.

An extensive irradiation tests programme is scheduled using neutron (poor in photon background), proton and X-ray photons fluxes as irradiation sources. Several sources have already been used (neutrons at JINR-Dubna and via CEA-Saclay, protons in Karlsruhe, X-rays at CERN) and are known to be satisfactory.

The changes of the sensor characteristics as a function of their exposure to intense ionising particle and neutron fluxes will be studied with the help of simulation programmes, such as the ISE-TCAD package.

The influence of the temperature on the radiation tolerance of the sensors will be studied, and the possibility to treat sensors degraded by extensive exposures in order to make them recover (part of) their original performances will be investigated.

4.4 data acquisition system

The data acquisition system associated to a MAPS based detector must cope with an impressive information density provided by the detector, even after zero suppression. Most of

[8]according to preliminary test results

[9]red light penetrates deeply in the substrate

this information comes in fact from converted e^+e^- pairs in the inner most layer, and is thus unlikely to be reducible before any sort of track reconstruction.

The most relevant data sources are:

- *electronics noise:* Using channel-per-channel pedestal and noise values, and applying an on-chip suppression of noisy channels and a 3 standard deviation zero suppression, one can expect a surviving fraction of noisy channels of order 10^{-4}. This leads to no more than 0.01 % occupancy and is relevant only for the otherwise quiet outer layers. Since these data concern mainly single channels, they can be further reduced by clusterisation in early stages of the data treatment (on chip);

- *converted e^+e^- pairs:* as exposed in section 3.1, typical TESLA running conditions at 500 GeV are expected to translate in a hit rate density of about 5 hits per cm^2 and per beam crossing in the inner most layer. This leads to about 1500 clusters per cm^2 in a 100 μs integration time, or eventualy only 300 clusters if one succeeds to read frames in 20 μs. Assuming an average cluster multiplicity of 10 hit channels, one expects a raw data rate of about 300 MB/s from each 0.25 Mpixel structure, i.e. from every cm^2 of the detector. Contrary to the electronics noise, most of these signals cannot be eliminated with a sparsification logic only based on their cluster singularities.

The data rate from physics event related tracks is negligible compared to the backgrounds above. For the whole detector, and assuming that 10 consecutive frames will be buffered during a bunch train crossing, this means that the DAQ has to buffer about 7 GB of data every 1 ms, dominantly from beamstrahlung pairs. Implementing a tower-like geometry of matrices may allow to substantially reduce the data rate. Simple road algorithms could pre-select clusters of interest and reject isolated background clusters. One may even envisage to implement more sophisticated local track finding techniques, like minimum spanning trees or Kalman filters, provided that sufficient buffer memory and processing power can be made available. The 200 ms separating consecutive bunch trains will be used to apply these algorithms.

If a faster integration time for the inner layer is achievable, one can envisage to identify the frame corresponding to the event and to ignore the others. One may thus reduce the occupancy and the background by a factor of about five. We rely on the progress in technology in processor and memory access speed to provide the necessary contingency required by the uncertainty inherent in current background estimations.

If no substantial background data reduction is achieved at this level, one will be forced to envisage using a parallel DAQ structure following the basis of the column wise parallelism developed for the read-out electronics. Multiple input ports would feed a buffer memory that builds a local event for each matrix.

The development of a DAQ prototype will proceed in three steps. In the first one, a test bed originally developed for the read-out of the AMS-02 detector, the CAEN S9007 (see Fig. 4), will be adapted for use as a MIMOSA read-out board. For this purpose, it will be supplemented with a front-end, adapting to the on-chip electronics of the MIMOSA prototype series. In early prototypes, where on-chip read-out logic is still reduced, the front-end will substitute missing features, e.g. digitising the analog serial signal. In a second step, the board will be upgraded to 50 MHz speed to gradually approach the required DAQ speed and study the consequences of a highly parallel approach. In a third step, in early 2003, dedicated hardware will replace the test bed for a demonstration model of the complete DAS.

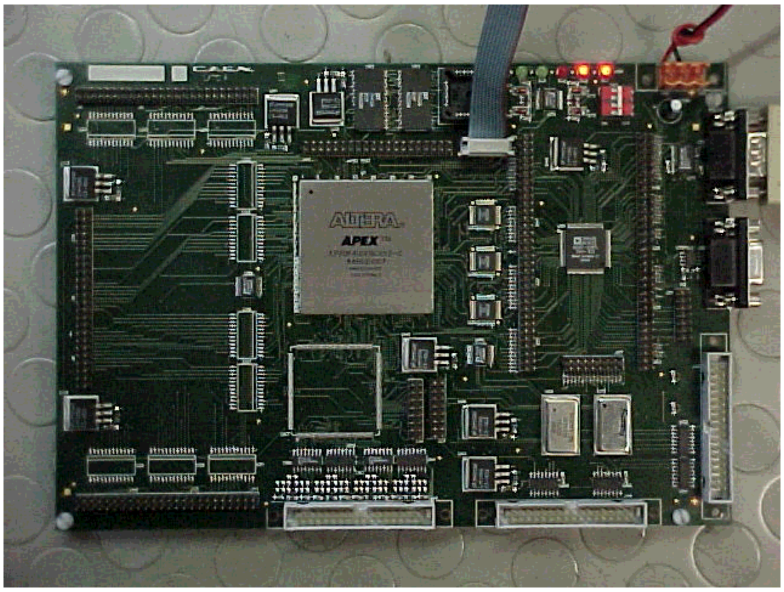

Figure 4: The CAEN S9007 digital test bed. On the left side of the board, a piggy back with a read-out front-end can be fitted to adapt to the MIMOSA read-out features and substitute functionalities missing in early prototypes.

4.5 backthinning

The physical process of charge generation and collection in MAPS being located in a very thin layer (i.e. less than 20 μm), mechanical aspects of MAPS look very similar to the CCD ones. MAPS can thus be thinned down as much as CCDs.

Two ways of thinning down the sensor arrays will be investigated: mechanical polishing and chemical etching. Whereas the former can be performed in foundries but is exposed to low yield, the second is less likely to damage the sensors but imposes to carry them to, and from, a dedicated laboratory where etching is performed.

Mechanical thinning is used both for high resistivity silicon substrates provided to make high energy physics detectors, and for processed (but undiced) wafers of deep sub-micron CMOS read-out electronics to be bump bonded together with thinned sensors to make hybrid pixel detectors for the LHC. Thicknesses down to 50 μm for 4” wafers and and 100 μm for 6” wafers can be achieved in this way with reasonable yields.

The MAPS being produced in wafers of 6” or more, further thinning may be necessary. This is typically achieved by chemical etching on the back of the substrates with litographically defined regions left at greater thickness for mechanical stability. Regions with thicknesses down to 10 μm can be achieved in this way. How far such techniques can be adapted to the processing of CMOS sensors is a matter for study, but the requirements of large area astronomy CCDs developed for operation with back illumination have led to significant experience which should be of direct relevence to the requirements discussed here. Good contacts have been established with EEV (now part of Marconi Applied Technologies) who have long experience of such applications for astronomy and space science.

The foreseen chemical etching procedure needs in particular to be adapted to the p-type of the silicon substrate. Studies were already made at the Centro Nacional de Microelectronica (i.e. CNM, Barcelona/Spain), which has long experience in this domain and is well equipped for its purpose. The study showed that the substrate can be etched at a speed of about 36 μm per hour and that the residual thickness and planeity of the sensors can be controled with an accuracy better than 1 μm via infrared interferometry. Thicknesses of $\sim$ 50 μm or less seem quite easily achievable.

Thus, provided chips as thin as $\sim$ 50 μm can be handled with enough care, the material budget of the sensors should amount to about 0.05 % radiation length per layer.

4.6 mechanical support and cooling system

Exploiting the advantage of CMOS sensors as thin as 50 μm (or less) will first require to study the actual properties of a thinned silicon chip (or ladder), the processing of the CMOS wafer making it unlikely that the sensors will keep their textbook properties. The study of sensor samples will in particular allow to determine general properties such as elasticity and expansion coefficients. Also more specific properties shall be examined, such as wafer flatness and thickness uniformity.

Experience gained with current vertex detectors shows that incorporating cooling and, even more, cabling in the design of the support structures is essential. Most detector material budgets show actually a large contribution from cables and, in a lesser extent, from cooling. With an active part of the detector as thin as 50 μm, one may fear that the contribution of cooling and cabling will be even more dominant in the global material budget than for previous detectors. Ways out of this trend have to be found.

A very positive feature of CMOS sensors is that a large amount of functionalities can be integrated on the sensor itself, without additional material due to electronic chips or PCBs. The integration of micro-circuits performing a rather sophisticated data treatment in the fiducial volume of the detector is, however, exposed to a danger: it may introduce substantial power dissipation which may, in turn, call for a quite substantial increase of the cooling system, whereas each pixel, by itself, dissipates only a few nanowatts and needs therefore no heavy cooling. This aspect of the development of the read-out micro-circuits will thus be followed closely.

Plans for the design of the support itself depend on whether a single large area sensor is used or several 2 x 2 cm^2 sensors instead. In the former case, it is tempting to suspend the ladders with springs at their ends, as proposed for the CCD option of the vertex detector. The material budget in the active area of the detector would then be governed by the sensor itself. Besides the development of the suspending procedure, one needs to investigate the performance of the sensors under tension. Alternatively, if 2 x 2 cm^2 sensors are to be assembled, a support has to be made, which competes with the thin detectors. At present, the use of carbon fibre structures is widespread, but their thickness is yet too large (in the order of several hundreds of μm), due to the use of several fiber layers. The possibility of producing single carbon fibre sheets, allowing for a stiff construction, will be investigated.

5 Schedules

The R&D programme exposed in this document will go through a couple of important steps in the coming three years, which should result, by 2004, in clear views on the feasibility and performances of a vertex detector based on CMOS sensors operated within the TESLA running conditions. Important steps towards this goal should already be achieved by the end of 2002 or early 2003. The profile of the progresses expected within the coming three years is summarised hereafter.

5.1 Sensor developments

Since various sensor architectures need to be investigated, it is considered that the most cost and time effective way of progressing in the design consists in two related, parallel sensor developments, which will eventually merge together whenever the main design issue will be cleared out. Sensors fabricated in each of the laboratories will be tested by the different members of the collaboration, ensuring a deep understanding of the properties of MAPS, as needed before the ultimate design supposed to apply to the vertex detector.

- Intrinsic detector performances (see table 2 and 3)
  - end 2002/early 2003: various signal sensing devices will have been tested, deep submicron fabrication processes will have been tried and radiation harder designs will have been tested;
  - 2004: the best combination of the different structures developed until end 2002 will have been put together and tested as part of a single large ladder optimised for all components of the detector (S/N, operating temperature, material budget, a.s.o.);
- Fast read-out electronics with data sparsification (see table 2 and 3)
  - end 2002/early 2003: various read-out architectures will be tested on small prototypes and their performances compared, part of the read-out chain will be tested on a full scale pixel array and the consequences of stitching will be known;
  - 2004: real size detector modules, including complete read-out micro-circuits, will have been fabricated in deep submicron technology and tested;
- Radiation Tolerance
  - end 2002/early 2003: the effect of ionising radiation and of neutron fluxes will have been disentangled, micro-circuits intended to provide better radiation tolerance will have been tested and different hypotheses on the origin of the MAPS sensitivity will have been studied with simulations;
  - 2004: final optimised design rules for the best radiation tolerance will be defined and applied to real size detectors.

5.2 System developments

- Data Acquisition System
  - end 2002/early 2003: a first circuit, adapted to one or several read-out schemes, will have been designed, fabricated and tested;
  - 2004: the full chain of the data acquisition system will be designed, adapted to a complete detector ladder;
- Backthinning

Fabrication date	Process	Purpose
Autumn 2001	AMS 0.6 μm real size chip	first, simple, wafer-size detector
Early 2002	0.25 μm small size chip	new process test run with structures already tested on MIMOSA 1-5
Mid 2002	0.25 μm small size chip	pixel level processing blocks (amplifiers, analogue memory cells), alternative to the standard diode signal sensing test structures, study of the active reset scheme, column level signal discriminators
Autumn 2002	0.25 μm full size chip	choice of the best suited core architecture elements, full size detector chip with simplified periphery
Early 2003	0.25 μm or 0.18 μm small size chip	test chip with implementation of peripheral processing units (column level ADCs, DACs, comparators and data compressing units)

Table 2: IReS/LEPSI sensor prototyping schedule.

Fabrication date	Process	Purpose
December 2001	0.25 μm thick epitaxy	Test sensors with different pixel structures (ampli, analogue cells, etc), on-chip CDS and column FPN reduction circuit
Mid 2002	0.25 μm thick epitaxy	Full reticle sensor, with I2C interface, control logic, fast analogue and/or digital output
Autumn 2002	0.25 μm thin or thick epitaxy	Sparsification logic read-out circuit
end 2002 or early 2003	0.25 μm	2nd set of test structures or/and 2nd iteration of full sensor, optimised for LC

Table 3: RAL sensor prototyping schedule.

- end 2002/early 2003: tests of thinning reticle sized detectors will be done, and the achievable thickness will be known;
- 2004: mechanical and chemical thinnings will have been compared and the final thinning procedure should be defined. Handling methods of the etched chips will be under study;

- Mechanical support and thermal control system
  - end 2002/early 2003: thermal dissipation details will be known, as well as various aspects related to the design of large area sensors, and a first - approximate - vertex detector design will be produced;
  - 2004: mechanical properties of the thinned chips and of the supporting structure will be tested and a complete vertex detector design will be under way.

6 Finances

This section summarises the major expenses foreseen in the coming years for manufacturing array prototypes, for data acquisition circuit and system integration prototyping, as well as for updating test equipment.

3 to 5 new (small size) chip prototypes may come out each year, testing new schemes of charge collection and read-out micro-circuit architectures. They will explore different manufacturing processes and will improve the radiation tolerance. Each of these prototypes will - in principle - be fabricated within a multiproject and cost between 20 and 40 kUSD[10], depending on the process feature size, on the manufacturer, on the sensor surface and on the total number of chips produced.

Typically every 12-18 months, a real scale prototype will be fabricated, which will allow testing the read-out of millions of pixels with their data acquisition system as well as aspects related to the design of a large area sensor. Such a large scale detector will originate an engineering run, which may cost between 50 and 150 kUSD. The average annual cost of chip fabrications should therefore lie in the range 150-300 kUSD.

The design of the data acquisition system will also require several successive circuit prototypes, which will reflect the evolution of the read-out architecture. Their cost should however be rather modest, typically of the order of 10 kEuros per year.

The equipment of the different test benches, including software, will need regular upgrades in order to adapt the system performance to the increasing size and read-out speed of the sensors. This may globally cost about 50 kEuros per year.

The design of the mechanical support and thermal control system will rely on test structures and simulation programmes, which will translate in yearly expenses of about 10 kEuros.

Other items, such as backthinning and radiation tolerance studies, have a modest impact on the global budget, and may add up to about 10 kEuros per year.

Table 4 provides an overview of the expenses introduced above. The financing of this R&D programme is not yet formally approved by any of the institutions concerned, as most of their budgets are only allocated for periods of one year. Moreover, the UK budget over these periods depends heavily on the outcomer of bids currently before the appropriate funding authorities.

[10] It is of common practice to quote prices of micro-electronics manufacturing in US dollars. Conversion in Euros is done on the basis of a conversion rate of 0.9 Euros = 1 USD.

Budget item	**cost per year**
small sensor prototypes	100 - 150 kUSD
large sensor prototypes	50 - 150 kUSD
data acquisition circuits	10 kEuros
mechanics and cooling	10 kEuros
thinning and radiation tolerance	10 kEuros
test equipment	50 kEuros
typical total annual cost	200 - 400 kEuros

Table 4: Expenses foreseen per year for each budget item.

These bids cover both equipment and some of the personnel needed to carry out several of the studies discussed here.

7 Test-beam needs

The performances of each new sensor prototype for charged particle tracking will mainly be tested with high energy particle beams, typically charged hadrons or muons of about 100 GeV/c or more. These tests necessitate several times a week of data taking per year.

It would be useful to complete these tests with exposures to particles representative of the TESLA beam background. For instance, exposing the sensors to a few GeV electrons as well as to sub-GeV photons may reveal very useful information on the sensitivity of the sensors to beamstrahlung particles expected near the TESLA interaction point.

8 Distribution of tasks

⋆ IReS and LEPSI:

The two laboratories have common experience on designing read-out micro-circuits for LHC tracking devices. Having designed the existing MAPS prototypes and assessed their adequacy for charged particle tracking, they will continue concentrating their efforts on the most fundamental aspects of the sensor development, i.e. their intrinsic performances and the read-out micro-circuits, as well as on the design of test structures supposed to exhibit improved radiation tolerance. Moreover, studies of chemical etching already under way with CNM (Barcelona), will be pursued.

⋆ RAL:

RAL has large experience in the design of radiation hard micro-electronics circuits for LHC applications as well as in the design of CMOS imaging sensors for applications as diverse as a star tracker or - since recently - a m.i.p. detector. It has also expertise in device modelling and testing as well as in backthinning. It will thus focus on the design of the sensors as well as on the data reduction chip, which might be common to the CCD read-dout system.

⋆ University of Liverpool:

Based on its experience in silicon detectors and in radiation tolerance studies for the purpose of the LHC, the team will mainly undertake detailed investigations of the radiation hardness of the sensors. It will also set up comparative tests of various MAPS designs and work on the determination of the optimal temperature to operate the sensors.

⋆ University of Glasgow

Glasgow has extensive expertise in the design, fabrication and test of radiation hard semiconductor particle detectors. It has proficiency in device modelling developed through LHC work on radiation damage in silicon and exotic X-/gamma-ray semiconductor detectors. It will work on the understanding of the charge collection mechanisms, on its improvment and identify substrate contributions. It will also collaborate closely with Liverpool on the radiation hardness issue. The laboratory will test in house and at testbeam all aspects of the MAPS devices produced by the collaboration to ascertain their suitability for the next linear collider.

⋆ University of Geneva

Based on its contributions to the AMS experiment concerning detector manufacturing, read-out and data acquisition electronics, the group will contribute mainly to the design of the DAS architecture and its implementation in hard- and software.

⋆ NIKHEF

NIKHEF was involved in several vertex detector projects in the last years. For the development of CMOS sensors towards a large scale detector, the laboratory is tackling the question of exploiting a 50 μm thin detector. It aims to investigate the properties of such a thin substrate. In parallel, solutions for thermal control and support structures will be investigated. Once a satisfactory understanding of the sensors properties, a prototype will be designed, that deals with handling, support and cooling, and aims to show the feasability of a CMOS type vertex detector.

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