SiLC: Silicon tracking for the Linear Collider

Proposal: PRC R&D -03-02

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The SiLC R&D collaboration gathers Institutions from:

ASIA:

Kyungpook National University, Taegu, Korea

Yonsei University, Seoul, Korea

Korea University, Seoul, Korea

Seoul National University, Seoul, Korea

SungKyunKwan University, Seoul, Korea

Tokyo University, Tokyo, Japan

HAMAMATSU, Japan

EUROPE:

IMB-CNM/CSIC, Barcelona, Spain

DPNC-University of Geneva, Geneva, Switzerland

University of Helsinki, Helsinki, Finland

IEKP Karlsruhe University, Karlsruhe, Germany

Moscow State University, Moscow, Russia

Obninsk State University of Atomic Energy, Obninsk, Russia

LPNHE-Universities of Paris 6&7/CNRS-IN2P3, Paris, France

Pisa-University/INFN, Pisa, Italy

Charles University in Prague, Prague, Czech Republic

University of Roma 1, La Sapienza, Rome, Italy

Instituto de Fisica de Cantabria (CSIC-Cantabria University), Santander, Spain

University of Torino, Torino, Italy

IHEP-Austria Academy of Science, Vienna, Austria

USA :

Department for Physics, University of Michigan, Ann Arbor, USA

Institute for Particle Physics and the University of California of Santa Cruz, Santa Cruz, USA.

(See next page the authors list)

Department for Physics, University of Michigan, Ann Arbor, USA.
T. Blass, S. Nyberg, K. Riles, H.J. Yang,

Centro Nacional de Microelectronica, IMB-CNM/CSIC, Barcelona, Spain
F. Campabadal, C. Fleta, M. Lozano, G. Pellegrini, J.M. Rafi, M. Ullan

Departement de Physique Nucleaire et Corpusculaire, Universite de Geneve, Geneva, Switzerland
M. Pohl, X. Wu

Department of Physical Sciences, University of Helsinki and Helsinki Institute of Physics, Helsinki, Finland
J. Kalliopuska, R. Lauhacangas, K. Oesterberg, R. Orava, N. Van Remortel.

Institut fur Experimentelle Kernphysik, Karlsruhe University, Germany
W. de Boer, A. Furgeri, F. Hartmann, Th. Muller

Moscow State University, Moscow, Russia
D. Karmanov, M. Merkin, S. Voronin

The Group of Korean Institutes that gathers:
Department of Physics, Kyungpook National University, Taegu, Korea
Department of Physics, Yonsei University, Seoul, Korea
Department of Physics, Korea University, Seoul, Korea
Department of Physics, Seoul National University, Seoul, Korea
Department of Physics, SungKyunKwan University, Seoul, Korea
B.G. Chean, Y.I. Choi, J.H. Kang, J.S. Kang, H.J. Kim, S.K. Kim, Y.J. Kwon, J. Lee, H. Park

Obninsk State University of Atomic Energy, department of Applied Mathematics, Obninsk, Russia
I. Bagdasarova, V. Galkin, D. Rizhikov, V. Saveliev, M. Zaboudko,

Laboratoire de Physique Nucleaire et des Hautes Energies, Universites Paris 6 et 7/CNRS-IN2P3, France
J. E. Augustin, M. Baubillier, M. Berggren, N. Bleurvacq, Cl. Chapron, G. Daubard, Ch.Evrard, J.F. Genat, T. Ph. Hung, D. Imbault, F. Kapusta, H. Lebbolo, F. Rossel, A. Savoy-Navarro, D. Vincent.

University of Pisa/INFN, Pisa, Italy
F. Bedeschi

Charles University in Prague, Prague, Czech Republic
Z. Dolezal, P. Kodys, P. Kubik, P. Reznicek

Universita di Roma 1, La Sapienza, Rome, Italy
C. Dionisi, S. Giagu, C. Luci, M. Rescigno, L. Zanello

Santa Cruz Institute for Particle Physics and the University of California at Santa Cruz, USA
C. Flatto, A. Grillo, J. Kroseberg, G. Nesom, H. Sadrozinski, B. Schumm, A. Seiden, N. Spencer, L. Winstrom, M. Young.

Instituto de Fisica de Cantabria (CSIC-Cantabria University), Santander, Spain
C. Martinez Rivero, A. Ruiz, I. Vila

Department of Physics, University of Tokyo, Tokyo, Japan
H. Aihara, M. Iwasaki

University of Torino, Torino, Italy
F. Bianchi, L. Demaria, D. Gamba

Institut of High Energy Physics, Austrian Academy of Science, Vienna, Austria
Th. Bergauer, M. Friedl, M. Krammer, M. Pernicka

HAMAMATSU

The SiLC collaboration is also in close contact with:

Fermi National Laboratory, USA[1]*:*
B. Cooper, M. Demarteau, J. Krempetz, H. Weerts

Stanford Linear Accelerator Laboratory, USA[2]*:*
T. Barklow, M. Breidenbach, N. Graf, J. Jaros, T. Nelson,

SiLC: Silicon tracking for the Linear Collider

The SiLC R&D collaboration was launched 3 years ago and presented a proposal to the PRC in May 2003.

Its aim is to develop the next generation of large area Silicon trackers especially suited for performing very high precision measurements in spatial position and momentum at the ILC machine.

This international collaboration is addressing all the needed R&D aspects, namely on:

- Sensors
- F.E. and readout Electronics
- Mechanics

As well as on developing the needed tools:

- Simulations
- Lab test benches and test beams
- Alignment and calibration

Important progress have been achieved these last two years, on all these various aspects and are reported here. Among the main highlights:

- Characterization of long strips and development of fab line for producing new Si detectors
- Newly developed F.E. chip in deep sub micron (dsm)
- Developed expertise in setting up the Lab test benches and in achieving the precise requested test measurements (characterization of sensors and electronics)
- Full detailed design of the various components of complete Si tracking systems and their implementation in the geometry DB for GEANT 4 based detailed simulations.
- Thermo mechanical studies
- Development of an extremely precise alignment system based on interferometry

The SiLC collaboration is preparing for an important test beam on Fall 2006.

1. Introduction

Since the SiLC R&D proposal [3] was submitted at the PRC-DESY in May 2003, there has been an important evolution in the development of the detector concepts for the ILC partly due to the choice of the machine technology in 2004. Three detector concepts are currently considered: GLD, LDC and SiD. In all three detectors concept the Silicon tracking is a crucial component of the tracking system. This is of course clear in the case of SiD where the overall tracking system is based only on Silicon strip technology. It is now indeed also the case in the so called large detector concepts, GLD and LDC, where Silicon tracking plays a complementary and essential role with respect to the central TPC tracker. Within this R&D collaboration people have developed the concept of a Silicon Envelope [4] surrounding the TPC in the case of LDC (previously called TESLA detector). The importance of this ensemble of tracking devices surrounding the TPC has become now clear and will be discussed in this status report[5]. This is certainly an important achievement of this collaboration.

However as stated since the beginning, this collaboration is considering both cases: a whole Silicon tracking system as preferred by SiD concept or a set of Silicon detectors surrounding the TPC as in the case of LDC. Indeed the R&D issues are quite similar for both cases. This makes also this R&D a unique place to study and compare these detectors concepts at least for what concerns the tracking system [6]. And after all one should notice that the main if not only difference between the detector concepts is the tracking system.

In the last two years, the SiLC collaboration has made impressive progress in most of the R&D fronts that were addressed in the proposal. This status report is going to summarize the main achievements on the R&D on: the sensors, the front-end and the readout electronics, the mechanics as well as the developments of the needed tools to achieve these results. These tools include: the development of Lab test benches dedicated to the study of performances of the sensors, of the detector basic prototype, and of the FE electronics; the construction of prototypes for various needed studies, as for instance, the cooling studies; the development of the simulation packages; the development of the calibration and of the alignment procedures; the preparation of the test beams.

There will be a section devoted to the main aims pursued by this R&D for the future, and the foreseen distribution of related tasks.

This report will be completed by a brief discussion on the expected evolution of the collaboration, on the actual financial support and on the future needs.

2. R&D GOALS:

The SiLC collaboration is aiming to develop the next generation of large Si-tracking systems able to work at the future ILC machine.

This is undergoing by pursuing the advances achieved in this R&D field especially by the R&D's for the Si trackers for the LHC experiments, also taking into account the progress made for constructing the Si devices for the Tevatron and for the embarked experiments: AMS and GLAST.

The goals are to build a tracking system able to perform momentum and spatial position measurements with very high precision, ensuring at the same time a low material budget, robustness, easiness to build and to work with, and low cost.

To achieve these challenging goals, an active R&D is conducted within the SiLC collaboration on sensors, electronics and Mechanics. The present status of these R&D aspects is reviewed here below.

3. R&D on sensors:

2.1 ***Baseline technology and achieved results***

The baseline technology is micro-strips sensors. The Silicon drift sensors initially proposed for some parts of the tracking system are not considered anymore. The length of the strips will be determined by the compromise between the availability on the market of larger wafers (at least 8 inches), the easiness to build longer strips by bonding several sensors together and by the occupancy constraint.

Current results from the Paris test bench on the response of the Silicon strips with respect to their length, especially S/N will be discussed here.

A photograph of the first prototype is shown here below (Fig. 1). The design of this prototype allows for microstrips of various lengths thanks to a serpentine output scheme to the readout.

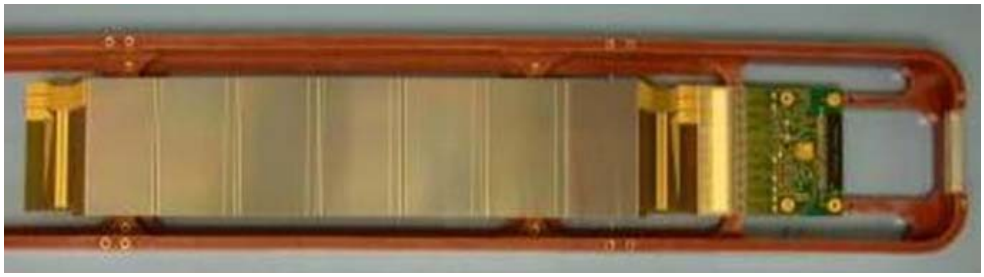


Fig 1: Prototype with microstrips of 28cm, 56cm, 112 cm and 224 cm length read out by VA64_hdr chips. This variable lengths prototype was built by Geneva University team using the AMS technique to build ladders made of several sensors (here 7) bonded together to form long strips.

The test set-up uses both LD 1060 nm laser diode and a Sr90 radioactive source to excite the Si substrate. This test set-up is described in section 5.2. Here we are summarizing the measurements and results actually achieved and the future foreseen tests.

A very detailed scan is performed automatically on the test bench thanks to the 3D motorized table that allows to scan the detector with a precision of 5 µ and to position the collimated laser diode with the same precision with respect to the surface of the sensor. Figure 2 shows the result of this scan and demonstrates that the pulse height measurements are extremely sensitive to a very accurate positioning of the IR light source.

Another measurement performed with the LD 1060 nm source consists in measuring the signal along the microstrips of different lengths. Figure 3 shows the results of these measurements when performed on strips of different lengths, i.e. 28, 56, 112 and 224 cm. It is striking to see that the response is similar, within 10%, for all the strips lengths but for the longest one. Indeed what is interesting to note is that the VA64_hdr front end chip has a shaping time of 3.7 µsec. Thus even for 112 cm long strips, this shaping time seems sufficient and it becomes only too tight for the 224 cm long strips.

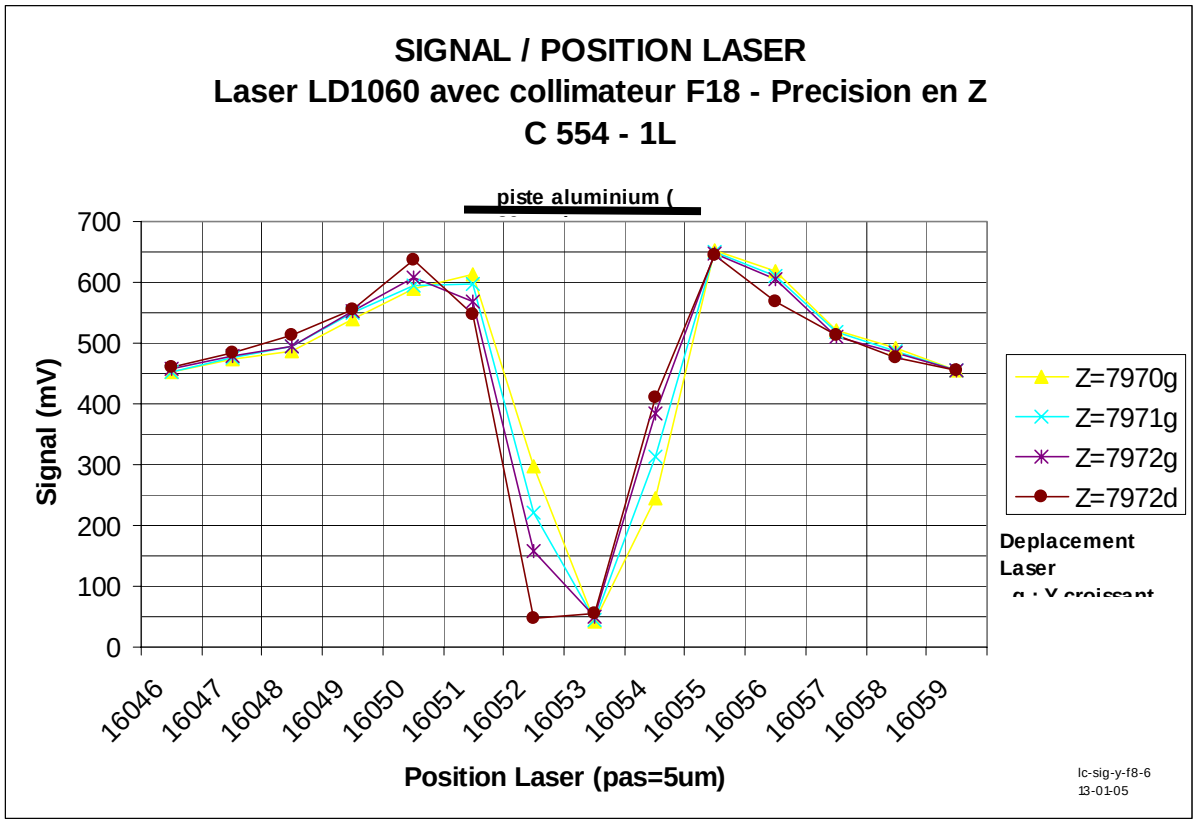


Fig 2: Automatic scan of the surface of the Silicon sensor by step of 5µ. One sees the very fine structure and the extreme sensitivity to a perfect collimation and positioning of the source.

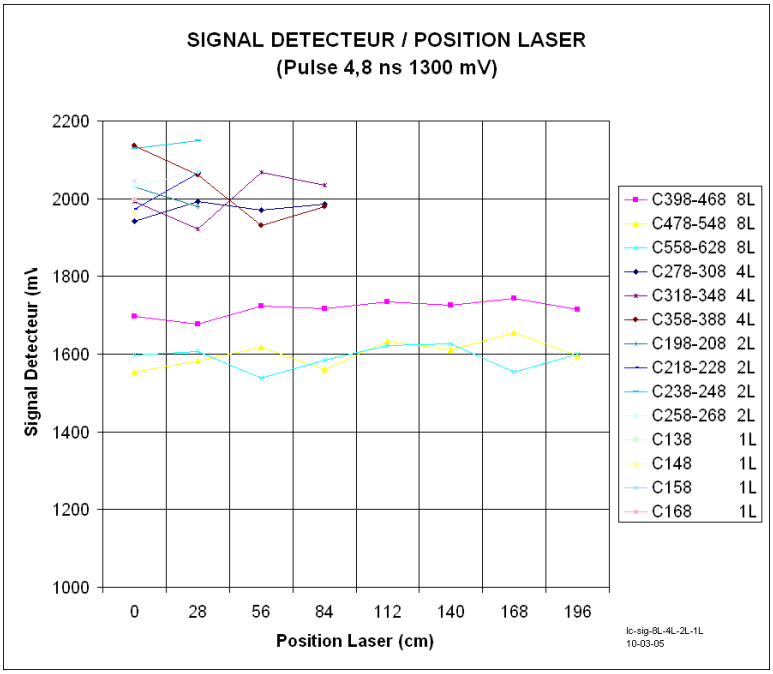


Fig 3: Measurement of the signal as a function of the position of the laser along the strips of variable lengths (N x L = N x 28 cm, with N = 1,2,4 and 8).

With the same set-up but using a radioactive Sr90 source to stimulate the Si substrate, a preliminary measurement of the signal over noise ratio (S/N) was performed and compared with the theoretical calculated curve. The Figure 4 shows the comparison between the theoretical curve and the measurement performed on three different strip lengths, namely: 28, 112 and 224 cm. As an indication, it gives that within the present set-up conditions, i.e. a readout based on theVA64_hdr F.E. chip with a shaping time of 3.7 µs, the S/N ratio for a 60 cm long strip is of the order of 20 ± 5. More work is undergoing these next weeks to improve these measurements. The LPNHE and Prague teams will jointly perform new measurements and cross-check the ones just reported here.

For completeness, the theoretical S/N ratio was calculated by computing the electron equivalent noise, ENC_{ladder} , as the quadratic sum of ENC_{VA} (intrinsic noise of the VA circuit), ENC_{leak} (leakage current noise), ENC_{res} (noise due to the polarization resistors), and ENC_{ms} (noise due to the metal strips). For a ladder with 28 cm long strips, ENC_{ladder} was found to be equal to 671 e-.

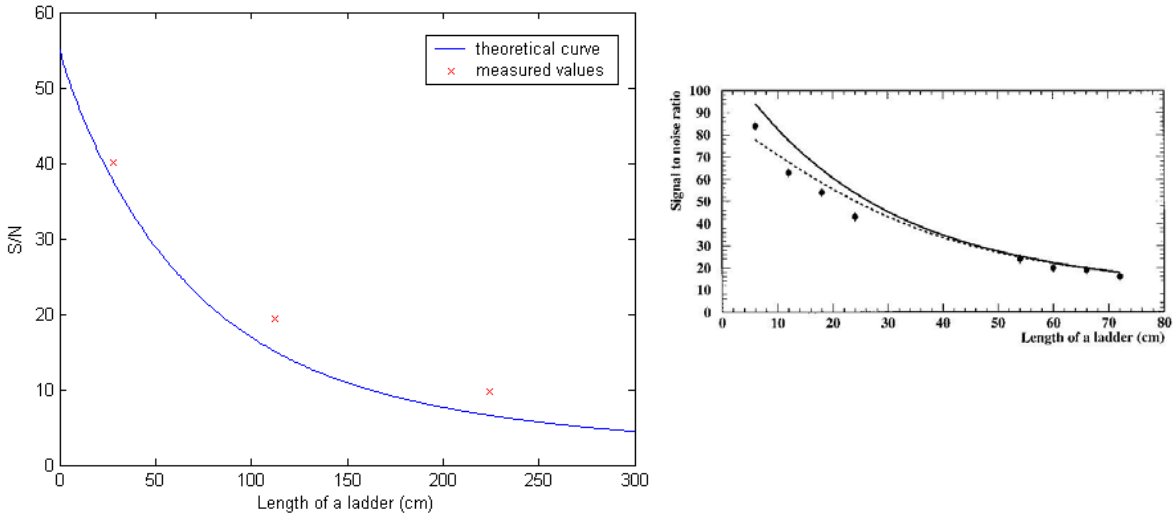


Fig 4: On the left, results on very preliminary measurements of the signal/noise ratio (S/N) for strips of variable lengths, irradiated by Sr90 radioactive source and read out by VA64_hdr FE chip with a shaping time of 3,6 µs. These results are compared with the theoretical calculated curve (full blue line) and with measurements from NOMAD (plots and results on the right)

It is interesting to note that the preliminary measurements reported in Figure 4 (plots on the left) are in rather good agreement with the ones obtained for the microvertex of the NOMAD experiment (NIM A 413 (1998), 17-30), see plots on the right. Indeed the sensors equipping the NOMAD device are the same as the ones equipping our prototype, and their device was read out by VA1 chips.

2.2 ***Sensors characterization***:

The sensors for future high-energy experiments will have many strips to achieve a high spatial resolution. An automated test system for those sensors is necessary if the measurement of the electrical parameters of each strip is required.

Sensor characterization set ups have been developed in some Laboratories in charge of the quality control of the sensors delivered by the Industrial firms, for the LHC experiments. This is a major task that allows first to decide if the produced sensors are satisfying the required specifications and to ensure later on the follow-up of the production to reject the sensors if they do not satisfy strict quality requirements, before mounting them on the detector.

Such facilities exist in the SiLC collaboration both at Vienna and Karlsruhe and were set up for the quality control of the sensors for the CMS experiment. They are described here below, and will be of great use for this R&D.

Note that other Institutes in the collaboration have same type of facilities (ex: Korean Institutes and Pisa).

2.2.1. Mechanical Setup

At the Institute for High Energy Physics (HEPHY) of the Austrian Academy of Sciences, the mechanical set-up of the sensor characterisation system consists of a vacuum support carrying the sensor. This support is moved by a motorised-XYZ-table together with the micropositioner holding a needle in permanent contact with the detector's bias line. This arrangement allows the spatial movement of the sensor while the bias voltage is always applied. For the bias ring contact it would be sufficient to use only one needle, but as little shocks are unavoidable due to the movement one probe occasionally loses contact. Using two probes in parallel has solved this problem.
Two additional micropositioners are located on a separate support and probe the individual strips. These two probes contact the DC and the AC pad of each strip. The sensor is moved by the XYZ-table in a way that the strips are located sequentially underneath the stationary strip probe needles. The system is controlled by a computer running a LabVIEW measurement program. The computer communicates with the motor controller and the instruments via an IEEE488 interface bus.

Fig. 5 shows the complete system with the computer on the left, the instruments in the middle and the probe box on the right.

Figure 5

Figure 6 shows the mechanical set-up of the probe station. On the left one can see the two stationary micropositioners. The support platform in the middle is seen carrying both the sensor and the micropositioner in contact with the bias line. A movable microscope and a light source are needed to adjust the probe positions as the structures are very small.

Figure 6

Once the sensor is placed onto the vacuum chuck, the system has to be aligned. Three reference points on the sensor are located so that the program can determine the orientation of the sensor and the pad positions. The pad layout of the sensor is loaded from a configuration file and, therefore, this system can measure different sensor layouts without hardware modifications. The measurement has to be done in a closed light tight box because the sensor is sensible to light. Moreover, the box serves as an electromagnetic shielding.

The software controlling the system is configured loading an input file. This input file contains instructions on measurement procedures like voltage range, voltage steps,

measurement frequencies, etc., but also the acceptance criteria for all parameters tested. This concept of an input file ensures that all tests and the acceptance cuts are performed in the same, well-defined way.

2.2.2 Electrical circuit

The electrical circuit of the probe station set-up is designed for high voltages up to 1000 V and very low currents in the range of a few pA. Therefore, HV isolation and shielding of all cables are crucial items. Several instruments and voltage sources are connected to the sensor pads (as illustrated in fig. 7) via two cross point switching matrix cards (Keithley 7153).

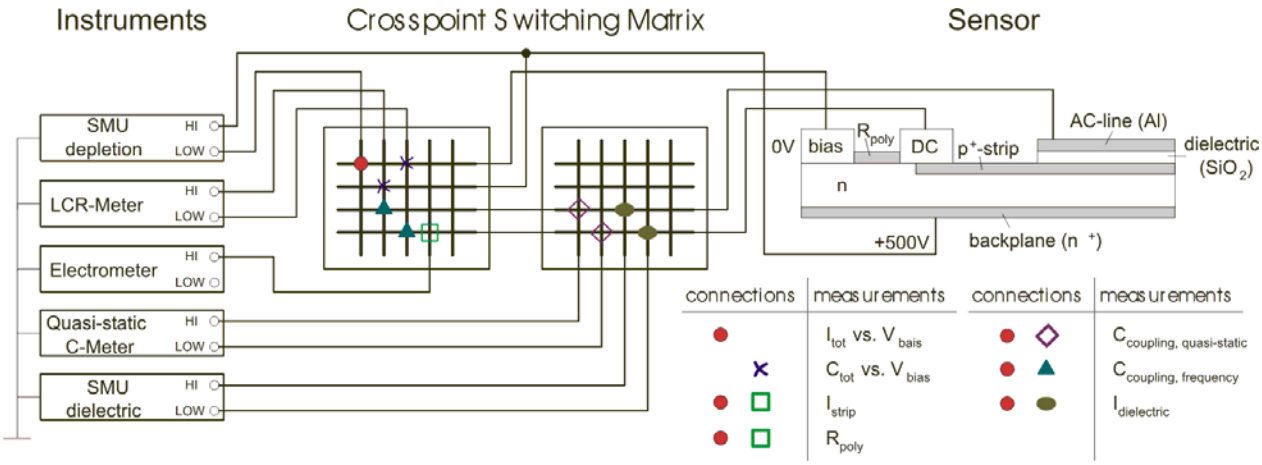


Figure 7

A source measure unit (SMU, Keithley 237) and an LCR-Meter (Agilent 4284A) are used to measure the total leakage current (IV) and the total capacity (CV) of the sensor versus the reverse bias voltage. Both quantities are measured during a single bias voltage ramp. After the voltage has been increased by one step and the leakage current has been measured, the switching matrix is reconfigured for the capacity measurement. To avoid the influence on measurements of parallel instruments the external ground connections have been used to close the current path. This also saved one line in the switching matrix. The measured values and deduced parameters like the depletion voltage (V_{depl}) can be seen in Fig 8. In this plot, the capacitance was measured up to 300V and is plotted as 1/C^2 to see a clear change of the slope to extract the depletion voltage. The dark current of the sensor was tested up to 550V in steps of 5V.

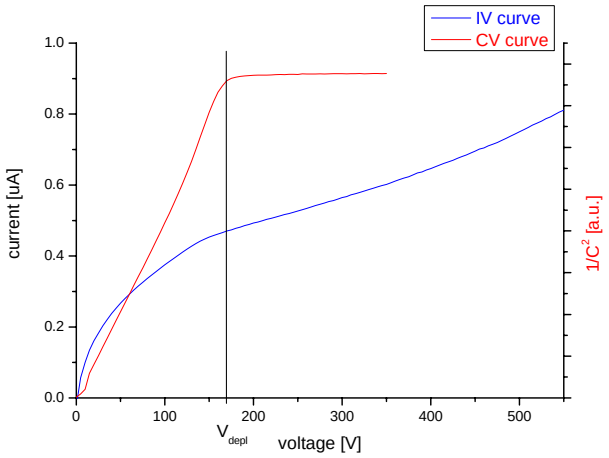


Figure 8

- After the bias voltage ramp has reached the defined upper voltage, the strips are scanned. The strip leakage current I_{strip}, the poly-silicon resistor R_{poly}, the coupling capacitance C and the dielectric current I_{diel} values are measured for each strip. The single strip current is measured with an electrometer (Keithley 6514). The measurement of the coupling capacitance and the check for pinholes are done with the LCR-Meter (Agilent 4284A) and a second source measure unit (Keithley 2410) probing the dielectric with 10 V. The poly-silicon resistor is also measured with this SMU. A typical result of such a stripscan on a sensor with 51 2 strips is shown in fig. 9. One pinhole at strip number 43 (high I_{diel}, low coupling capacitance) and one noisy strip (high I_{strip}) at position 300 can be seen.

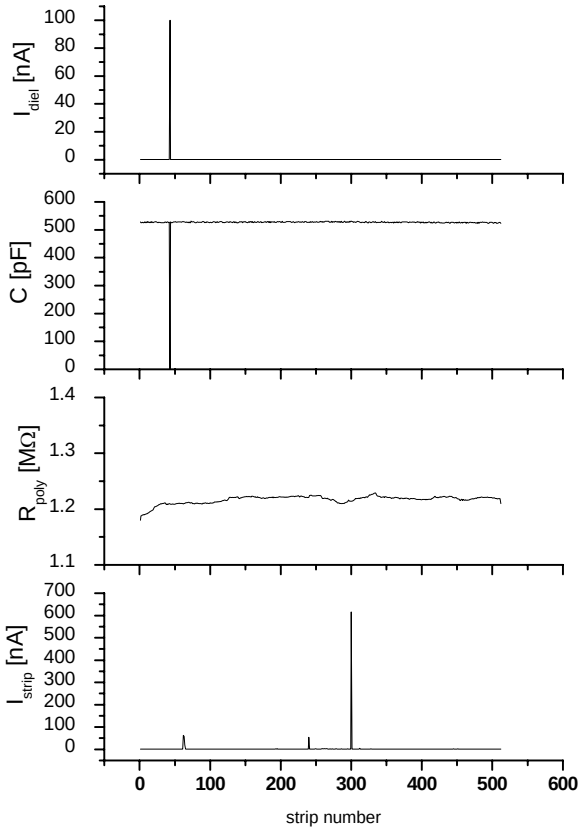


Figure 9

Once the strip scan is finished, the strip parameters are compared to the requirements defined in the input file. The measurement data are stored in a file.

This system was used to test and characterize the 10 sensors delivered by HAMAMATSU to LPNHE, of the new GLAST type and that are being mounted now on a ladder to test different lengths microstrips, in the so-called second prototype (see Section 4).

2.2.3. The Karlsruhe sensor characterization facility

The Karlsruhe sensor characterization lab is operational for more than 10 years being responsible for the quality control of sensors for Delphi, CDF II and CMS.
We run two fully automatic probe stations, which are very similar to the one described in the upper section by Vienna and is also accepting the same configuration files. We are able to do all standard strip characterization measurements, namely strip currents, poly resistors, coupling capacities, interstrip capacitances, interstrip resistances, currents through oxide with voltage applied, etc.. All parameters can be monitored versus time and/or versus voltage. The station may run in scenario mode, meaning several completely different measurements can automatically be done in a consecutive order with different delay times and parameter changes. Both stations can even perform all strip measurements on full sized CMS module containing two independent sensors. One of the stations, ready

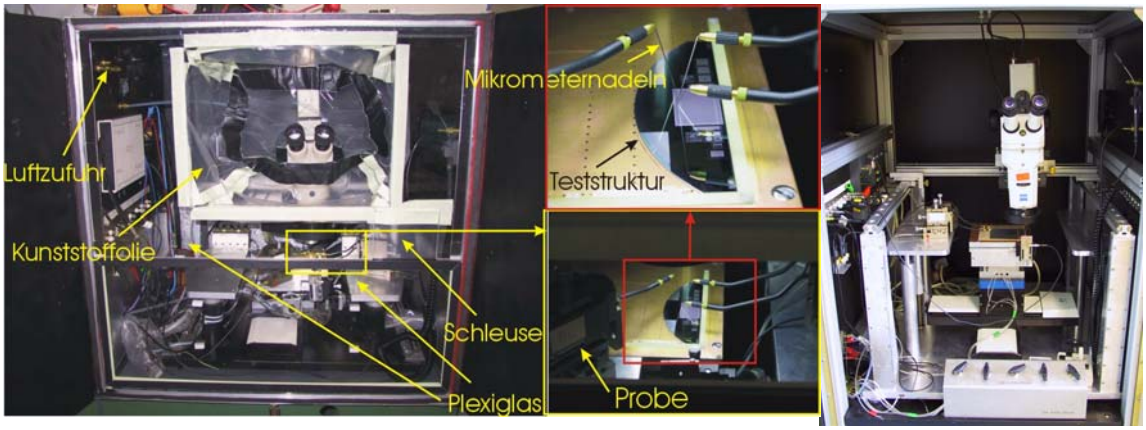


Figure 10

for post irradiation measurements is able to be cooled or warmed. The temperature ranges from -12°C up to 100°C. Both stations are home-made therefore being very flexible to implement almost all kinds of measurements. Both stations are shown in figure 10.

Another long term station is able to monitor currents for up to 10 sensors parallel over long time. Our instruments are 3 Keithley 6517 electrometer, 2 Keithley electrometer 617, 2 Agilent LCR-meter 4284A one SMU Keithley 2410 plus 1 Keithley multimeter 2010 with scanning card.
In figure 11 some illustrious examples are displayed, namely leakage current, Rpoly and coupling capacitance strip scans before and after irradiation, followed by depletion voltage

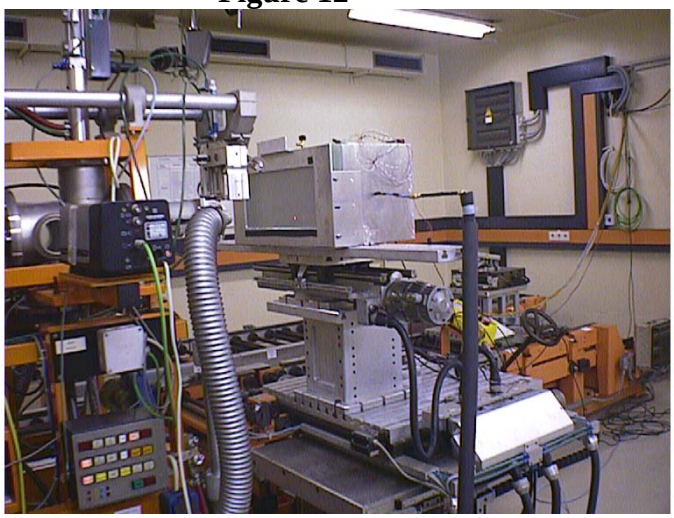
evaluations versus fluences: The 5th plot shows an interstrip capacitance measurements versus voltage in the sub-fF range. The last plot shows Rpoly versus voltage, the field establishing on the junction side is clearly visible in the first 20V.

Figure 11

2.2.4. The Karlsruhe irradiation facility

In order to monitor radiation hardness for prototyping and/or production quantities, Karlsruhe has a long time experience, being responsible for the radiation hardness of CMS sensors and modules. In figure 12 one can see the beam area in our cyclotron facility on site. The box in the middle represents the sensor or module carrier. The carrier is sitting on an X-, Y-stage, whose fast movement guarantees a homogeneous irradiation. Areas of 20X30cm² may be irradiated. With dry air passing a liquid nitrogen dewar, we are able to establish a -25°C environment during radiation. The facility runs smoothly since several years with a 34MeV proton source and achieves ~1*10^14 1MeV_N_eq / cm² on a 100cm² in about 15 minutes, when running in low fluences mode (heat up limit). Dosimetry is done by measuring the cyclotron current and crosscheck by Ni-foil activation measurements. Results are displayed in figure 11.

Figure 12



2.3 Development or follow up of new sensors and different sensor shapes:

The main aim is to define the needs and to convince the industrial firms to produce the corresponding sensors. The present goal is to have larger wafers (at least 8''), thinner and with a smaller pitch. HAMAMATSU is currently part of this R&D project and we expect this firm to be able to produce the wafers both for the preliminary prototypes that are extensively tests on our Lab test benches, then for test beam detector prototypes, and later on for the construction of the overall tracking system. At LHC this firm has demonstrated to produce the higher quality sensors in the most reliable way. We anticipate this is going to continue to be the case.

2.3.1 Development of complete framework to fabricate prototype sensors:

However, there is also some ongoing R&D on sensors, at some Laboratories that are part of the SiLC collaboration. The aim is to pursue advanced R&D on Si detectors. This will allow to have centres that are able to produce prototypes that eventually will be transferred to industrial firms for massive production. For instance:
The Korean group is fabricating new double-sided strip sensors, using 5'' wafers [7]. They are made in their research centre and no industrial firm is involved. The wafer size is 5,56 cm x 2,95 cm, 380µ thick , 50µ readout pitch both on p and n sides and a total of 512 readout channels on each side. Therefore this research Institute is developing a 5 inches fab line for double sided silicon detectors whereas at the present time HAMAMATSU has only 4 inches lab line. And this Institute is intending to develop a fab line producing wafers with a size larger than 5 inches.

The prototypes have been first submitted, for quality check, to electrical tests I-V of similar type to those performed in Vienna or Karlsruhe. They were then submitted to a test with a SR90 radioactive source and the measurements just achieved give a signal over noise ratio of 10 for these sensors (see Fig 13).

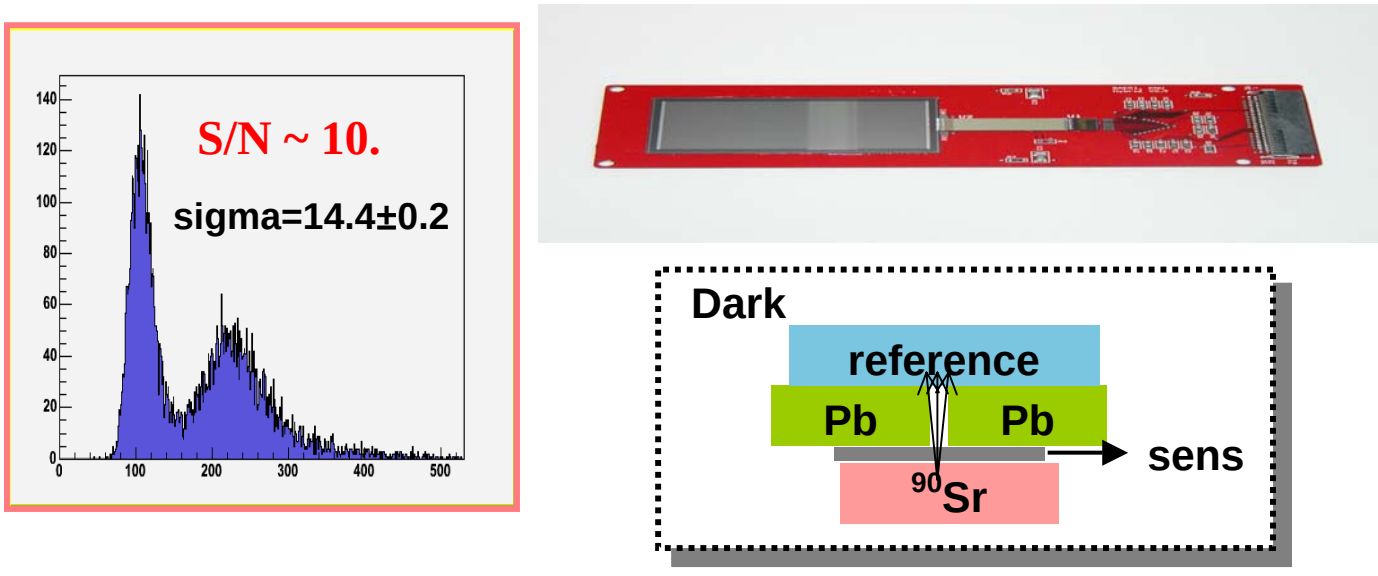


Fig 13: Measurement of the signal to noise ratio with a Sr90 radioactive source as provided by the microstrip sensor developed by the Korean Institutes. The new prototype sensor is shown on top right and is read out with VA1 F.E.chip.

They will be submitted to radiation hardness tests, using beams at KEK.

2.3.2 Other available facilities for sensor R&D in the SiLC collaboration.

Other Institutes in the SiLC collaboration are also interested in exploring new sensor technologies and they have developed both expertise and appropriate equipments for achieving this R&D aspect.

This is the case of the IMB-CSIC in Barcelona which developed various technologies P-on-N, N-on-P, N-on-N with wafers with pads, strips or pixels, high resistive poly, capacitive coupling, two metal layers, two sides processing (see Figure 14). They are limited to 4 inches technology.

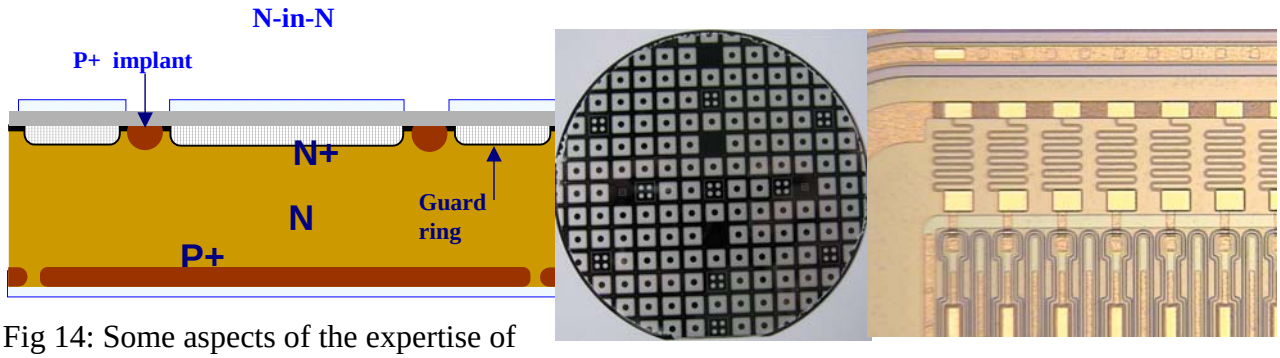


Fig 14: Some aspects of the expertise of IMB-CSIC on sensor R&D

Another Institute in the SiLC collaboration exploring sensor technologies is Helsinki Physics Institute. They are developing 3D Si detectors and have a large expertise in the domain.

There are very useful software packages that allow detailed Si device simulation by including the characteristics parameters of the detector technology (provided they are given by the manufacturer) with the electrical simulation. They provide, for instance, a reliable simulation of the charge collection and charge sharing in 3D. They are very useful for both developing the F.E. electronics attached to such detectors and for implementing the results in the simulation of the full detector (GEANT based), in order to fully apprehend and study the performances of the detectors. Several Labs (ex: IMB-CSIC, Helsinki, Paris) in the collaboration are equipped with these packages and have gained expertise in using them.

2.3.3 Keeping close contacts with new Si sensor technologies or various sensor shapes.

Moreover contacts are established or being established with new detector technologies developed in particular for the microvertex. We are starting to investigate the possible special needs for certain parts of the inner Silicon tracking, as for instance, the disks in the very central forward location. In the initial design these disks, that sit very nearby the microvertex, were proposed to be made with pixels like those used in the ATLAS experiment i.e. 50µx300µ pixels.

Also under study is the possibility to use different sensor shapes (ex: trapezoidal large size sensors, R-Phi detectors as used for the VELO detector in the LHCb experiment, see Fig. 15). These two different sensor shapes are under consideration to design respectively the forward

Si trackers in the projective case (see Section 4) and eventually some of the internal forward disks.

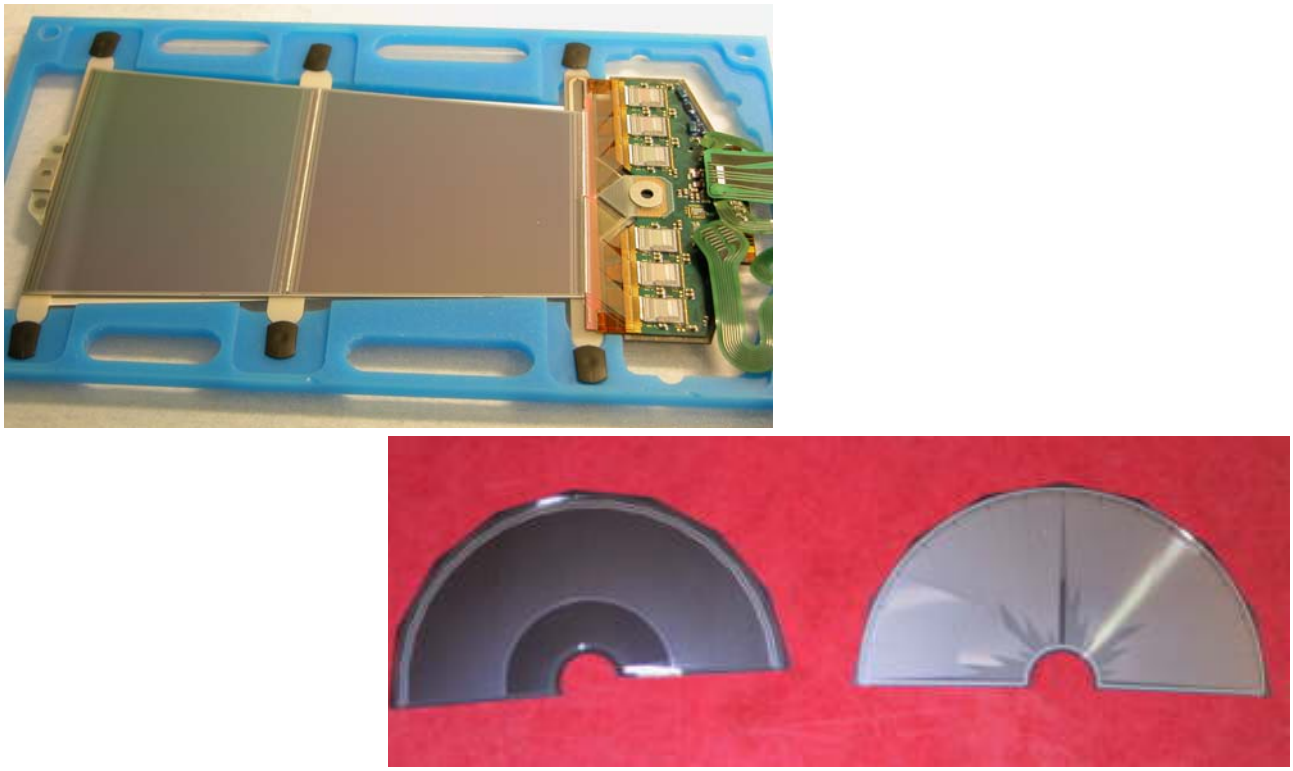


Fig 15: Top photograph shows a ladder made of two trapezoidal wafers bonded together to be part of the forward disks for ATLAS tracking system. Bottom photograph shows a R-Phi detector as designed for the VELO detector of LHCb.

4. R&D on Front End and readout electronics

The readout electronics system should not degrade significantly the intrinsic detector performance within the environment of the ILC detectors, matching therefore the following constraints:

- Comply the duty cycle of the ILC machine, being presently defined as sequences of one millisecond data taking times of 2986 bunches separated by 337 ns, followed by 2 milliseconds readout times.
- Ensure an electronics MIP to noise ration of 25, at 3 μs shaping time, for a 50 pF capacitance Silicon detector strip.

- Provide a continuous stream of loss-less compressed digital data at the end of each bunch train.
- Dissipate a total average power under 15 Watts.
- Minimize the on-detector total material regarding transparency to radiation.
- Ensure the reliability of the whole system for 5 years over the 2 million channels.

These constraints dictate for active components making use of highly integrated electronics, implementing the best suited analogue and digital signal processing techniques and algorithms, with the most up to date reliable technologies, keeping in mind the most likely ILC detectors construction time-scale. Mechanical supports and fast data transmission media should make use of the thinnest and most transparent materials leading to a total budget less than:

- Silicon chips 100 cm^3
- Beryllia or Kapton supports 400 cm^3
- Fiber optics 300 cm^3

Two main F.E readout electronics are developed; their current status is discussed in the next following two subsections.

3.1 FE Electronics developed by UCSC

The Santa Cruz Institute for Particle Physics (SCIPP) has been developing a deep-submicron (0.25 μm) "LSTFE" ASIC optimised for reading out silicon microstrip ladders of length approaching two meters, with a temporal resolution commensurate with the nominal 337 nsec crossing time of the ILC **[8]**. A pulse-development simulation developed at SCIPP indicated that a 3 μsec shaping time preamplifier would be quiet enough to read out a 167cm ladder – the half-length of the current SiD design. Power would be cycled at the 5 Hz repetition rate of the ILC, saving approximately 99.5% of the IV power loss, and eliminating the need for active cooling.

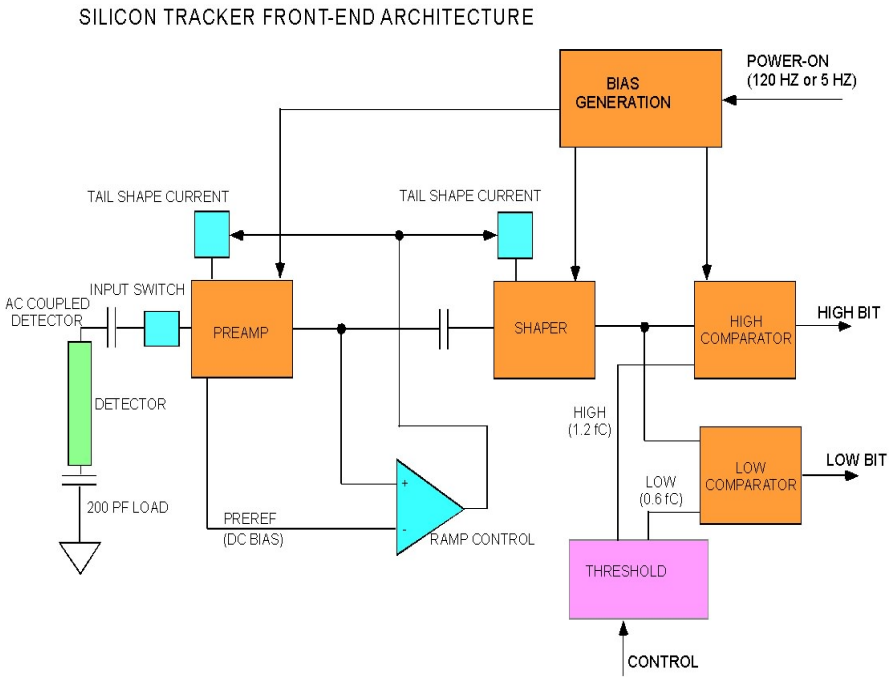


Figure 16: Schema of the F.E. electronics chip developed by SCIPP

SCIPP Lead Engineer Spencer has designed a prototype eight-channel front-end ASIC, shown in block form in Figure 16, which will be submitted to the MOSIS consortium for fabrication on May 9, 2005. In addition to a long shaping-time, low-noise preamplifier, the

chip features a double-comparator discrimination system, from which analogue information will be derived via time-over threshold. The high comparator will protect against false signals from electronic noise while maintaining efficiency for normal-incidence track in excess of 99.9%. The low comparator will be read out for nearest neighbours of channels exhibiting a high threshold crossing. The information from the nearest-neighbour channels that cross the low-threshold will be essential for centroid finding, as shown in Figure 17, which shows the point resolution as a function of the low-threshold comparator setting for the readout of a 167cm ladder. For this ladder, the high threshold operating point is 0.29x(min-i), and so the use of the lower-threshold comparator is expected to reduce the point resolution from 9 to 6.5 μm, within the 7 μm spec of the SiD tracker.

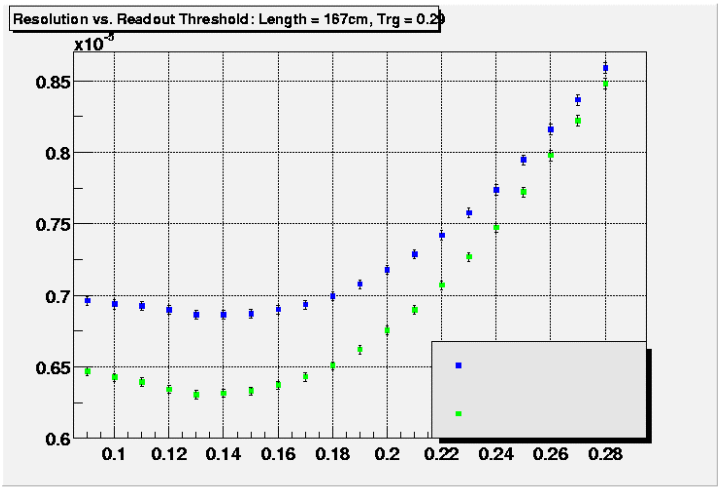


Figure 17: Gaussian-fit (green) and RMS (blue) resolution of a 167cm ladder read out by the SCIPP LSTFE front-end ASIC, as a function of the lower comparator threshold setting, as a fraction of min-i. From simulation; the resolution is in unit of 10^{-3} cm.

A full test-bench system has been developed at SCIPP, including an FPGA-based readout system, in preparation for the arrival of the LSTFE ASIC in July. Results are expected for the Snowmass meeting of the American Linear Collider Physics Group.

After submission of the chip on May 9, SCIPP will begin to consider the back-end and data-transmission issues associated with the readout of long ladders at the ILC. In addition, work is underway to define the makeup and goals of a test beam run, expected to take place in late 2006, in collaboration with LPNHE Paris and Fermilab.

It is expected that in mid 2007, after analysis of the test beam data, this proof-of-principle will allow for the fair comparison of the advantages and draw-backs of the long-shaping time approach to reading out silicon ladders in the barrel region of the Linear Collider Detector. Milestones en route include results from the prototype ASIC in August 2005, the development of a multi-channel test beam prototype, with appropriate back-end digital and data-transmission architecture by March, 2006, and then implementation on a long-ladder test beam run in Fall, 2006.

3.2 E.E. and readout electronics developed by LPNHE

The actual goals of this development are low noise preamplifiers, shaping times from 500ns to 5µs (depending the strip length to be read out, namely tiles or longer strips), an analogue sampling, highly shared ADCs (at least 512 channels), sparsification, very low power dissipation, power cycling, compact and transparent. For several of these reasons, we choose to work with CMOS deep sub micronic technology, starting with the one which is currently available and fits best our needs (UMC 0.18µm technology). We are also considering the possibility to use SiGe for the very front-end analogue part of the chip [9].

3.2.1 The front end and readout scheme

The schema of principle of the Front End and readout electronics as developed by LPNHE team is shown here below in Figure 18.

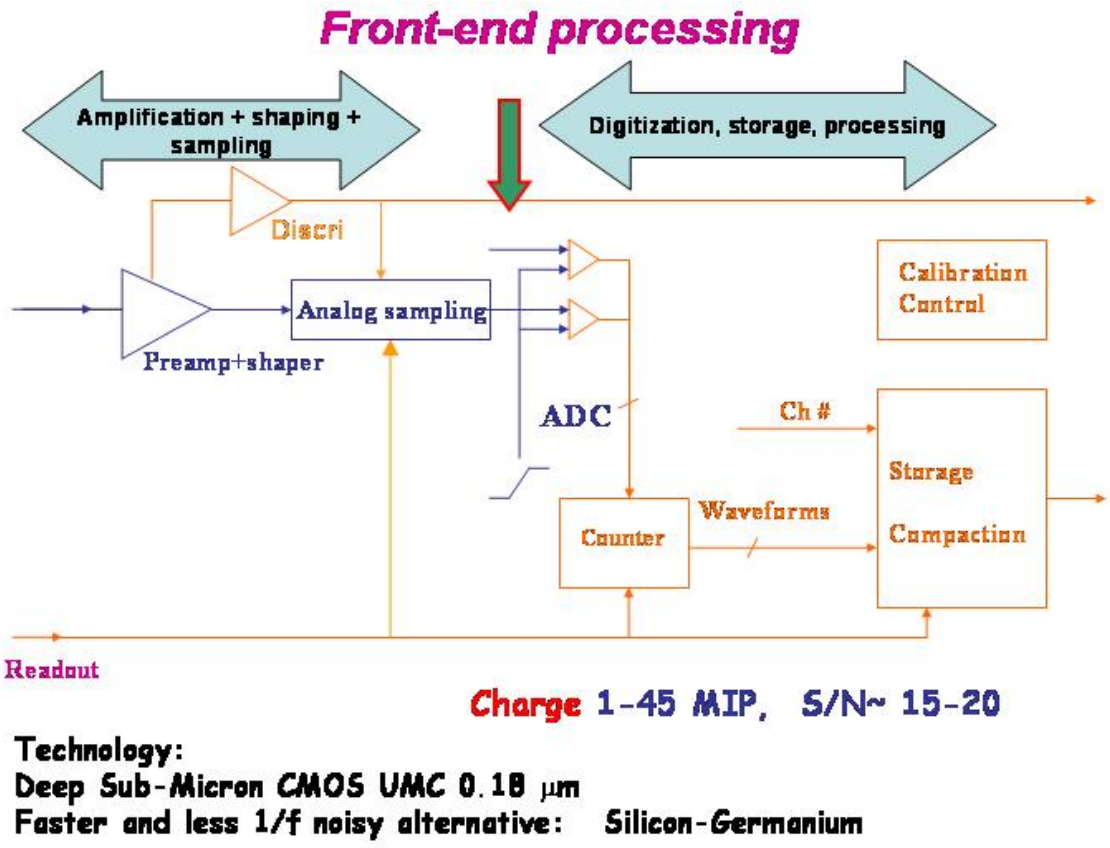


Fig. 18: Schema of the front-end readout as developed by LPNHE team.

3.2.2 **R&D program**

Started in June 2004, an intensive R&D program intended to achieve the following goals:

Fall 2004:

- Submission to Europractice of a Deep Submicron CMOS prototype chip (UMC 0.18 µm technology) integrating 16 analogue readout channels including (Figure 19)
- Low noise amplifiers (see Fig 20)
- Pulse shapers
- Sampling devices
- Comparators

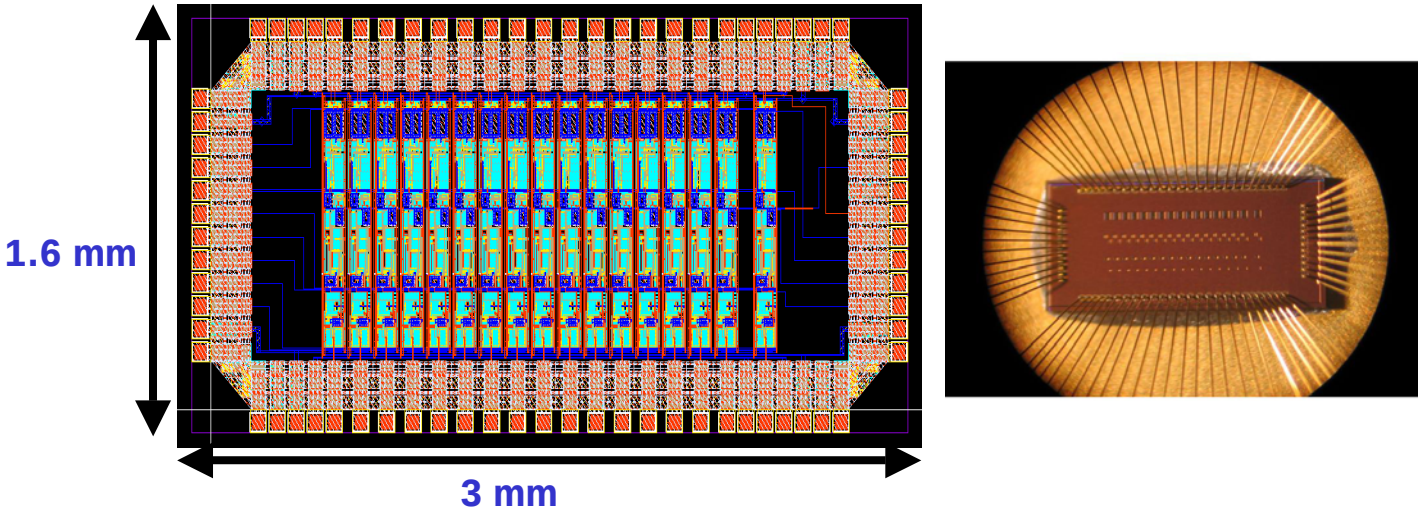


Fig 19: Layout of the LPNHE chip with 16 channels + one for detailed tests of each component of the channel. On the right side there is a photograph of the actual chip as received from the foundry.

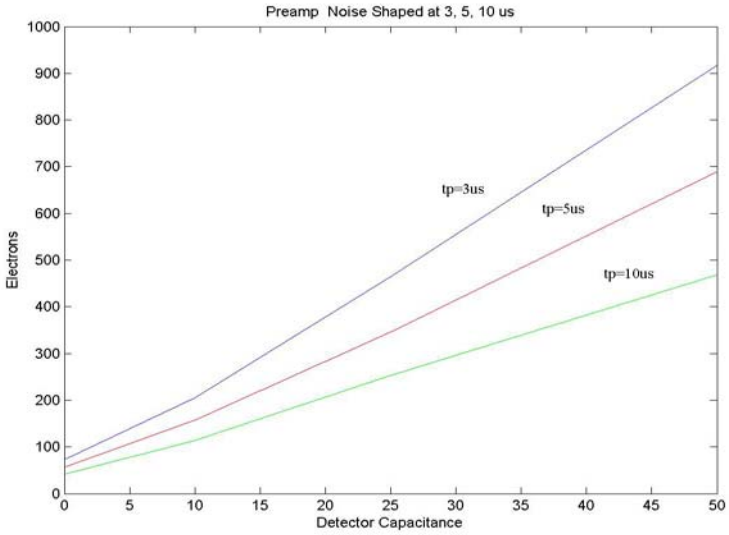


Fig 20: Simulated FE noise as a function of detector capacitance for 3 shaping times 3, 5, 10µs

- Extensive tests of the prototype chip on an electronics test bench as well as on an actual Silicon strips detector.
- Detector simulations using the TCAD Silicon process simulator.

3.3.3 Results

Submitted Nov 2^{d} 2004, a prototype chip has been received Feb 23^{d} 2005, and two samples are presently under tests. First results are positive regarding noise and power that are within specifications: at 3.3 pF input capacitance and 3 µs shaping time, the measured noise is 180 electrons (upper limit) against 140 expected. Power per channel of 330 µWatt is measured, as expected. The linearity has been measured and looks satisfactory; the 1.5% non-linearity for low level signals will be improved for high level signals. A custom socket is being designed at LPNHE in order to allow the extensive characterization of the full 30 sample chips set. Ten bare samples have been delivered, to be wire-bonded to an actual detector and tested in-situ. Figure 21 shows an example of the very encouraging preliminary results obtained when testing the chip on the test board (Figure 22).

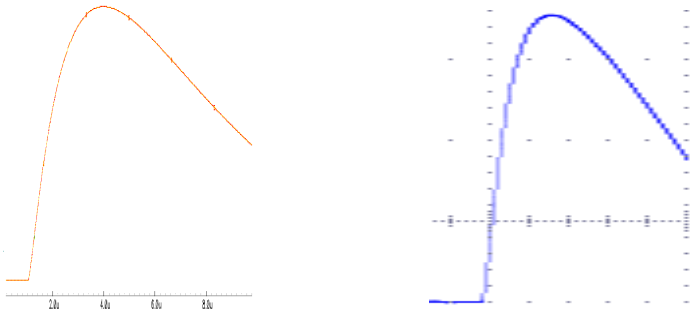


Figure 21: Simulated and measured shaper outputs (Horizontal: 2 µs / division)

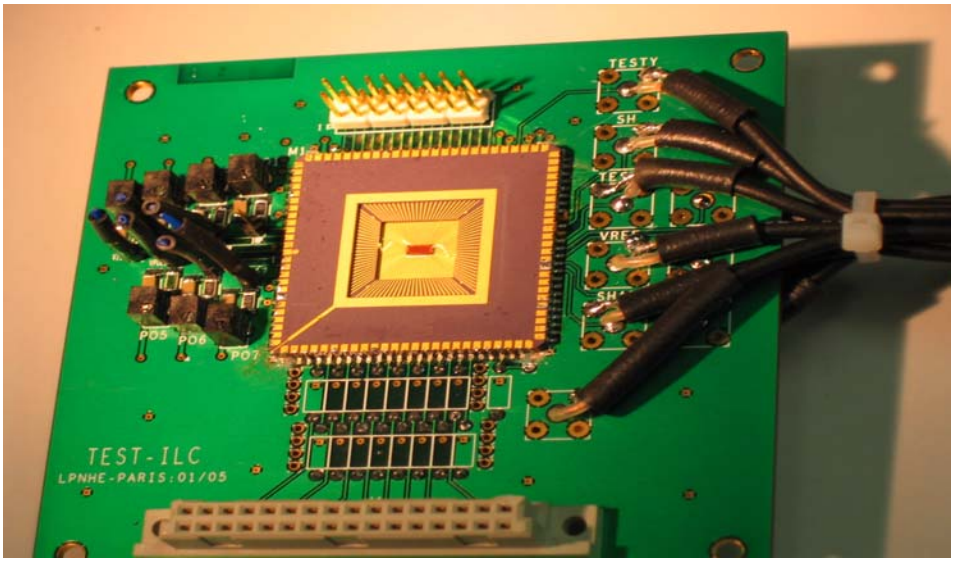


Figure 22. Test card for the CMOS 180 nm prototype chip.

The readout architecture optimisation leads to the current design of analogue pipe-lines and their readout control to be included in the next 128-channel chip in the UMC 180 nm CMOS process, as shown Figure 23.

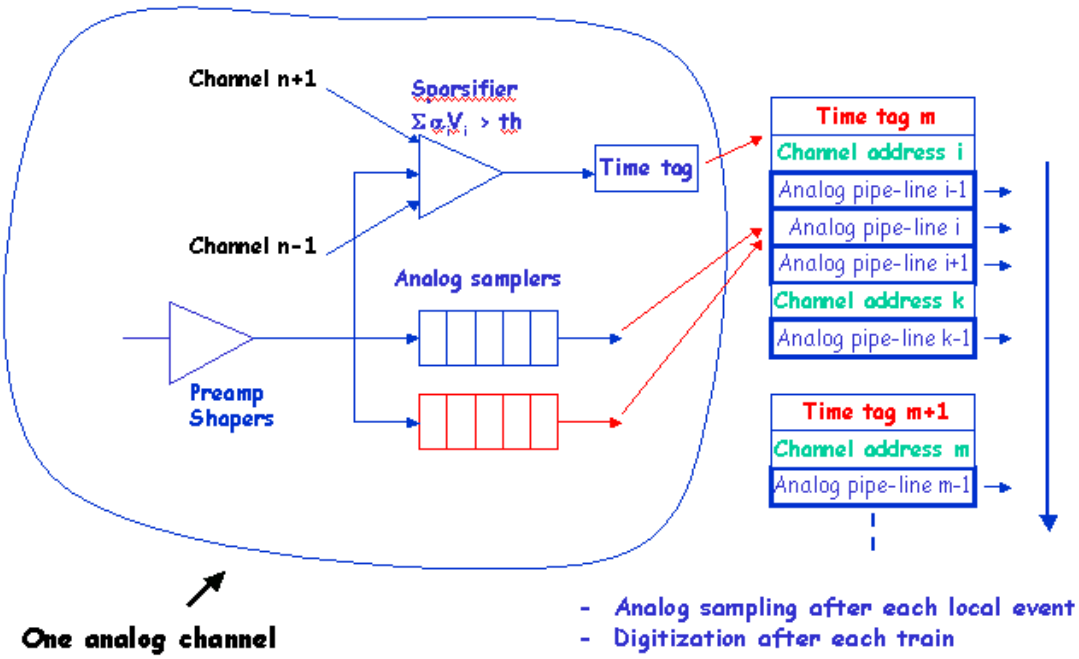


Figure 23 Some details of the Front-end Readout electronics

Whenever the sum of the charges collected on three adjacent strips exceeds a given threshold, a time stamp and channel number are recorded, and the analogue pipe-lines continuously running are frozen waiting the end of the data taking stage to be digitised. After two shaping times, the shapers outputs point to the next available analogue pipe-line and starts recording again. At the end of the train, analogue pipe lines locations that contain relevant information are digitised, using the multiplexed ADC able to convert one location from all channels at the same time (Figure 5).

In parallel, in order to understand the detector behaviour and optimise the readout electronics, simulations with a process Silicon simulator (TCAD, Silvaco) are underway, using the Silicon strips process (HAMAMATSU) available parameters. Results are compared to the test bench measurements, providing help to match the detector and front-end electronics.

3.3.4 Next future plans

Starting from the results described in the last section, The R&D program should proceed as follow:

Summer 2005:

Extensive tests of the prototype chip wire-bonded to an actual Silicon strips detector using the LPNHE test facility under various detector stimulations such as Laser diode IR light, and ^{90}Sr beta rays source (See Test bench Section).

.

Fall 2005:

Submission to Europractice of a 128-channel readout chip including:

- Low noise amplifiers
- Fast and slow shapers
- Fast and slow Sampling devices configured as a structured addressable analogue memory and its digital control
- 10 bit Analogue to Digital converter

The design of a readout system for the Silicon strips detectors has started and is in progress with the delivery and tests of a Deep Sub-micron CMOS prototype chip, demonstrating the concept of a highly integrated analogue readout chain under very low power dissipation, compatible with the Silicon strips detector requirement at the ILC. Simulations and tests of the detector are underway, in order to understand and optimise the coupling between detector and front-end electronics.

4 R&D on Mechanics

The aims of the R&D on Mechanics are:

- Low material budget
- Easiness of construction (simple modular structure, transfer to industry)
- Robustness
- Low cost
- Integration issues

Therefore an active R&D on Mechanics is conducted on the following aspects:

4.1 Detailed CAD designs

The detailed CAD design of the various components of the tracking system, is studied in this collaboration for both the SiD and the LDC detector concepts, and taking into account the specificities of the GLD design.

It is important to note that, also in this aspect of the R&D for Si trackers at ILC, there are close contacts with the SiD and LDC proto collaboration, through regular meetings and exchange of information. Several teams are involved in both detector concepts and have signed for them. *This makes this R&D a unique place to study in details and compare different detector concepts and their performances*.

The CAD tools are crucial to design in details the different components of various tracking systems and therefore to get a deep understanding of their feasibility, of what are the problems and eventually how to solve them. There is an ongoing brain storming on the possible modifications of the actual baselines for the various detector concepts. This tool plays a central role to rapidly respond to this quickly evolving work. Besides it allows the

definition of the geometry DB of the detector designs, needed for the GEANT based simulations. We have developed the needed tools and expertise for this work.

Although the main difference in the proposed detector concepts is their tracking system, the related study and R&D can be done -- and greatly profit from being done -- within a collaborative framework such as SiLC. Indeed their main issues and challenges are quite similar in many respects. For the mechanics we have to study the different components of such systems, namely: the internal barrel and forward components and the external barrel and forward components. Whether the tracking is all Silicon or Silicon plus a TPC, this does not really modify the main aspects of the mechanical design of the components and of the related issues [6].

SiLC is undertaking a detailed study for both, the all-Silicon and the Silicon plus TPC tracking systems. In the case of the LDC concept, it was proposed to have a complete coverage of the central TPC with Si trackers all around the TPC. This is the so-called Silicon Envelope[4], shown in Figure 24, which is composed of the 4 fundamental parts of a complete Si tracking system: inner and external components both in the barrel and forward regions. Here below we will describe the present status of these ongoing detailed design studies for each component for both the SiD and LDC concepts.

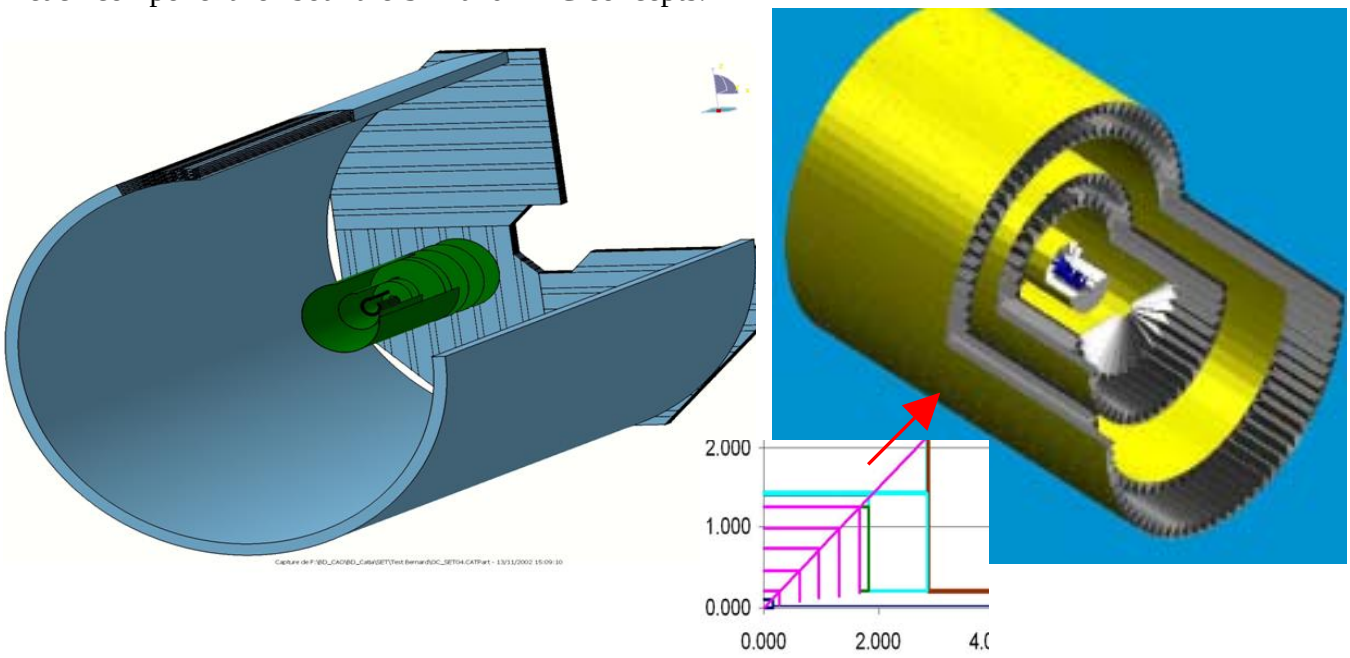


Figure 24 shows on the left the design of the Si Envelope in the LDC case; the external components in the barrel and the forward are in blue, the innermost parts in the barrel and in the forward are in green surrounding the microvertex also in green. The TPC would be located inside the volume defined by these external and innermost components .On the right is shown the general sketch of the Si tracker for the SiD concept together with a quadrant view.

4.1.1 The internal barrel Si tracker

The innermost layers of the Si tracker have to make the transition between the microvertex and the outer tracker which consists of Si layers in the SiD case and of a TPC in the LDC and GLD cases. But the issues are the same: in order to have a smooth transition, these layers have to give a very precise spatial resolution of order 7 µm. In the LDC case it is proposed to have 2 or 3 double sided layers made of ladders with strips of 30 cm length ensuring for the first layer nearby the microvertex to have the electronics on the edges of the

detector and likewise for the following layer. The preliminary simulation studies with SGV fast simulation indicate that the expected level of occupancy allows for this strip length.

SiD designers prefer to use tiles, it is to say single sensor as basic component of the detector architecture. The price to pay for this, is a much larger number of channels and so the increase in power dissipation (and price) as compared with longer strips.

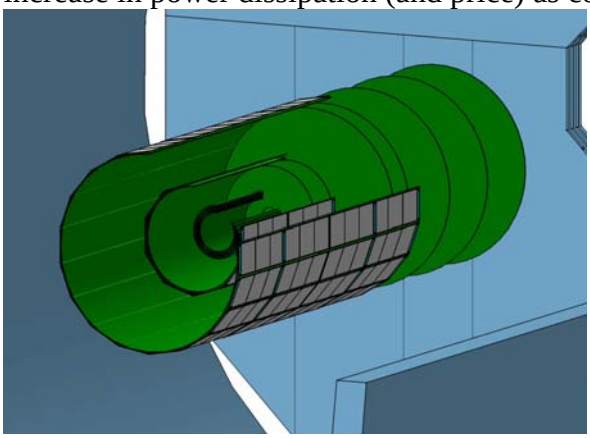


Figure 25

Figure 25 shows the design of the two innermost Si layers situated respectively at a radius of 16 and 30 cm from the beam axis. The first layer is 60 cm long along the beam axis. It is made of ladders with strips of 30 cm long.

4.1.2 The external barrel Si tracker

The construction of large area layers in the barrel part of the tracking system, started by the innermost layers described in the previous section is pursued in the outer layers. In the present SiD baseline design the barrel comprises 5 layers all made of tiles, i.e. of single sensors of 10 cm by 10 cm and Figure 26 shows the actual proposed design.

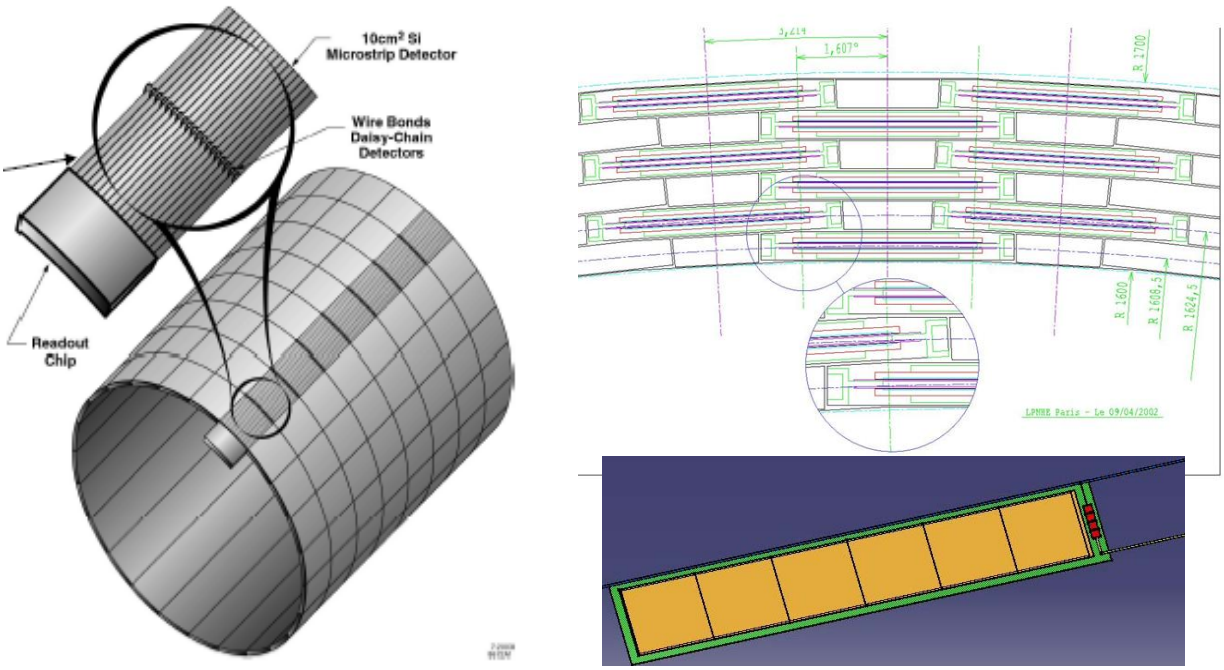


Figure 26: Outermost layers made of tiles in the SiD case (left) and of longer ladders inserted in the structure with alveoli in the LDC case (right)

In the case of the LDC, the outermost barrel part included between the TPC and the e.m. calorimetry is inserted in a Carbon fibre structure made of alveoli, and the basic element are long ladders made of 6 sensors bonded together that make 60 cm long strips [10]. Such ladders are also shown on Figure 26. Hermeticity is ensured both in the longitudinal and radial directions. Of course such ladders can also be used to build the outermost layers of the SiD central tracker. The occupancy permits this strip length according to preliminary simulation studies. This whole issue of occupancy is now starting to be addressed with the GEANT based simulation and the accurate description of the detector elements and geometry.

4.1.3 The internal forward Si tracker

The forward region is a key-region for Physics at the ILC centre of mass. To have a highly performing tracking system at large angle is therefore mandatory. It is also important to address with great care the overlap between central and forward tracking.

In the LDC case the innermost forward Si tracking components covers between 25 and 7 degrees with respect to the beam axis. There is almost no TPC information available in this region. Thus these very first disks must link the microvertex to the external forward tracker and sitting between them there is the TPC end cap. Figure 27-a is a sketch of this region in the LCD case (left) and the SiD case (right).

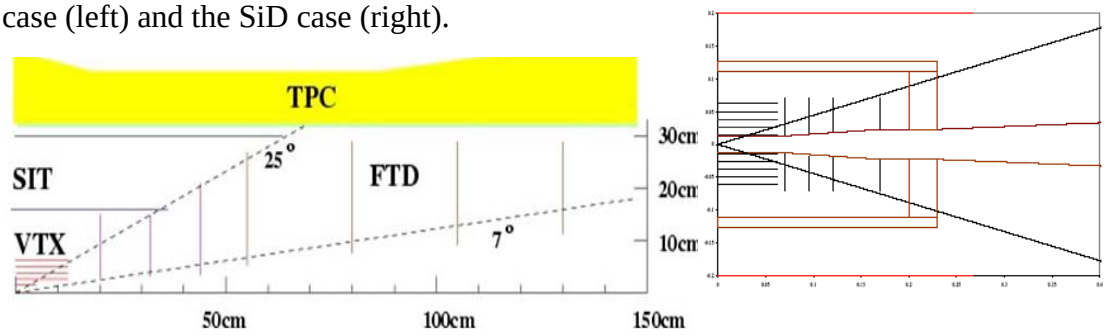


Figure 27-a

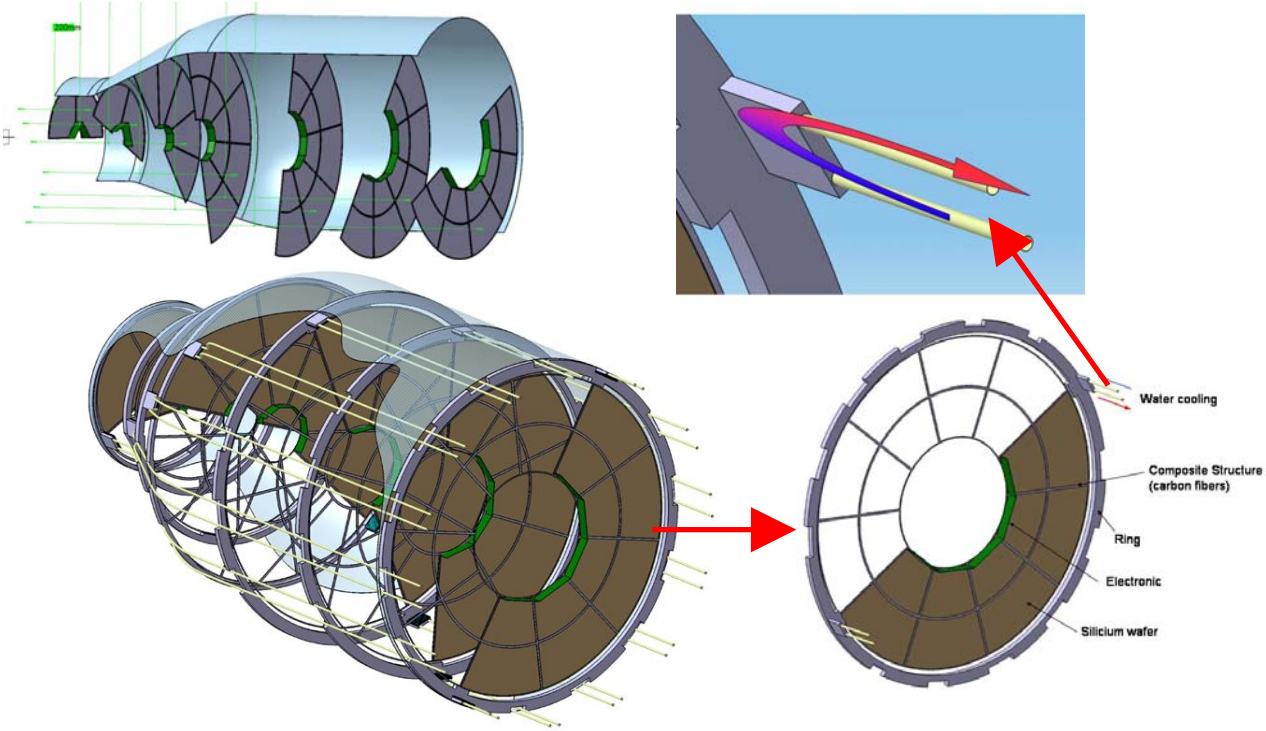


Figure 27-b

The work has started to study in more details this innermost forward region. Figure 27-b shows the most advanced ideas in the case of the LDC concept. It is foreseen to have a total of 7 disks, the three innermost ones are presently made of Si pixels. But we are considering as mentioned in Section 2 to use instead new Si technologies as those that are proposed for the microvertex[5, 6]. The following 4 disks would be made of strips and the R-Phi detectors built for the VELO detector in LHCb are of particular interest to fabricate these disks. This work is just starting at LPNHE, and some new teams are interested to join this effort.

This work directly applies to the SiD case, where in the present design, 4 disks are sitting in the direct neighbourhood of the microvertex.

4.1.4 The external forward Si tracker

Two possible cases are studied for the external forward layers, namely to apply the projective design as in the case of the innermost forward disks or an XUV design [11].

Figure 28 shows the projective case. This is the solution adopted for the forward trackers of the LHC experiments (ATLAS and CMS). However here the difficulty is that all or part of the external forward layers must cover much larger length in radius, namely above 1m in radius (presently it goes up to about 1.6 m in radius) and thus it makes the projective design more tricky as shown in Figure 28, here below [5, 6] .

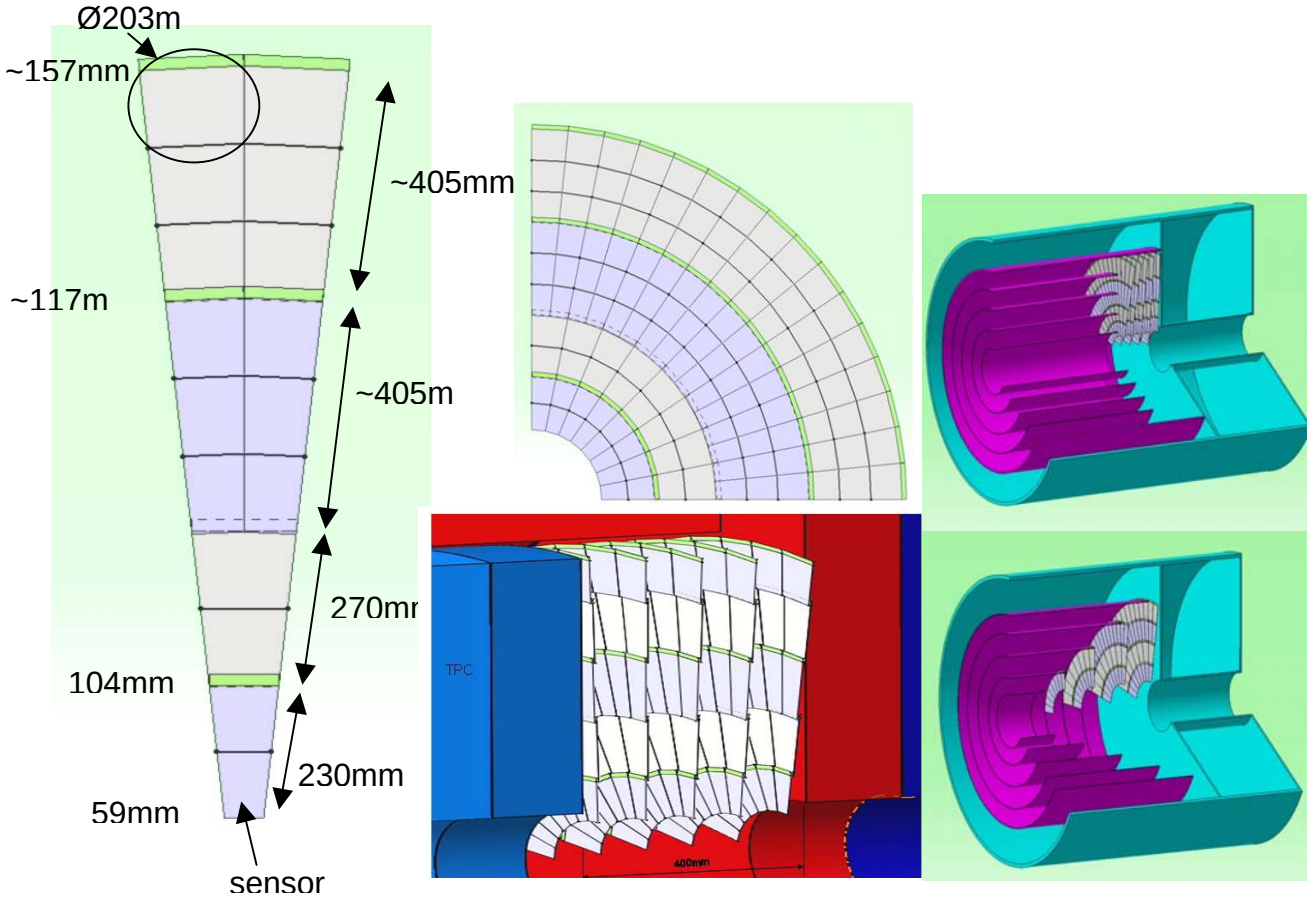


Figure 28: The projective design for the outermost part of the forward Si trackers (as designed by LPNHE). On the very left is shown the basic sector. A full quadrant is composed of 8 such sectors as shown on the middle top design. The application to the LDC case (middle bottom) or the SiD forward parts (right).

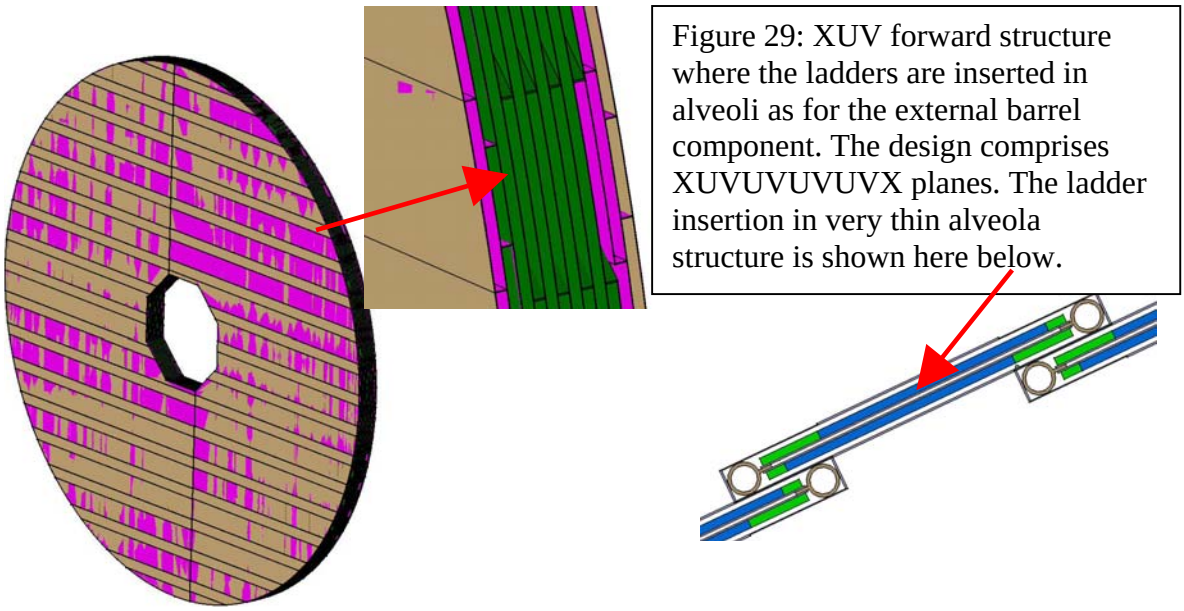


Figure 29: XUV forward structure where the ladders are inserted in alveoli as for the external barrel component. The design comprises XUVUVUVUVX planes. The ladder insertion in very thin alveola structure is shown here below.

The Figure 29 shows the current status on the XUV alternative design for the outer forward Si tracker or Si layers. The asset of this solution is to be able to build the whole detector, with a single type of sensor, as for example a 10 cm by 10 cm sensor like for the barrel part. But the design is not as simple as it may appear at first.

The projective and XUV cases will be studied with detailed simulations and compared.

4.2 Construction of the basic element

The basic element of the Si tracker architecture is the ladder which is made of one or more than one sensor bonded one to the other with a very precise alignment.

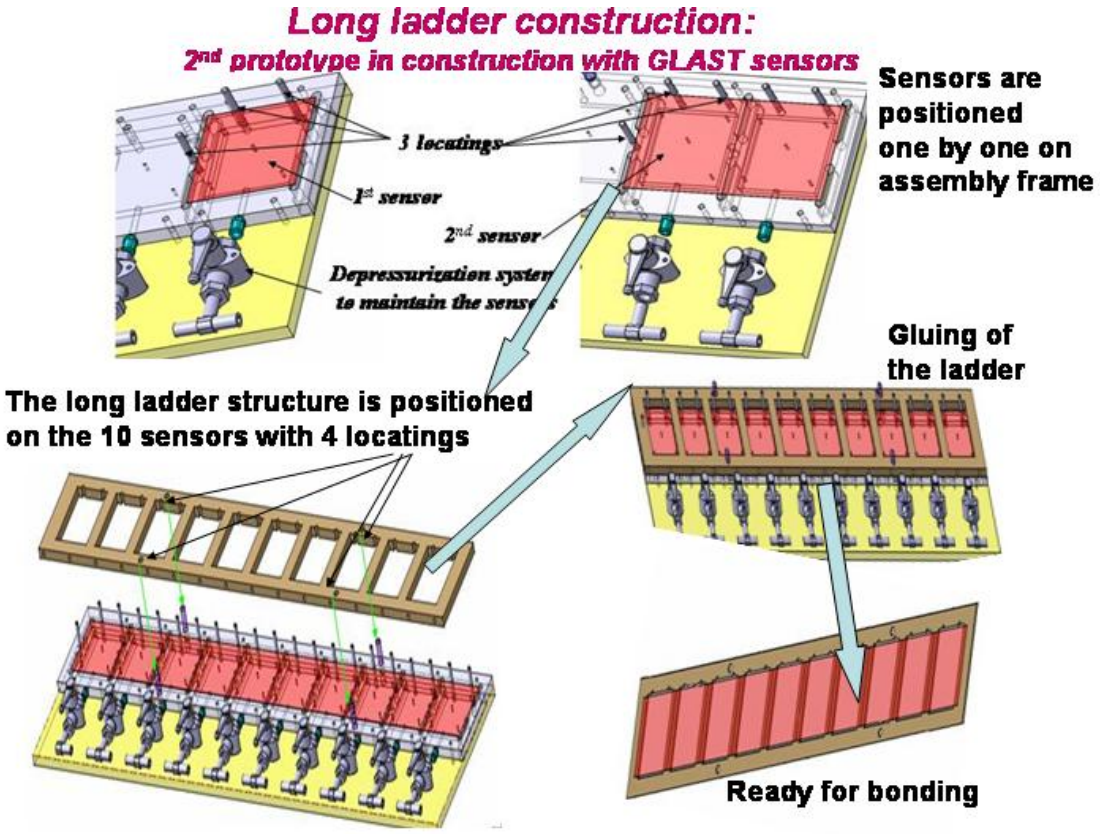


Figure 30: Schema of the long ladder construction, here made of 10 sensors.

The procedure to build ladders with strips of relatively long length was developed in various places and already used in several experiments in particular to build Si strips microvertex at LEP or Tevatron for instance. The most challenging ones were built for the AMS Si tracker where up to 15 sensors were bonded to one another to make very long strips [12]. A very precise method was developed by this collaboration. The aim in our case is to study it and see how it could be transferred to Industry. Also by using larger size wafers this would decrease the number of sensors to be bonded together and thus facilitate the overall operation.

As schematized in Figure 30, the sensors are positioned one by one on the assembly structure, with locatings. A depressurization system is used to maintain the sensors once on the assembly structure. The long ladder Carbon Fiber structure is then positioned on the sensors with 4 locatings and glued to the sensors. The sensors are then ready for the bonding.

4.3 Thermo-mechanical studies

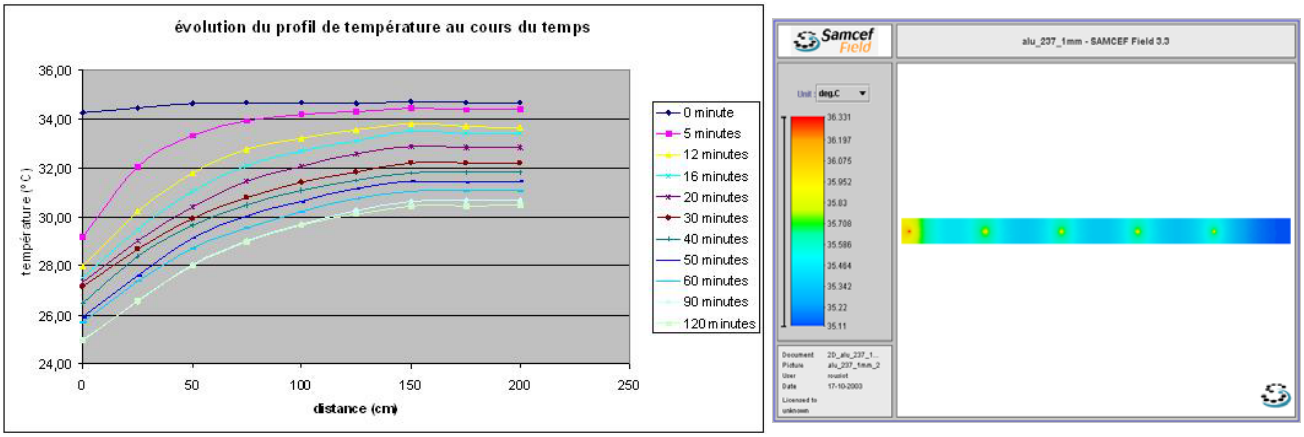
The cooling system is a major contributor to the material budget. Extensive thermo mechanical studies have been conducted with realistic mechanical prototypes (see next section) and hypotheses of work based on the foreseen and now verified power consumption of the electronics on detector and on the environmental conditions (temperature, temperature gradients and irradiation levels). The cases of the outer Si components both in the barrel and the forward regions have been completed.

Tests are based on mechanical prototypes that reproduce the thermal conductivity coefficient of the Carbon fibre and simulate a section of the barrel and of the forward outer Si tracker of about 2 m length and with a structure with alveoli where are located the detectors. The detectors are sitting in drawers that gather each one 4 to 5 ladders. At one end of the drawer, there is cooling water that provides a cooled air convection by wind turbine plus conduction in the alveoli of the support structure

The external temperature is maintained at 35°C. Power dissipation per channel of 400 µWatts and no power cycling are supposed. The goal is to maintain the temperature on the detector at most at 30°C in order to avoid intrinsic noise increase.

Prototype results are used to model the CAD thermal software (SAMCEF).
The obtained results (see Figure 31) shows that even with air cooled with water at 19°C, at 2 m from the source of air cooling, the temperature on detector is maintained at about 30°C. And an important remark is that what really matters is the environmental temperature. We took it to be of the order of 35°C as educated guess.

Figure 31: Evolution of the temperature on the detector along the overall detector length, i.e. as a function of the distance with respect to the source of air cooling. The maximal distance is 2m in this present test.



The main conclusions from this study is that for the outer parts of the Si tracking system both in the central and forward regions, the cooling is not really an issue, in the ILC environmental case. The main parameter is the external temperature mainly driven by what the other detector sub systems are providing as power dissipation.

The case is a bit touchier when considering the innermost components. A careful study of the cooling in this case is just starting now.

4.3 Design and construction of prototypes

Several types of prototypes have been already built in the SiLC collaborations. They include:

- The basic element prototypes, i.e.: ladders with several sensors bonded together are submitted to tests on Lab test benches. One long ladder prototype with variable length of strips was built by Geneva University and intensively test in Paris (see Fig 1 page 5).

Another one is under construction with new types of sensors in Paris. UCSC and FNAL intend to build one such prototype soon.

- Mechanical prototypes for the thermo mechanical studies: several such prototypes have been built at LPNHE, and Figure 32 shows a photograph of one of these prototypes, actually a sector of the external forward detector in full length, in the XUV projection design case. On the left of the Figure 32 is shown the box in which this prototype is maintained under the supposed environmental conditions, namely an external temperature of 35°C.

Fig 32: Prototype of a sector of the outer forward Si tracker in the XUV case; the detectors are inserted in a structure with alveoli as sketched on the right and the air convection and conduction is also as indicated on the right scheme

The cooling study of the inner parts of the Si tracking system is starting now (see Fig.33)

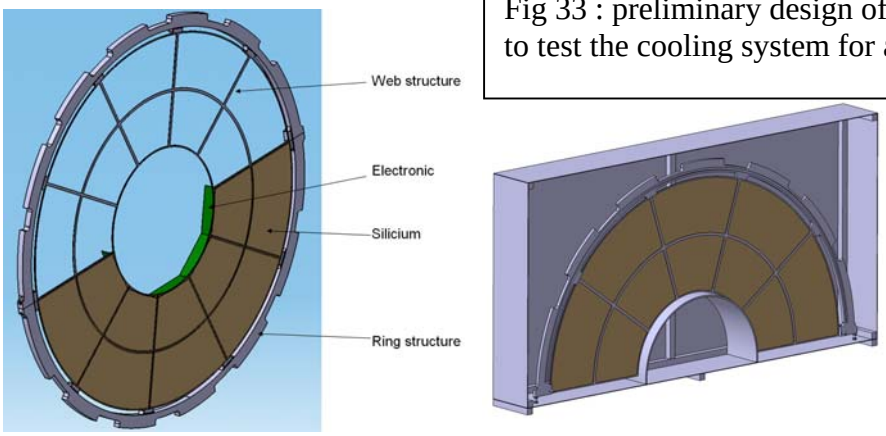


Fig 33 : preliminary design of the mechanical prototype to test the cooling system for a disk of the inner forward

- The other prototypes, under study are those for the test beams (see Section 5.2.3)

5 Developing the main tools

Three main tools are needed in order to pursue these R&D studies: detailed simulations, test set-ups, alignment and calibration tools.

5.1 Simulations

The general task of the simulation and analysis packages is to provide a flexible infrastructure and the needed tools for the development, the validation and the use of the Monte Carlo simulation application in the main simulation frameworks of ILC. These frameworks currently available are: SLIC [13], JUPITER [14] and MOKKA [15] which are GEANT4 based and BRAHMS [16] which is GEANT3 based, but at the present time contains the most complete reconstruction package of all.

The first goal of our simulation activity is to implement the detailed geometry design of the various silicon tracking subsystems presently under consideration within the main simulation frameworks. This is in order to study the performances of each system and to compare them. Currently under consideration are: the SiD baseline tracking system, the LDC and the GLD tracking systems. Our collaboration comprises people that are working in each of these three detector designs and thus all 3 concepts are studied. The study of performances should mainly be based on specific physics processes, which are particularly sensitive to the tracking performances and are those recommended as benchmark physics processes for ILC.

5.1.1 Physics Generators

As mentioned before the detailed study of the silicon tracking sub systems should be based on the specific physics processes which required the benchmark processes and the development of physics generator with interface to the main simulation frameworks. The main physics event generator is PYTHIA 6.2 with an interface in HEP standard. The important features are:

- The Initial State Radiation (ISR) as simulated by PYTHIA,
- The beamstrahlung process which is taken into account by using the CIRCE [17] package. One of the main benchmark physics process is the study of the Standard Model Higgs strahlung process: e+e- -> ZH -> l+l- X with an analysis based on the recoil mass algorithm. This channel is recommended as a benchmark process for ILC for the study of the tracking system performance.

Other physics processes sensitive to the tracking system performance are under study and will be included in the plans of investigation.

5.1.2 Geometry Implementation

The Monte Carlo simulation of the silicon tracking sub detectors for the ILC experiment(s) is based on two main detector concepts: the LDC spectrometer and the simulation framework MOKKA (GEANT 4), and the SiD concept and the simulation framework SLIC (Geant4).

The geometry implementation includes the main silicon tracking sub detectors except the vertex detector. It thus comprise: the internal Si tracker, the internal forward Si tracker, the external Forward Si Tracker and the external barrel Si tracker for the LDC option, and, the internal forward Si tracker, the main barrel Si tracker, the main forward Si tracker for the SiD option.

The detail geometry including support structures and electronics is implemented in the MOKKA MySQL database geometry description for the MOKKA framework. The geometry description of the SiD concept is based on GDML – XML package and is currently being installed.

As an example, the inner Si tracker system including: the inner forward Si tracker and the inner barrel Si tracker together with the vertex tracker (VTD) as described in the MOKKA framework, is presented on the Fig 34. The external barrel Si tracker and the external forward Si tracker surrounding the time projection chamber (TPC) are shown on the Fig. 35.

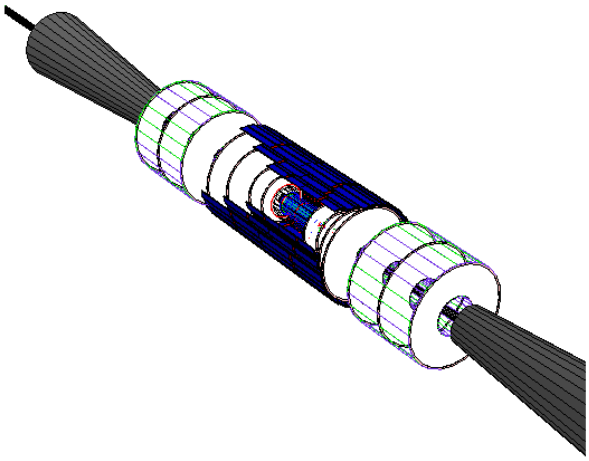


Figure 34: Inner Tracker including the Forward Si disks system and three layers of the Inner barrel Si Tracker

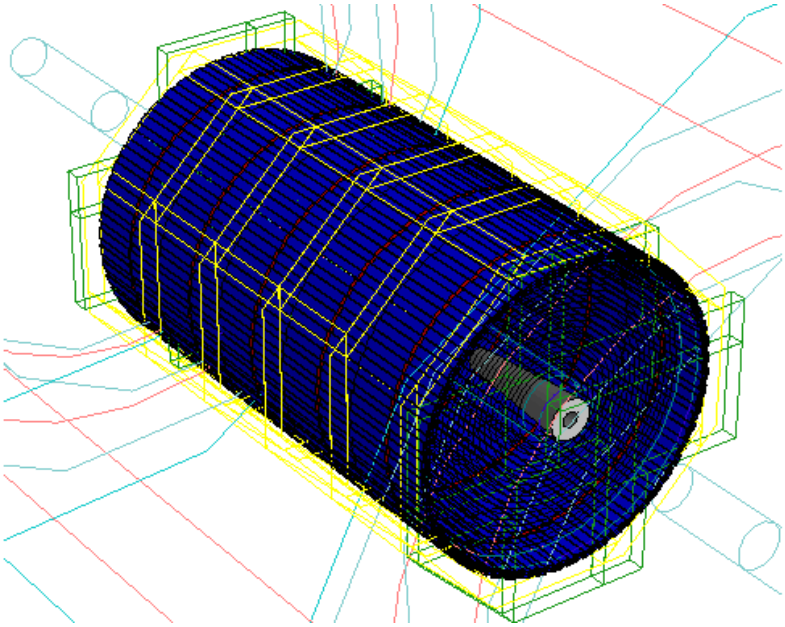


Figure 35: the external barrel and the external forward Si trackers, surrounding the Time Projection Chamber (TPC).

5.1.3 Reconstruction and analysis

The first step is the occupancy study of the Si tracker components. This is in order to precisely determine the optimized dimensions of the basic element of the tracking architecture, i.e. the ladder which includes one or more than one sensor. This study must be performed with the full Monte Carlo simulations in the main ILC simulation frameworks.

More detailed study of the detector and of the physics performances require the complete reconstruction frame. Up to now, only the "old fashion" BRAHMS (Geant3) simulation and reconstruction framework are reliably implemented and thus we intend to perform these studies starting first with BRAHMS .

The reconstruction framework for the GEANT 4 based simulation frameworks is not yet completed. MOKKA GEANT 4 reconstruction and analysis framework is under development. A common effort is underway within the LDC group, in order to release the MARLIN framework, which includes the tracking reconstruction concept from BRAHMS; we intend to take part to it.

The SiD reconstruction framework based on JAVA is also under development and test. It is our intention to use the most up to date reconstruction and analysis frameworks for the detailed study of the Si tracker sub systems, as soon as they will be ready.

5.1.4 Preliminary results

The first look to the physics analysis was realized within the MOKKA (Geant4) framework applied to the study of the Higgsstrahlung process **[18]**.

A statistics corresponding to 500 pb^{-1} was generated and passed through the full simulation framework MOKKA (GEANT4). The tracking includes three external Si layers in addition to the TPC. The goal is to get the mass resolution of the Z at the level of natural width, in order to study the Higgs bosons properties using the recoil mass method. Fig 36 shows the full simulation of the Higgsstrahlung process in MOKKA (GEANT4) framework. The statistical analysis is planned to be performed with MOKKA (GEANT4) output interfaced to the BRAHMS reconstruction and analysis framework using LCIO.

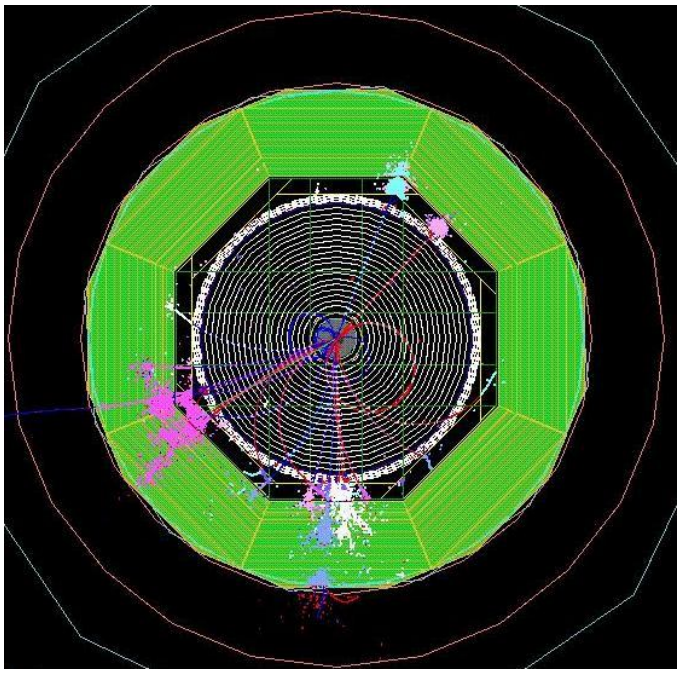


Figure 36: MOKKA event display with the full simulation of the Higgsstrahlung process. Note that the tracking system in the barrel includes an internal silicon tracker, plus an external silicon tracker that surround the central TPC.

*5.1.5 **Plans***

- The first goal is to complete the implementation of the Si tracking sub systems geometry within the full simulation packages for LDC and SiD concepts.
- Then to perform the occupancy analysis with the full simulation in order to optimize the geometry design of the various Si tracking components and disentangle between the need for tiles or longer ladders.
- A real task force should concentrate on including in the GEANT 4 based simulations the full reconstruction if we want to be able to really optimized the LDC and SiD tracking concepts. We will take part to it.
- Last but not least: Physics analysis with dedicated physics channels sensitive to the tracking performance on the overall needed geometric acceptance are going to be performed

5.2 Test setups

5.2.1 Laser test

Laser testing systems are developed in various Laboratories that are part of the SiLC collaboration. At the Paris test bench the laser system is used to test both the detector prototypes and the prototypes of the new F.E. electronics. Prague has also such a facility; Paris and Prague are developing a collaborative effort for cross-checking and exchanging measurements.

A similar facility was developed at the University of Geneva for the AMS experiment and served to test the sensors and the first long strip prototype once it was built and before being installed in the Paris test bench. These tests at the Geneva University, demonstrated the good functioning of the newly built prototype both from the sensors and the connected F.E. electronics point of views.

The principle of functioning of the laser test is as follows:

Here a focused laser beam with 5 micron spot size. Both 660 and 1060 nm wavelength can be used. These two wavelengths differ significantly in a penetration depth in silicon and so they can provide us with different view of the process (see Figure 37 here below)

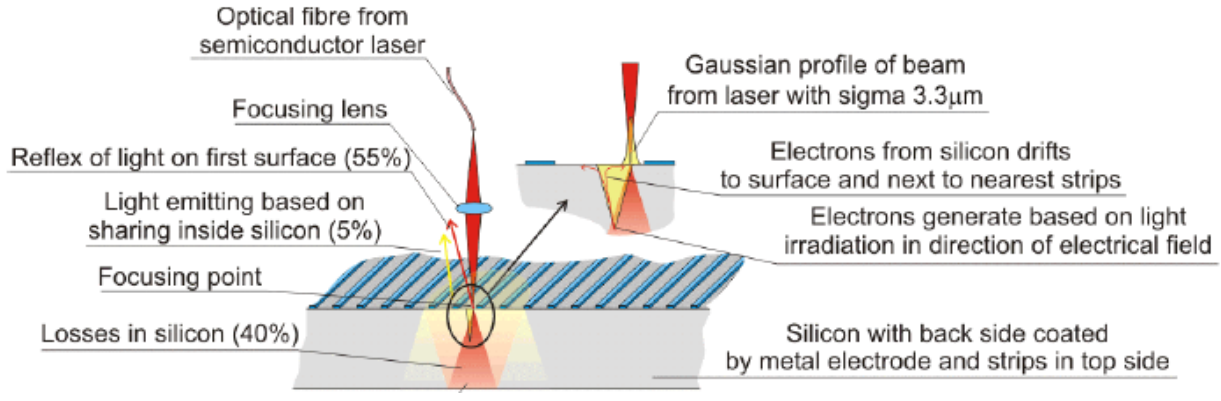


Fig 37: Sketch of the Laser diode IR collimated light stimulating Si detector

Due to its excellent position definition, this laser provides important information on silicon response to this light, charge sharing, etc… It has been shown in subsections 2.1 and 2.3, how this source is used for measuring Si detector characteristics on the Lab test bench.

5.2.2 Radioactive source test

Tests with radioactive source (Sr90) can complement laser tests described above. Here the spatial resolution is not known, but for signal-to-noise measurement one needs a signal from a real particle close to the spectroscopy chain, as sketched in Figure 38 here below.

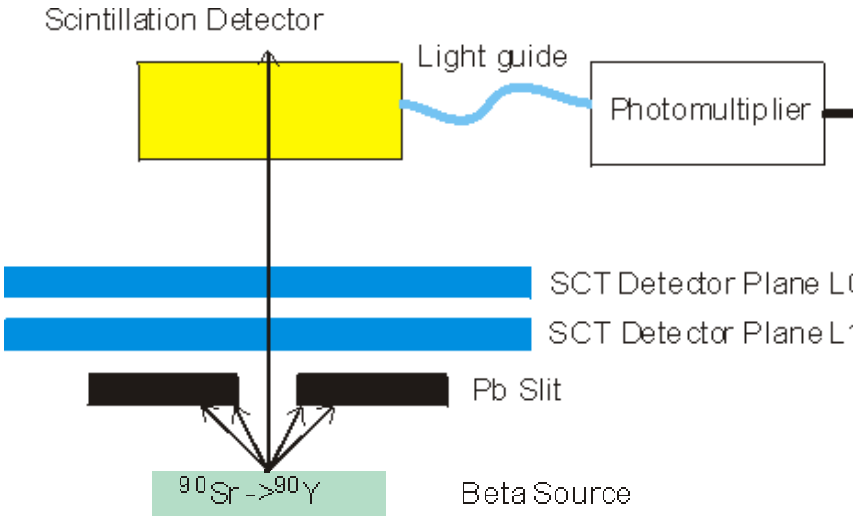


Fig 38: Sketch of a test set up on a Lab test bench using a radioactive source for stimulating the Si detector to be tested.

As an example, Fig.39 shows a photograph of the Lab test bench in Paris where are ongoing the measurements on the long strips reported in section 2.1. Also a similar system is set up for the test presented by the Korean team on new sensors (see section 2.3). In both Labs the measurements of the signal to noise ratio on Si detectors have been obtained in this way.

Fig 39 Photograph of the Lab test set up in Paris, the long ladder prototype is installed in a Faraday cage, on a 3D motorised table and is excited by a LD1060 nm or by a radioactive source. The strips are read out by VA64_hdr front end chips and the test set-up is LabView based.

5.2.3 Test beams

Test beam is an essential tool to evaluate properly the performances of detectors in terms of their designed functionality: detecting particles. For position sensitive strip detector modules the following parameters need to be determined using accelerated particle beams:

- detection efficiency vs. operational parameters
- Landau spectrum, signal amplitude
- spatial resolution
- signal-to-noise determination
- cluster size (number of hit strips)
- pulse shape
- bias scans
- angular scans
- Lorenz angle determination

In addition to these physical parameters, test beam measurements provide also important informations on several system aspects (i.e. susceptibility to external noise, crosstalk, synchronisation with other systems, etc.).
Figure 41 shows a typical test beam configuration: a collimated beam of relativistic particles pass through a scintillator leaving signal enabling to trigger the readout system. Then the particle passes through a set of telescopes (strip or pixel detectors) which determine the exact position of the beam particle. Signals from the device under test (DUT) placed usually in between the telescopes are analysed, and if the signal comes from the sensor close to the measured particle track, this is counted as an efficient hit. Events with no hit or a hit far from the beam, are counted as inefficient.
Extensive beam tests of SiLC prototypes are planned for coming years. As the operation of all systems is quite expensive and requires large amount of manpower, common beam tests of several groups is foreseen. SiLC is preparing for a test beam in standard beam test facility at DESY for fall 2006 and later at CERN and FNAL.

A prototype of a part of a Si tracker is under study and design in Paris. It is intended to submit it to the electron beam in DESY and to have the possibility to include this prototype within the 5T magnet in order to be able to also study its effect on the spread of the signal, and thus to complete the full to do list given at the beginning of this section. The foreseen date is sometime in the last trimester of 2006.

Besides it is our intention also to test, in this test beam session, the new FE chips that both SCIPP-UCSC and LPNHE will have hopefully produced to equip of the order of at least 1K channels each.

For this test, a preliminary sketch of the alignment system will be implemented too. The detector will be sitting on a 3D table that will allow to perform angular scans. This overall effort is starting to be organized and set-up.

Figure 40 shows the preliminary design of the prototype under study for this test beam. It is a part of a forward detector in the projective case. It is made of two layers one that will comprise two sectors according to what was described in the section 4.1.4 (see Figure 28), and the one behind that will be made of only one sector but covering half of the two previous ones. It will be on a structure that will allow an angular scan of the detector, as shown on Figure 40. It will represent a few thousands channels to be read out.

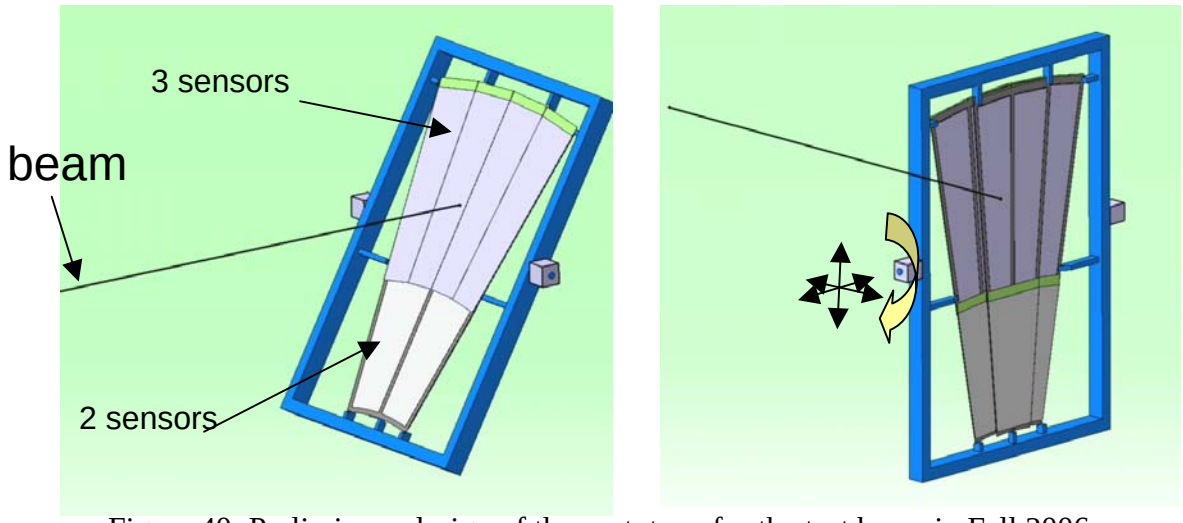


Figure 40: Preliminary design of the prototype for the test beam in Fall 2006

It is also foreseen to test long strips prototype in this same test beam.
This will be a joint effort of the overall SiLC collaboration and also a group from FNAL has expressed interest in joining this effort.

In the longer term future it is intended to have combined test beams with other sub detectors. And we are already starting to study also these possibilities.

SiLC is also preparing a common beam tests with DEPFET project (Bonn, Mannheim, Munich) both at Bonn University (electron synchrotron ELSA providing electron beam up to 3.6 GeV).
Prague group will adapt their track fitting and alignment software system for both groups. The first beam test in Bonn is foreseen for the 3rd quarter of 2005

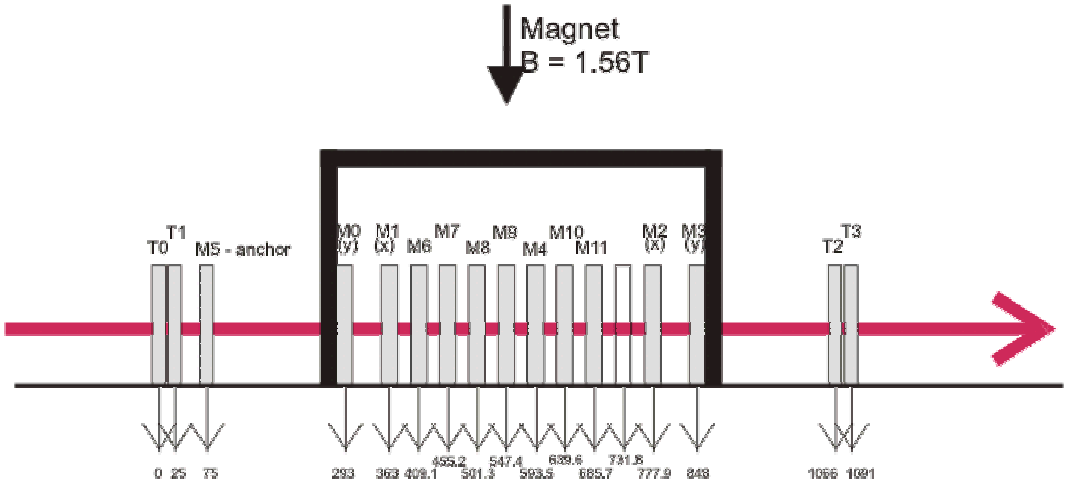


Figure 41: Sketch of the test setup with DEPFET

5.3 Alignment

In order to ensure the performances of the Silicon tracking system in an ILC experiment, one crucial key issue is the alignment. Two teams are presently working on solutions to this tricky problem.

5.3.1 Frequency Scanned Interferometry for ILC Tracker Alignment

The group from the University of Michigan is studying a tracker alignment system based on frequency scanned interferometry.The motivation for this project is to design a novel optical system for quasi-real time alignment of tracker detector elements used in the ILC detector. Current plans for future detectors require a spatial resolution for signals from a tracker detector, such as a silicon microstrip or silicon drift detector, to be approximately 7-10 microns [19]. To achieve this required spatial resolution, the measurement precision of absolute distance changes of tracker elements in one dimension should be on the order of 1 micron. Simultaneous measurements from hundreds of interferometers will be used to determine the 3-dimensional positions of the tracker elements.

The University of Michigan group constructed two demonstration Frequency Scanned Interferometer (FSI) systems with laser beam transported by air or single-mode optical fiber in the laboratory for initial feasibility studies. Absolute distance was determined by counting the interference fringes produced while scanning the laser frequency. The main goal of the demonstration systems was to determine the potential accuracy of absolute distance measurements that could be achieved under controlled conditions. Secondary goals included estimating the effects of vibrations and studying error sources crucial to the absolute distance accuracy.

5.3.1.1 Demonstration System of FSI

A schematic of the FSI system with a pair of optical fibres is shown in Fig.42. The light source is a New Focus Velocity 6308 tuneable laser (665.1 nm - 675.2 nm). A high-finesse (>200) Thorlabs SA200 F-P is used to measure the frequency range scanned by the laser. The free spectral range (FSR) of two adjacent F-P peaks is 1.5 GHz, which corresponds to 0.002 nm. A Faraday Isolator was used to reject light reflected back into the lasing cavity. The laser beam was coupled into a single-mode optical fibre with a fibre coupler. Data acquisition is based on a National Instruments DAQ card capable of simultaneously sampling 4 channels at a rate of 5 MS/s/ch with a precision of 12-bits. Omega thermistors with a tolerance of 0.02 K and a precision of 0.01 mK are used to monitor temperature. The apparatus is supported on a damped Newport optical table.

In order to reduce air flow and temperature fluctuations, a transparent plastic box was constructed on top of the optical table. PVC pipes were installed to shield the volume of air surrounding the laser beam. Inside the PVC pipes, the typical standard deviation of 20 temperature measurements was about 0.5 mK. Temperature fluctuations were suppressed by a factor of approximately 100 by employing the plastic box and PVC pipes.

The beam intensity coupled into the return optical fibre is very weak, requiring ultra-sensitive photo-detectors for detection. Considering the limited laser beam intensity and the need to split into many beams to serve a set of interferometers, it is vital to increase the geometrical efficiency. To this end, a collimator is built by placing an optical fibre in a ferrule (1mm diameter) and gluing one end of the optical fibre to a GRIN lens. The GRIN lens is a 0.25 pitch lens with 0.46 numerical aperture, 1 mm diameter and 2.58 mm length which is optimized for a wavelength of 630 nm. The density of the outgoing beam from the optical fibre is increased by a factor of approximately 1000 by using a GRIN lens. The return beams are received by another optical fibre and amplified by a Si femtowatt photoreceiver with a gain of $2*10^{10}$ V/A.

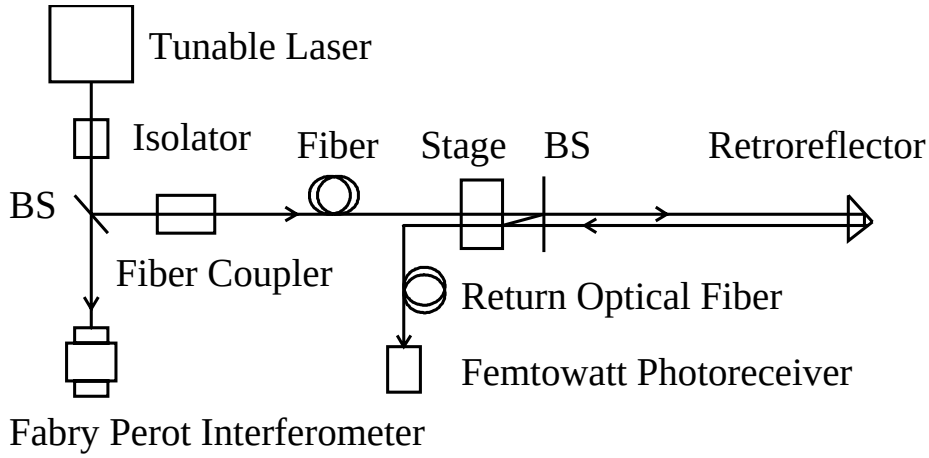


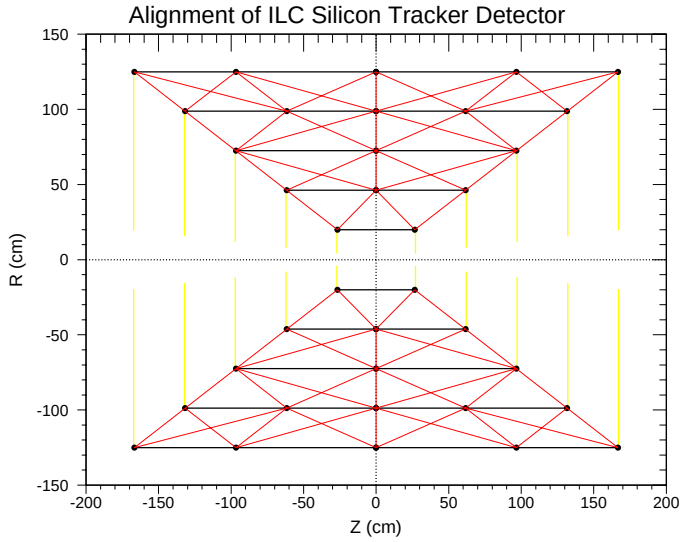
Fig.42. Schematic of an optical fibre FSI system.

5.3.1.2 Results

Absolute distance measurement precisions of approximately 50 nm for distances ranging from 10 cm to 70 cm under laboratory conditions were achieved using the new multiple-distance-measurement analysis technique. Vibration frequencies ranging from 0.1 Hz to 100 Hz with minimal amplitude of a few nanometers can be extracted precisely using the presented analysis technique [20]. Work is underway to apply similar techniques to a dual-laser interferometer, in order to achieve comparable precision under realistic detector conditions [21].

5.3.1.3 A Possible Tracker Alignment System for ILC Silicon tracker

One possible Silicon tracker alignment system is shown in Fig.43, with top plot for alignment in R-Z plane of the tracker barrel, middle plot for alignment in X-Y plane of the tracker barrel, bottom plot for alignment in the tracker forward region. Red lines/dots show the point-to-point distances need to be measured using FSIs. There are 752 point-to-point distance measurements in total for the alignment system. More studies are needed to optimize the distance measurements grid.



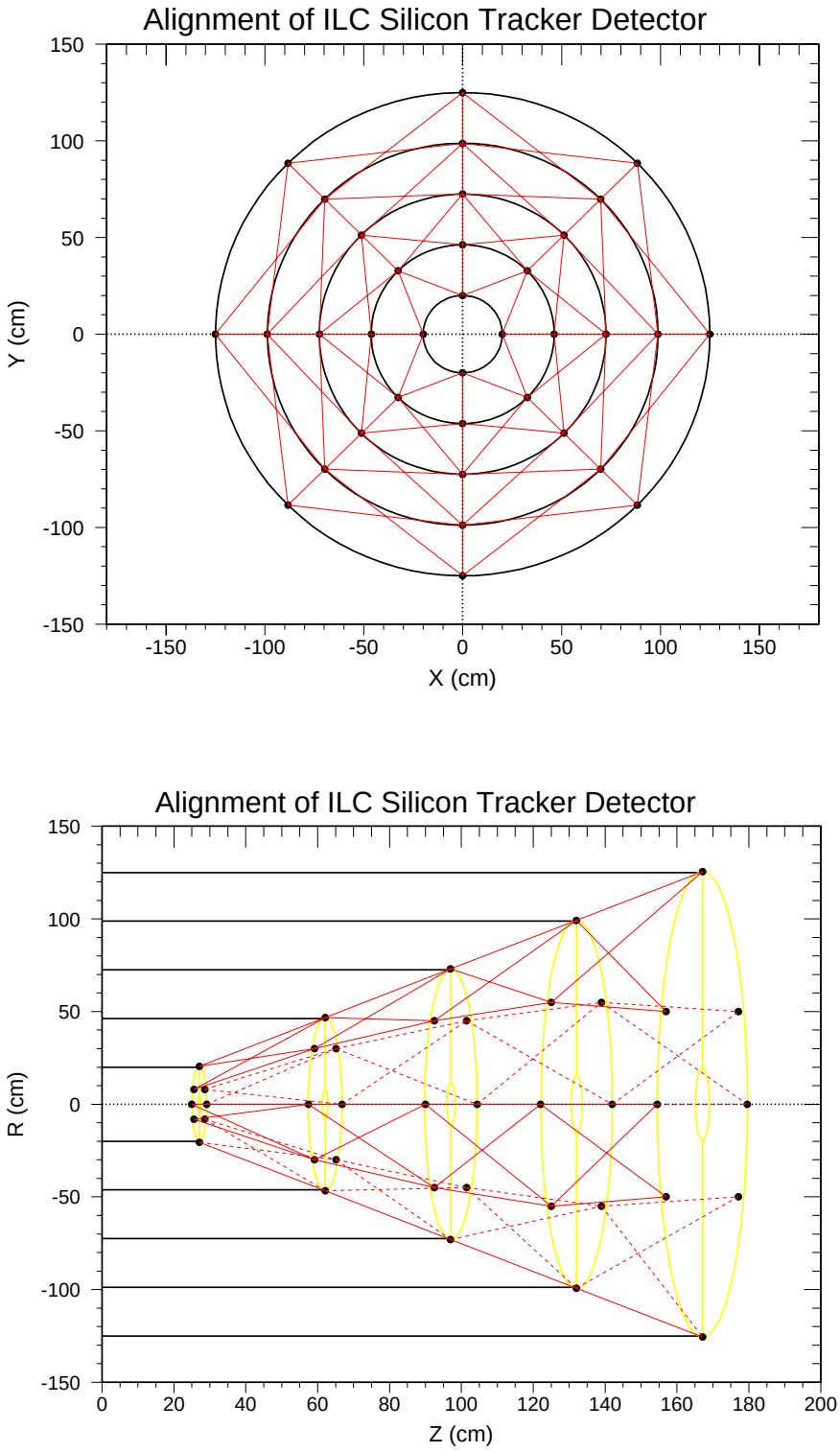


Fig.43: A Possible ILC Silicon Tracker Alignment System.

5.3.2 Hybrid approach: Integrated co-linearity monitors and offline track alignment.

The usual limiting factors in the accuracy of a position monitoring system based on opto-mechanical devices are: *mechanical transfers*, between the monitored imaging sensors and the active particle tracking elements; and *non-strait propagation* of the reference laser lines; quite

often, extremely precise position monitoring systems suffer from poor accuracy due to the previous two factors. The approach that the Cantabria University group propose here below will solve the first issue and reduce the effect of the second one.

Concept for the alignment of the silicon system.

This conceptual design is built on its successfully application to the AMS-1 [22] tracking system, and on the current developments for the CMS silicon tracker alignment. The main features of the proposed concept are the following:

- Collimated laser beam (IR spectrum) going through silicon detector modules. The laser beam would be detected directly in the Si-modules. The alignment readout is fully integrated in the silicon readout; tracks and laser beam share the same sensors removing the need of any *mechanical transfer*.
- No external reference structures. All the elements of the alignment system (laser beam collimators, steering optics, etc.) are mounted directly on the tracker elements.
- No precise positioning of the aiming of the collimators. The number of measurements has to be redundant enough to reconstruct the detector without any knowledge of the laser beam initial parameters.
- Optical and tracking data will be *combined* to optimise the alignment procedure.
- A minimal impact of the alignment system on the layout of the tracker and its production technology.
- Based on previous AMS-1 experience we can project that few microns resolutions would be achieved.

Gaussian laser beams and Si-sensor treatment

From the point of view of the instrumentation, the two key stones of this hybrid approach to the tracker alignment are: non-magnetic hard-rad fibre collimators, delivering a extremely pure gaussian beam; and the anti-reflecting coating of the Si-modules for increasing sensor transparency. The first issue has been already solved in the context of the CMS global alignment for visible light, custom-made titanium collimators with a fused silica optical system deliver almost pure gaussian beams; here, we need to modify the optics design for the IR range. Concerning the Si-modules, a dedicated test stand will be built for the optical characterization of the Si-modules, testing the sensor coatings and treatments. The sensor coating will reduce its reflectivity, increase the transmittance and suppress the deflection of the beam after traversing the Si-module; the testing procedure is very well understood since we have carried out it extensively on semitransparent amorphous silicon sensor developed for the CMS alignment [23].

6 The main R&D aims for the Future

Here below is a preliminary list of the main R&D aims to be pursued by the collaboration in the next future and the people presently involved in those different aspects.

- **Sensors**: towards 8 inches.

  SiLC collaboration gathers several Labs and Institutes which have expertise in the domain (Korean Institutes, Helsinki, IMB-CSIC) as well as Labs that have the infrastructure and expertise for a detailed characterization of the sensor characteristics (the previously mentioned Labs plus IHEP Vienna and IEKP Karlsruhe for instance). In

addition most of all the other Labs are equipped and have expertise in Lab test bench to measure the performances of detectors with Laser diode and sources.

This potential should be used to help getting at least 8 inches wafers. The final production line should be of course done by industrial firm(s).

- **Electronics:**

- Get the LPNHE and SCIPP chips, fully functional and ready to (partly) equip the test beam.

Currently only LPNHE and SCIPP-UCSC are involved in this electronics R&D, but this doesn't prevent other interested labs or people to join the effort in particular for the treatment of the digitized signals at the readout upper level.

- Start working on connectics, packaging and cabling issues (several Labs are interested among which IMB-CSIC which has a good expertise in the domain).

- **Mechanics**:
  - Full design of the SiD, LDC and GLD Si-tracker systems (baseline and a few other alternatives)

    Up to now LPNHE has been performing most of the mechanical studies presented here. New teams are willing to join the effort.
  - Build detector prototype(s) for test beams
  - Perform cooling studies for the inner Si detectors (barrel plus forward)
  - Develop expertise in constructing the basic element and the needed Carbone fiber structures.
- Get the full **GEANT4 based simulation package,** as user, for studying detector designs, performances and related physics studies (Obninsk, UCSC, Tokyo University, LPNHE, in collaboration with SLAC and DESY simulation developers).
- Develop a realistic **alignment and calibration** framework (Michigan University and Cantabria University)
- Perform **tests beam** studies. (All)

7 The collaboration and Financial Support

These last two years the SiLC collaboration has been developing around a "hard core" of teams and people that acted as an "avant garde". The other Institutes were keeping close contacts and/or bringing some more punctual contributions. This was in particular the case of several Institutes that are part of SiLC but also actively involved in the construction of the LHC (Si trackers or other parts of the experiments). These teams are becoming more and more available and willing to collaborate actively to SiLC.

Besides, because of the positive evolution of the ILC project, more and more groups are willing to invest time and resources to this field and the topic of the SiLC R&D is especially tempting because in all the detector concepts, there is a crucial need for Si trackers. And the Si trackers for the ILC must have even better performances than the ones presently under construction or already running. A lot of improvements and breakthrough have still to be accomplished !

For all these reasons, it is expected that these next two years the involvement of people and Institutions in SiLC will be still growing as well as the allocated resources.

Concerning the financial support, we all have been relying on funds provided by our national funding agencies. At the start of the preparation for test beams, implying building realistic prototypes of detectors and new highly performing F.E. and readout electronics, the cost is becoming an order of magnitude higher. Money will be one of the crucial issue for allowing the good development or not of this R&D program.

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