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Project: CMOS sensor based Vertex Detector for the ILC
Status Report

Development of Swift and Slim CMOS Sensors for a Vertex Detector at the International Linear Collider

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Abstract

CMOS sensors are being developed to equip a vertex detector offering the perfomances required for the physics programme at the International Linear Collider. The progress realised from Spring 2005 to Spring 2007 is exposed in this report. It addresses mainly the design of fast integrated signal processing micro-circuits. Besides this main issue, efforts were made to further improve the tolerance to ionising radiation at room temperature and the reliability of the industrial thinning procedure. The exploration of fabrication technologies was continued and some new results were obtained on the tolerance to non-ionising radiation.

The optimisation of the geometry of a high precision vertex detector best adapted to the running conditions near the ILC interaction point was also extended, keeping in mind that the dominant beam background (due to beamstrahlung) is subject to large uncertainties. Overall, the ambitionned performances of the detector should allow to cope with a background rate exceeding substantially the Monte-Carlo predictions. The requirements underlying the development of CMOS sensors in terms of read-out speed and radiation tolerance are therefore more severe than those targetted with other technologies developed for the ILC vertex detector.

Contents:

1 Introduction

CMOS sensors of the MIMOSA[1] series are being developed since 1999 for the ILC vertex detector [1]. The main outcome of the R&D until early 2005 was summarised at the PRC session of May 2005 [2], where the established detection performances were shown to match several requirements of the ILC vertex detector. The best performances were obtained with sensors manufactured in the AMS-0.35μm OPTO technology, which has become the baseline process for the continuation of the development.

Since May 2005, substantial progress was achieved in several areas. Remarkable test results were obtained with a fast read-out prototype featuring integrated signal discrimination and with a prototype designed to be tolerant to ionising radiation at room temperature. The latter is actually part of the development of a sensor dedicated to the STAR vertex detector upgrade [4] and will also lead to sensors equipping the beam telescope of a facility supported by the E.U. [5]. Prominent aspects of all these achievements are summarised in this report.

Progress was also achieved in other R&D areas (e.g. characterisation of fabrication technologies, industrial thinning, power cycling). The most significant outcomes of these activities will be summarised.

The vertex detector geometry taking best advantage of CMOS sensors differs slightly from the one usually considered for CCDs or DEPFETs (described in the TESLA Technical Design Report [6]). The optimisation of the geometry based on CMOS sensor is guided by the possibility to cope with a background rate exceeding substantially the Monte-Carlo predictions, which are subject to sizeable uncertainties. The background evaluation and the prominent features of the vertex detector geometry were exposed in the 2005 PRC report [2], together with the estimate of the hit rate due to beamstrahlung $e^{\pm}$. These results, which influence dominantly the requirements the sensors have to meet, are not repeated in this report, which contains only a brief summary of the most relevant progress achieved in this area during the last two years. More details on the studies performed may be found in [7] and references therein.

The development of the sensors addresses numerous different topics. The latter are shared between several prototypes, each concentrating on a small sub-sample of the list of topics. A summary of the main features of the prototypes mentionned in this report is provided in the Appendices available at the end of the document.

2 Sensors with integrated fast read-out architecture

The rate of beamstrahlung electrons will determine the occupancy in all layers of the vertex detector, with particularly demanding constraints on the two inner ones [3]. In order to cope with the high rate expected in these two layers, the ambitionned frame read-out time was set to 25 (respectively 50) μs in the inner most (respectively second) layer. These target values, which are more ambitious than those indicated in the TESLA TDR, should allow for nominal impact parameter resolution even if the background rates come out to be a factor of 3 to 5 above the value derived from present Monte-Carlo simulations.

In ordre to achieve the short read-out times ambitionned, the sensors are subdivided into columns of pixels read out in parallel. Inside each column, the pixels are read out sequentially. The pixel read-out frequency foreseen is 10 MHz (typically 16 clock cycles at 160 MHz inside

[1] standing for Minimum Ionising MOS Active pixel sensor.

each pixel). The two inner most layers would host sensors with columns made of $\gtrsim 256$ and 512 pixels, translating into read-out times of ~ 26 and 51 μs respectively.

The development of the sensors is based on three work packages addressed in parallel, and sharing the analog, mixed and digital parts of the sensors:

- WP-1: development of a fast, column parallel, architecture, which encompasses the sensing elements, the analog micro-circuits integrated in the pixel and at the column end, as well as the discriminating logic ending each column;
- WP-2: development of a 4-5 bit ADC foreseen to be integrated at the end of each column (replacing the discriminator developed in WP-1);
- WP-3: development of sparsification micro-circuits to be integrated on the chip periphery, and complemented with output memories.

2.1 Development of a fast column parallel architecture

2.1.1 The MIMOSA-8 prototype

a) Main features of the sensor: Most of the R&D effort on MIMOSA sensors addresses the read-out speed issue and the related data flow reduction micro-circuits to be integrated on the sensor. An important step was achieved with the MIMOSA-8 prototype (fabricated in TSMC-0.25μm technology), which provides digitised discriminated outputs. It features 32 columns of 128 pixels (25 μm pitch) read out in parallel, out of which 24 are equipped with an integrated discriminator, while the remaining 8 columns deliver an analog output. Pedestal subtraction is performed before discriminating the signals with the help of correlated-double-sampling (CDS) micro-circuits integrated in each pixel, complemented with double sampling (Fixed Pattern Noise subtraction) at the end of each column [8]. Some main features of this prototype are summarised in Table 1.

Fabrication technology	TSMC-0.25
Thickness of epitaxial layer:	$\lesssim 7$ μm
Nb of columns:	32, out of which 24 equipped with discriminator
Nb of pixels per column:	128 (= number of rows)
Pixel pitch:	25 μm
Nb of sub-arrays:	4 (32 rows each)
Specificity of sub-array 1:	sensing diode of 1.2x1.2 μm^2, clamping architecture
Specificity of sub-array 2:	sensing diode of 1.7x1.7 μm^2, clamping architecture
Specificity of sub-array 3:	sensing diode of 2.4x2.4 μm^2, clamping architecture
Specificity of sub-array 4:	alternative amplification architecture
Read-out clock frequency:	nominal value 100 MHz
Row read-out frequency:	nominal value ~ 6 MHz

Table 1: Prominent features of the MIMOSA-8 sensor.

b) Laboratory tests results: Several sensors were tested and calibrated with an ^{55}Fe source. Besides determining the charge-to-voltage conversion gain, a major goal of these tests consisted in assessing the operation of the 24 integrated discriminators. This was performed

by looking at the sensor outputs while varying the discriminator thresholds. This test was repeated with and without illuminating the sensor. The results are shown in figure 1.

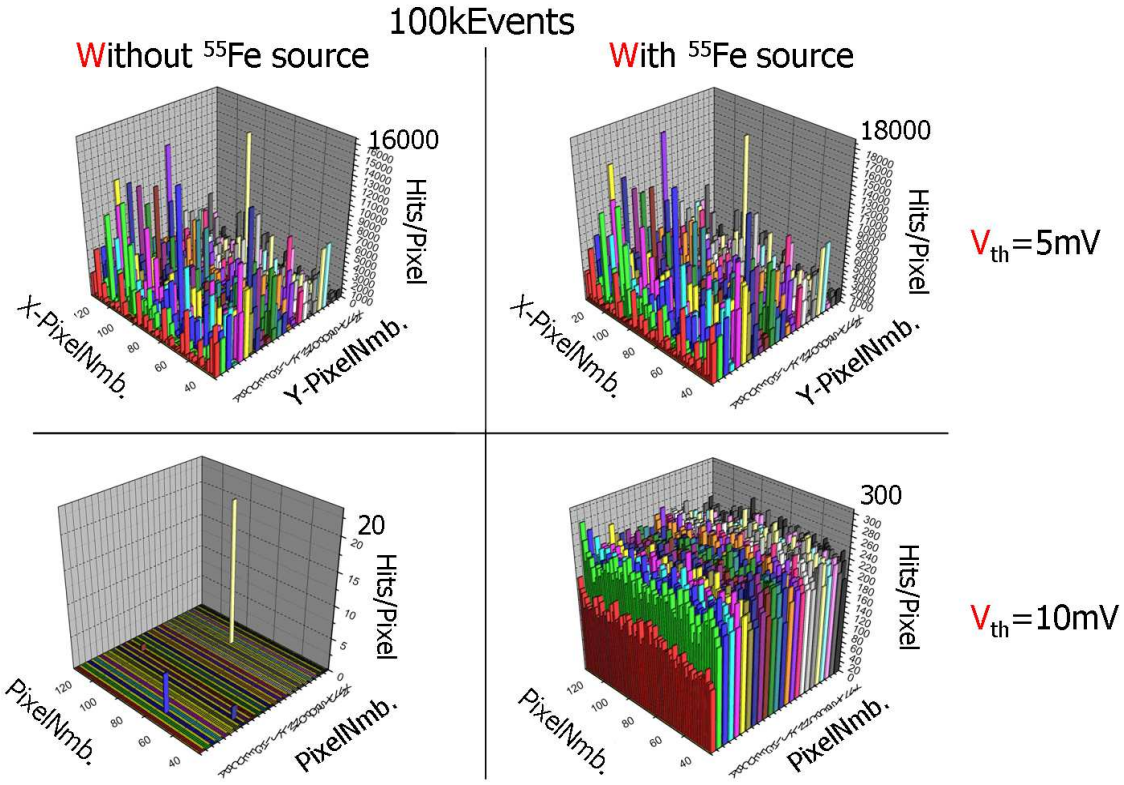


Figure 1: MIMOSA-8 tests with ^{55}Fe source: variation of the number of pixels passing the discriminator threshold over the array of 24 columns (each made of 128 pixels), for two different values of the discriminator threshold voltage (top: 5 mV ; bottom: 10 mV). Figures on the left hand side were obtained without illuminating the sensor, while those on the right show how the sensor behaves when being illuminated.

One observes that all pixels fire when the discriminator threshold is set to 5 mV, whether illuminated with the source or not. Once the threshold is ramped up to 10 mV, very few, isolated, (i.e. noisy) pixels still pass the threshold in absence of the source, while all pixels continue firing when the source illuminates the sensor. The chip is thus working as expected. Moreover, the uniformity of the 24 thresholds was evaluated. It corresponds to less than 1 mV noise, and affects therefore only marginally the signal discrimination, which is typically set at a few millivolts.

c) Beam tests results: Next, some sensors were mounted on a beam telescope made of 4 pairs of Si-strip detectors and installed on a $\sim$ 5 GeV e$^-$ beam at DESY. The operation of the sensor on beam could only be verified up to a row read-out frequency $\gtrsim$ 2.5 MHz (i.e. about a quarter of the target value) because of data acquisition limitations.

The noise of the signal after CDS was measured to be less than 15 e$^-$ENC. The detection efficiency derived from the discriminated data collected with the telescope amounts to 99.3 $\pm$ 0.1 % for an average discriminator threshold equivalent to slightly more than 3 times the noise.

The corresponding fake hit rate was found to be $\sim 10^{-3}$ only (see figure 2). This achievement can be considered as a breakthrough, especially whith regard to the relatively thin epitaxial layer ($< 7\ \mu m$) inherent to the TSMC-0.25 technology.

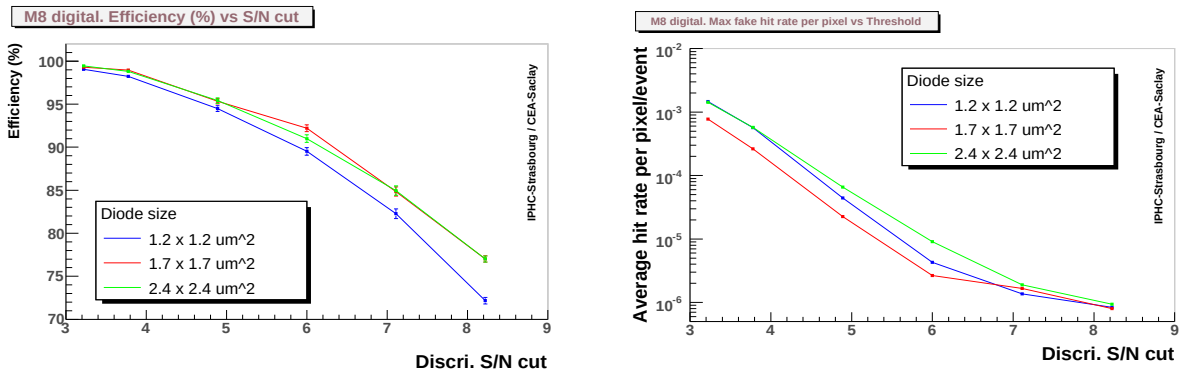


Figure 2: MIMOSA-8 beam tests: detection efficiency (left) and fake hit rate (right) as a function of the discriminator threshold, expressed in terms of signal-to-noise ratio (S/N), for 3 different sensing diode sizes (1.2x1.2, 1.7x1.7, 2.4x2.4 μm^2). The row read-out frequency is 2.5 MHz (equivalent to a clock frequency of 40 MHz).

The single point resolution of the sensor was evaluated in Summer 2006 at the CERN-SPS, with the Si-strip beam telescope mentionned above. A resolution of $\sim$ 7 - 8 μm was found, i.e. about the intrinsic resolution ($\sim$ 7.2 μm) reflecting the pixel pitch (25 μm). This result indicates that the replacement of the discriminators with ADCs featuring very few bits will be sufficient to satisfy the requirements of the ILC vertex detector (typically $\lesssim 3\ \mu m$ single point resolution in the inner most layer), keeping in mind that the pixel pitch will also be slightly reduced, to $\sim 20\ \mu m$.

Overall, these tests demonstrate that the chip architecture performs very well and can be extended by replacing each discriminator with a 4-5 bits ADC. On the other hand, the chip should be manufactured in a technology offering a thicker epitaxial layer, in order to ensure a higher S/N ratio. The AMS 0.35 OPTO technology is at present the best candidate, since it offers a $\sim 11\ \mu m$ thick epitaxial layer, which translates into a typical S/N ratio of 20 – 30 (as already measured with prototypes MIMOSA-9, -11 and -14).

2.1.2 Translation of MIMOSA-8 pixels in AMS-0.35: MIMOSA-15

The first step consisted in translating the MIMOSA-8 pixels with integrated CDS (but not yet its columns ended with discriminators) from the TSMC to the AMS technology in order to investigate potential differences in the manufacturing parameters, such as those influencing the residual noise.

The study was performed with the pixels of sub-arrays 2 and 3. The prototype, called MIMOSA-15, was fabricated in Summer 2005 and consecutively tested with an ^{55}Fe source. The observed noise was close to 10 e$^-$ENC, showing that the pixel design was translated successfuly.

The only unexpected result concerned the charge collection efficiency (CCE), which came out to be extremely poor with the smallest diodes (i.e. 1.7x1.7μm^2) and was still rather modest

for the larger (2.4x2.4 μm^2) ones. In this case the CCE was actually found to be $\sim$ 10 % in the seed pixel (while $\gtrsim$ 20 % were expected) and the 3x3 clusters centered on the seed pixel collected only $\sim$ 30 % of the cluster charge (while $\gtrsim$ 70 % were expected).

This is to be compared to the previous sensors (MIMOSA-9, -11, -14) fabricated in the same technology, which did not exhibit a particularly low CCE. Since the sensing diodes integrated in these prototypes were typically 3.4x4.3 μm^2 large, there is a strong suspicion that the P+ doping in the neighbourhood of the sensing N-well diffuses towards the latter and may screen partly the contact surface between the N-well and the P- epitaxial layer. Since the CCE is strongly depending on this surface, small diodes may be much affected by this effect, which may only marginally modify the CCE of larger sensing diodes.

2.1.3 Translation of the full MIMOSA-8 sensor in AMS-0.35: MIMOSA-16

a) Main features of the sensor: The translation of the complete MIMOSA-8 design in the AMS-0.35 OPTO technology was achieved in 2006. Some of the main features of this new prototype, called MIMOSA-16, are listed in Table 2. Three modifications were introduced w.r.t. MIMOSA-8:

- the smallest sensing diode (1.2x1.2 μm^2) was abandonned;
- the pixels of the sub-array composed of 2.4x2.4 μm^2 sensing diodes were modified in order to improve their tolerance to ionising radiation;
- the architecture of sub-array 4 was replaced by a new one, featuring 4.5x4.5 μm^2 sensing diodes and a new amplification design.

Fabrication technology:	AMS-0.35 OPTO
Thickness of epitaxial layer:	$\sim$ 11 μm ("14 μm" option) or $\gtrsim$ 15 μm ("20 μm" option)
Nb of columns:	32, out of which 24 equipped with discriminator
Nb of pixels per column:	128 (= number of rows)
Pixel pitch:	25 μm
Nb of sub-arrays:	4 (32 rows each)
Specificity of sub-array 1:	1.7x1.7 μm^2 sensing diode, clamping architecture
Specificity of sub-array 2:	2.4x2.4 μm^2 sensing diode, clamping architecture
Specificity of sub-array 3:	like sub-array 2 but with radiation tolerant sensing diode
Specificity of sub-array 4:	4.5x4.5 μm^2 sensing diode, alternative amplification architecture
Read-out clock frequency:	nominal value 100 MHz
Row read-out frequency:	nominal value $\sim$ 6 MHz

Table 2: Prominent features of the MIMOSA-16 sensor.

Figure 3 displays the layout of the sensor, with a zoom on the column bottoms hosting the 24 integrated discriminators.

b) Laboratory tests results: The tests of the sensors fabricated with the so-called "20 μm" option started by the end of 2006. They were performed with an ^{55}Fe source, using the signals of the 8 columns with analog output.

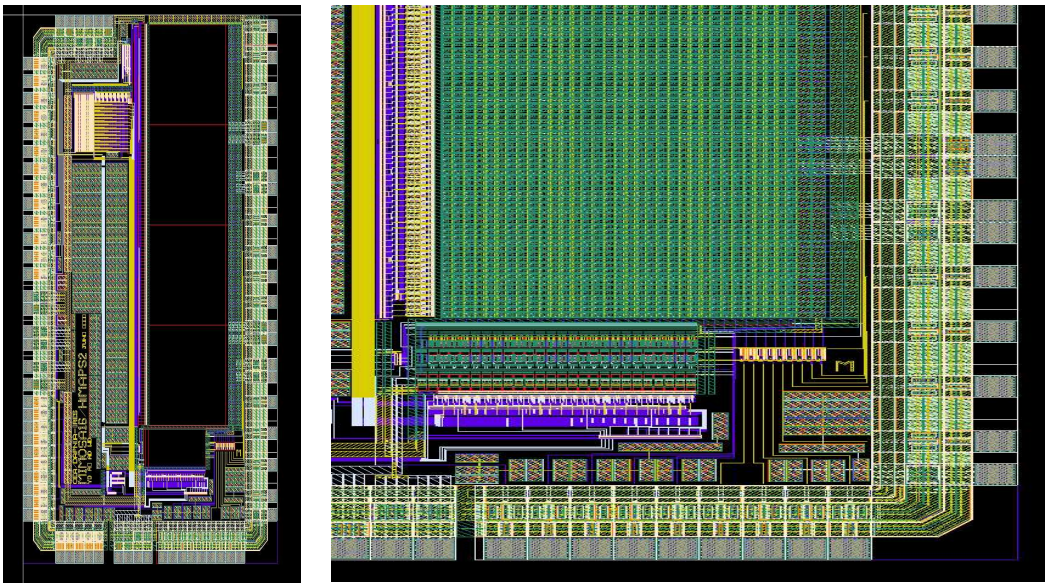


Figure 3: **Left:** Layout of MIMOSA-16 showing the 32 parallel columns, out of which 24 are ended with a comparator, while the other 8 provide an analog output. **Right:** Zoom on the column ends where the 24 discriminators are integrated.

Several parameters were measured as a function of the read-out clock frequency, which was varied from 1 to 150 MHz. The tests were first performed with the sensors fabricated with the "20 μm" epitaxy option. Figure 4 displays the pixel noise, the fixed pattern noise, the pedestal averaged over the columns and the charge collection efficiency (CCE) as a function of the frequency. The CCE is obtained by dividing the total charge collected in a cluster made of 3x3 pixels by the charge accumulated in a single pixel when a 5.9 keV X-Ray hits its depleted volume (it corresponds then to $\sim$ 1640 electrons).

One observes that the pixel noise (top-left) lies within the range expected up to the highest clock frequency values [2] The fixed pattern noise (top-right) adds very little to the pixel noise, as required. The mean pedestal of the columns (bottom-left) does not exhibit any significant feature as a function of the frequency. The situation is less satisfactory as far as the CCE is concerned (bottom-right). It amounts to less than 10 % for sub-array 1 and less than 30 % for sub-arrays 2 and 3. Its value is only acceptable for sub-array 4.

More recent measurements, performed with sensors featuring a "14 μm" epitaxial layer, exhibit a CCE drop which is less pronounced than with the "20 μm" epitaxy. More about this feature is exposed in section 5.

Overall, the conclusion of these measurements is that the next steps of the R&D should be based on the "14 μm" epitaxy rather than the "20 μm" option. Moreover, the dimensions of the sensing diode should be at least $\sim$ 3x3 μm^2. More information on the next steps of the development may be found in section 6.

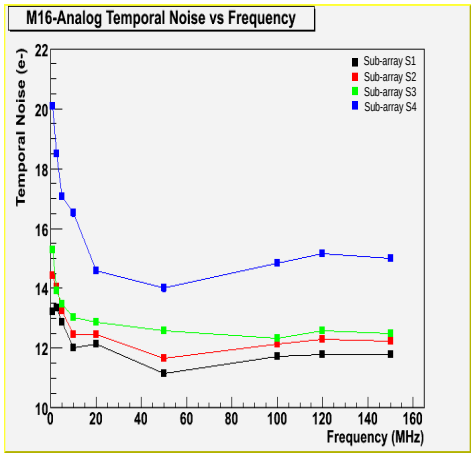
Besides finalising the test of the analog outputs of MIMOSA-16, the characterisation of

[2]The raise at low frequency reflects the usual domination of leakage current induced noise consecutive to long integration times.

Temporal noise vs Frequency

Chip#0 (old mezzanine board)

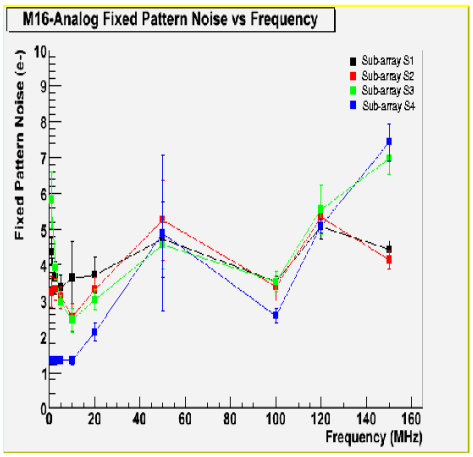
Columns 28-31



FPN (dispersion of pedestal) vs Frequency

Chip#0 (old mezzanine board)

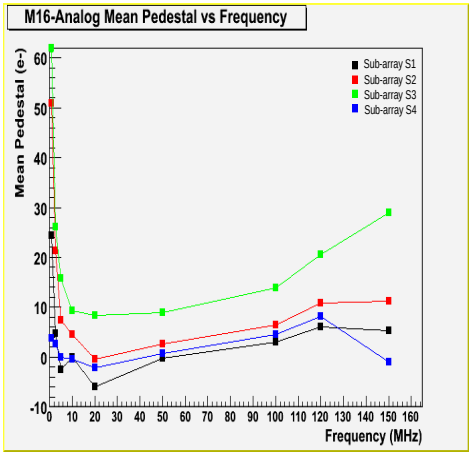
Columns 28-31



Pedestal Mean vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31



Charge Collection Efficiency vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31

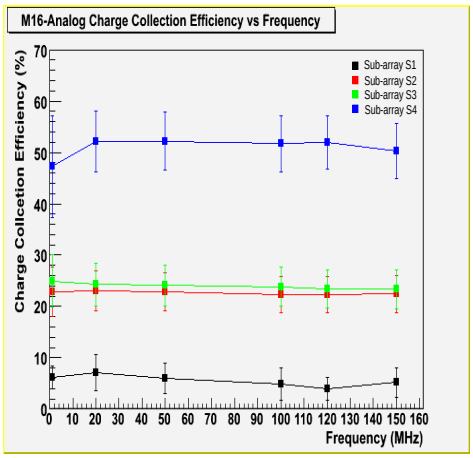


Figure 4: MIMOSA-16 analog output measurements with a ^{55}Fe source, displayed as a function of the read-out clock frequency: pixel noise (top-left), fixed pattern noise (top-right), mean pesdestal (bottom-left) and charge collection efficiency (bottom-right). The sensors were manufactured with the "20 μm" epitaxy option of the AMS-0.35 OPTO process.

the digital outputs remains to be done. It is planned for June 2007 in laboratory with an ^{55}Fe source, and on beam at the CERN-SPS in Septembre 2007.

2.2 Development of fast, low granularity, ADCs

To achieve the required resolution on the impact parameter, the pixels of the inner most layer should provide a single point resolution of $\lesssim 3$ μm. Charge sharing among the CMOS pixels belonging to the same cluster provides a powerful tool to derive a single point resolution much better the digital value associated to the pixel pitch. This is illustrated in figure 5, which shows the single point resolution extracted from real data collected with MIMOSA-9 at the CERN-SPS. This prototype was made of sub-arrays featuring pixel pitches of 20, 30 and 40 μm.

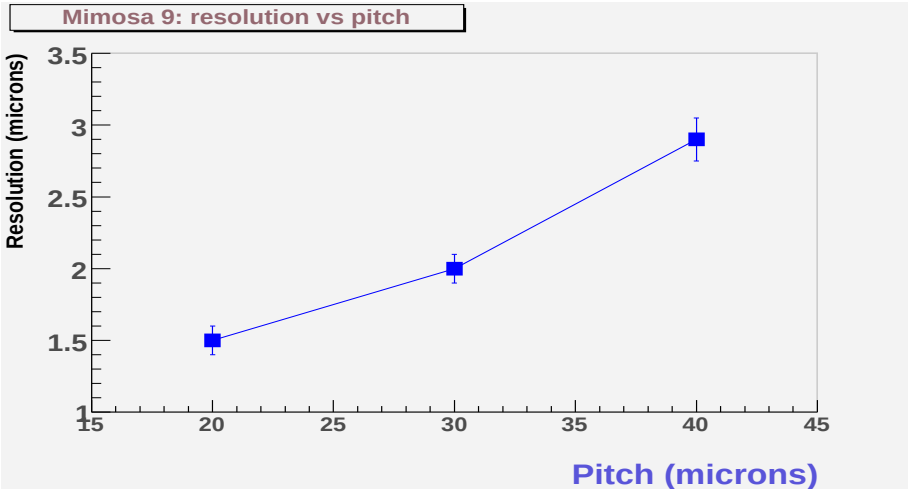


Figure 5: Single point resolution measured at CERN-SPS with the MIMOSA-9 prototype. The measured spatial resolution is displayed for three values of the pixel pitch: 20, 30 and 40 μm.

One observes that 20 μm wide pixels provide 1.5 μm resolution and that 30 μm pixels lead to ~ 2 μm resolution, i.e. values which are much better than the minimal performances required. Since the results were obtained with charges encoded on 12-bit ADCs, there is room left to encode the charges on a much less granular (and thus very compact and fast) ADC. Studies were made in order to evaluate how much the single point resolution degrades as one reduces the number of ADC bits on which the charge is encoded. The study was performed with the real (MIMOSA-9) data used in figure 5, simulating the encoding on 3, 4 and 5 bits. For a 20 μm pitch, resolutions of about 2.1, 1.9 and 1.7 μm were achieved, respectively. Equipping the sensors with ADCs featuring at least 3 (real) bits looks therefore sufficient to provide a resolution close to 2 μm. Accounting for the ADC noise in a conservative way, it was decided to develop 4-bit ADCs to be integrated at the end of each column of the sensor. The developement strategy consists in developing the ADCs independently of the sensors until they are mature enough to replace the discriminators equipping presently the column ends.

Since the ADCs needed for the sensors are very unsual, their design could not be derived from existing - similar - devices. The design requires finding a compromise between a minimal number of (real) bits, an unfriendly aspect ratio ($\sim$ 20x500-1000 μm^2), a high clock frequency (10 MHz) and very limited power dissipation ($\lesssim 500$ μW). It should allow discriminating those pixels which deliver a signal above a given threshold. In order to maximise the chances to

achieve a well performing ADC within reasonable time, the developement was started in 2005 in 4 different laboratories (Clermont-Ferrand, Grenoble, Saclay and Strasbourg), which explored the potential of different ADC architectures: flash, pipe-line, successive approximations (SAR) and Wilkinson.

These different architectures differ mostly in terms of speed versus power dissipation. For instance, a flash or a pipe-line ADC is fast enough to process signals coming from two neighbour columns. Flash ADCs have the tendency to be power consuming, while Wilkinson ADCs consume much less. On the other hand, the latter, just as SAR ADCs, tend to be slow. The architectures developed in each laboratory are summarised below:

- LPSC (Grenoble): amplifier + semi-flash (pipe-line) 5- and 4-bit ADC for a pair of columns (width: 40 μm instead of 20 μm; frequency: 25 MHz instead of 10 MHz);
- LPCC (Clermont): flash 4+1.5-bit ADC for a pair of columns
- DAPNIA (Saclay): amplifier + SAR (4- and) 5-bit ADC
- IPHC (Strasbourg): SAR 4-bit and Wilkinson 4-bit ADCs

The status of each developement is summarised in table 2.2.

Lab	proto.	phase	bits	chan.	$F_{r.o.}$(MHz)	dim. (μm^2)	P_{diss} (μW)	eff. bits	Problems
LPSC	ADC1	tested	5	8	15-25	43x1500	1700	4	Offset & N
	ADC2	fab	4	8	25	40x943	800		
	ADC3	design	4	> 8	25				
LPCC	ADC1	tested	5.5	1	5(T)–10(S)	230x400	20 000	2.5	P_{diss} & bits
	ADC2	fab	5.5	1	10	40x1100	1000		
DAPNIA	ADC1	tested	5	4	4	25x1000	300	$\gtrsim 2$	Missing bits
	ADC2	fab	5	4	4	25x1000	300		
IPHC	ADC1	fab	4	16	10	25x1385	660		
	ADC2	fab	4	16	10	25x1540	545		

Table 3: Summary of the characteristics and status of the different ADCs developed to equip the column ends of MIMOSA sensors. The parameters displayed include the number of bits, the number of channels, the power dissipation per channel, the clock frequency, the effective number of bits and the type of problem encountered during tests.

The most advanced design is the one of the semi-flash/pipe-line ADC developed at LPSC (Grenoble). It is close to match the most demanding requirements: 10 MHz clock frequency per column (twice as much for two columns), $\lesssim 500$ μW power dissipation per column, dimensions of 20 x 500-1000 μm^2 per column. This architecture is expected to translate into a first mature design late in 2007 or early in 2008. It may then be integrated in a sensor (see section 6).

2.3 Development of data compression micro-circuits

The drawback of developing fast sensors adapted to the running conditions close to the interaction point is the high genuine data flow one has to cope with. The read-out rate of the vertex detector generates a genuine data flow in the order of 100 Gbits per cm^2 of sensor. It is therefore mandatory to implement signal filtering functionnalities as close as possible to the

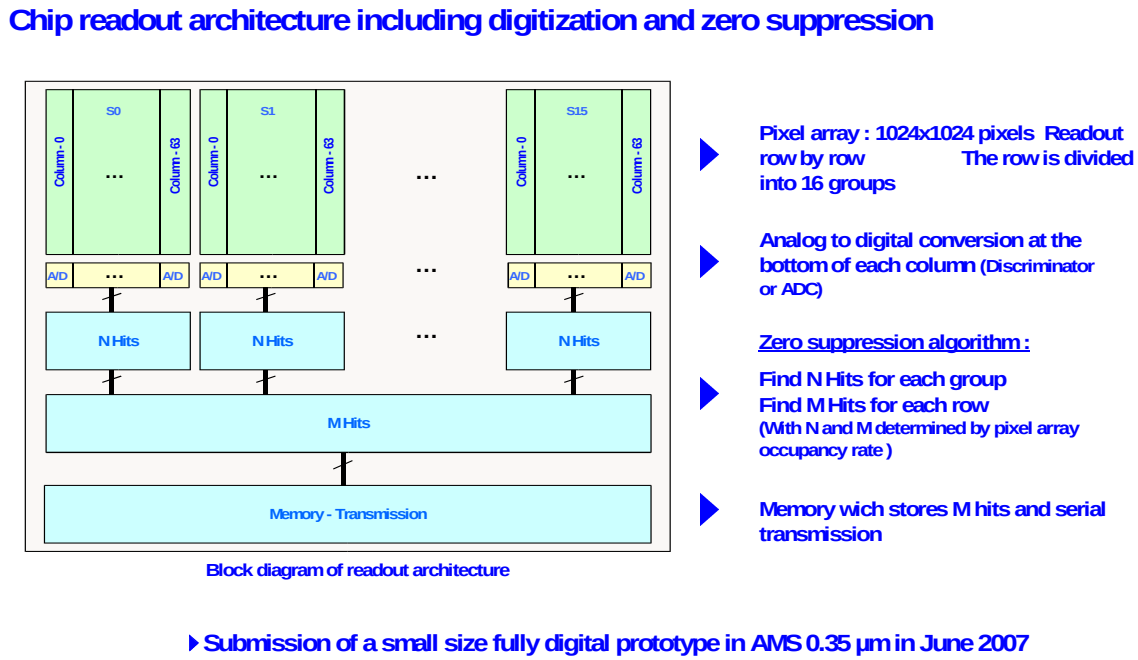


Figure 6: Block diagramme of the zero suppressing SUZE chip.

sensitive area. CMOS sensors are particularly well suited to this type of requirement, as they allow to integrate the necessary sparsification micro-circuits on the sensor itself.

The design of a zero suppression micro-circuit has only started recently. The first prototype (called SUZE-01) is based on a logic adapted to less demanding requirements than those of the ILC vertex detector. It actually fits to those of the beam telescope developed for the E.U. F.P.6 programme EUDET, as well as to those of the Heavy Flavour Tagger (HFT) of the STAR experiment at RHIC (BNL).

The block diagramme of the zero suppression architecture is displayed on figure 6. Its logic consists in filtering pixels which deliver a signal charge above the threshold set in the discriminators. For those selected pixels, it memorises the address of the pixel and transmits it to output memories.

The filtering logic is applied in two steps. The first step addresses groups of 64 columns. Inside each group, the logic scans the row currently being read out, relying on a *token ring* provided by those discriminators where the threshold was passed by a signal. The corresponding pixel gets then flagged with its address inside the row (typically 10 bits), and the number of adjacent pixels with signal above threshold is counted. Up to 4 adjacent pixels can be flagged in this way (on 2 bits). The logic thus provides series of 12-bit words, where the first 10 contain the address of the first pixel of a series, and the 2 remaining bits tell how many adjacent pixels delivered a signal above threshold. This is to minimise the size of the information transmitted, accounting for the fact that the signal is configurated in clusters of several pixels. The logic accepts up to 6 series of pixels inside each group of 64 columns.

The second step of the logic, which treats globally the outputs of all groups of columns, combines the information at the edges of contiguous groups, and keeps up to 9 series of adjacent pixels for the full row. This information is then written in memories, which will consecutively be read out from the external logic steering the detector.

The chip is currently being designed and will be submitted to fabrication by the end of June 2007. Its performances are suited to the EUDET and to the STAR requirements, but not yet to the ILC ones, which are more demanding. Its test results, late in 2007, will settle the ground for an architecture suite to the ILC running conditions.

3 Exploration of fabrication processes

The need to characterise industrial fabrication processes with real sensors is an essential aspect of the development of CMOS sensors for particle tracking. This is because some crucial parameters entering the detection performances (mainly addressing the analog part of the sensor and often related to details of the doping profile) have marginal influence on commercial product's quality (mainly digital micro-circuits). These parameters are therefore often poorly known by the founder, and can only be derived with the required accuracy from tests performed with real sensor prototypes.

3.1 Further evaluation of the AMS-0.35 OPTO technology

The most attractive fabrication technology characterised so far is the AMS-0.35 OPTO process. Excellent tracking performances were obtained with 5 consecutive small prototypes fabricated in this technology since late 2003, which was retained as a baseline for the sensor R&D and for their short term tracking applications (STAR HFT, EUDET beam telescope, demonstrator for the CBM vertex detector [3]).

3.1.1 Operation at room temperature

The latter require operating the sensors at room temperature, a constraint which turns out to be quite demanding for the STAR HFT, where the modest (air) cooling system may let the air temperature grow up to 30°C or even more. The sensitivity of the sensor detection efficiency to the temperature was assessed with the MIMOSA-9 prototype. For this purpose, several sensors were mounted on a Si-strip telescope and data were collected at DESY with an electron beam of a few GeV. The measured detection efficiency is shown by figure 7 as a function of the coolant temperature. The values displayed refer to two individual sensors and to their sub-arrays featuring pixels with 20, 30 and 40 μm pitch.

The figure shows that a detection efficiency of ~ 99.8 % is achievable for a coolant temperature of up to 40°C. This satisfactory behaviour remains however still to be confirmed after irradiation, with sensors made radiation tolerant and integrating signal processing micro-circuits, features which tend to degrade the S/N value.

3.1.2 Effect of noisy pixels on the data flow

The least significant bit of the ADCs integrated in the sensors will be used to select those pixels which were hit by a particle, and suppress all other signals. This is mandatory to keep the data

[3] Cold Baryonic Matter experiment at FAIR, GSI (Darmstadt)

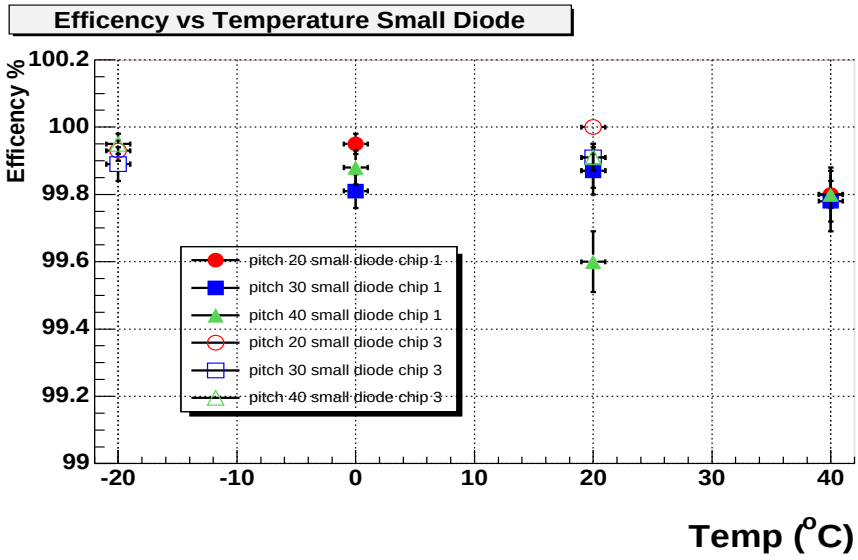


Figure 7: Data collected at DESY with two MIMOSA-9 sensors mounted on a Si-strip telescope. The detection efficiency for beam electrons is displayed as a function of the coolant temperrature for pitch values of 20, 30 and 40 μm.

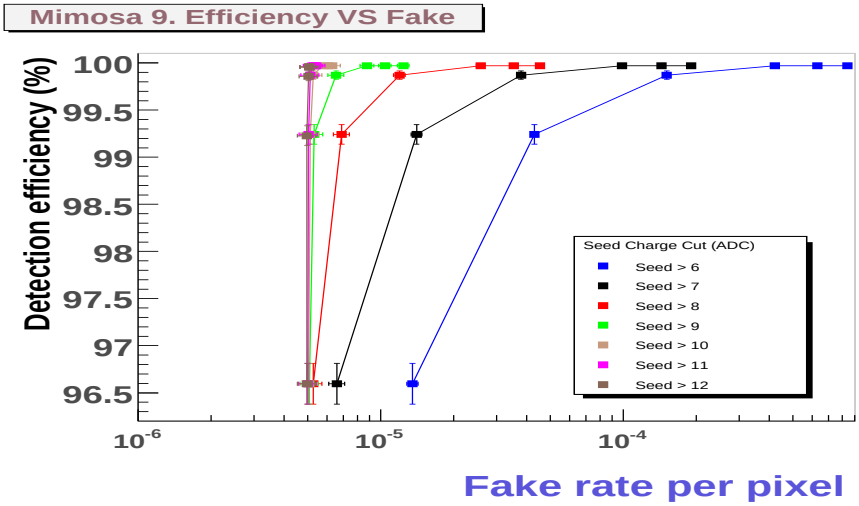


Figure 8: MIMOSA-9 beam test data. Correlation between the detection efficiency and the noisy pixel rate as a function of cluster charge threshold. Clusters are selected by applying separately a cut on the seed pixel charge and on the total charge of the 8 pixels surrounding the seed pixel. The former cut is varied from 6 ADC units (equivalent to $\sim$ 4 times the pixel noise) to 12 units by steps of 1 unit. Fore each of these 7 cut values, 6 different values of the cut on the crown charge are considered, amounting to to 0, 3, 4, 7, 9 and 13 ADC units (from right to left along each series of measured points). The lowest value of the "fake rate" is saturated due to the limited sensitivity of the measurements.

rate delivered by the sensors compatible with the data acquisition system. The optimal value of the threshold is to be found, which is sufficiently low to preserve the detection efficiency and high enough to reject efficiently noisy pixels.

The effect of noisy pixels was investigated with the beam test data collected with MIMOSA-9 at DESY. One of the motivations of the study was to find out whether the data flow of future sensors equipped with zero suppression micro-circuits would be influenced by noisy pixels delivering a fake signal above the discriminating threshold integrated at the column ends.

The results are illustrated by figure 8. It displays the detection efficiency as a function of the fraction of pixels delivering a fake signal coming from the electronic noise. The correlation between both parameters is displayed for various values of the cluster selection parameters. The latter are the seed charge and the sum of the charges of the crown of pixels surrounding the seed pixel. Measurements performed with the same cut value on the seed charge (varied from 6 to 12 ADC units) are connected with a line. They differ by the cut on the crown charge, varied from 0 to 13 ADC units.

One observes that a detection efficiency of $\gtrsim 99.9$ % is rather easily obtained without letting the fake rate exceed $\sim 10^{-4}$. Since the beamstrahlung rate is expected to fire a fractions of pixels ranging from $\sim 10^{-3}$ to several per-cent of the pixels (depending on the layer), one can conclude that noisy pixels should not increase significantly the data flow delivered by the sensors in any of the detector layers. The results need, of course, to be confirmed with the final sensors integrating all signal processing micro-circuits and fabricated with in their own industrial process.

3.1.3 Qualifying the "20 μm" option

Prototyping for STAR an EUDET triggered an engineering run in 2006, in order to manufacture real size sensors (i.e. $\sim$ 0.5 - 2. cm^2 large) to be used for detector demonstrators.

One of the goals of this run was to assess the fabrication yield; another objective was to characterise a new option of the process, featuring a thicker epitaxial layer (called "20 μm" epitaxy).

Two wafers, one with the standard "14 μm" epitaxy and one with the new "20 μm" option, were delivered in Octobre 2006. A fabrication failure was discovered, which affects several of the chips hosted on the reticle at different degrees, depending on their design. The founder recognised its mistake, and a new fabrication was launched early in 2007. Two wafers were delivered in April, which are currently being characterised.

The failure in the 2006 production did not forbid testing some of the sensors, which were only affected by a 10–20 % increase of the pixel noise and by the necessity to steer them with particularly unsual values of the steering parameters. The conditions were, in particular, good enough to allow a first comparison between the "20 μm" and the "14 μm" epitaxy options. A few sensors were taken from each of the wafers and illuminated with an ^{55}Fe source. Figure 9 compares the CCE observed for both options with the MIMOSA-20 prototype[4] developed for the STAR experiment.

The distributions obtained for the two types of epitaxy are quite different. The charge collected with the "14 μm" epitaxy sensor exhibits distributions which are actually very close to those obtained with previous chips fabricated in the same technology (MIMOSA-9, -11, -14,

[4]640 x 320 ionising radiation tolerant pixels with 30 μm pitch, active area $\sim$ 1x2 cm^2, integrated JTAG steering logic.

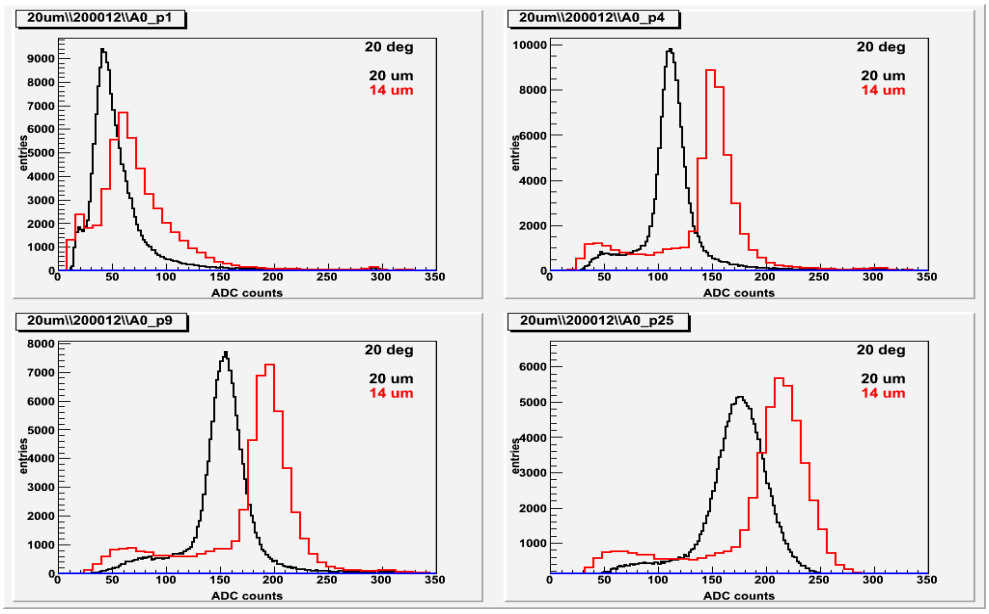


Figure 9: MIMOSA-20 sensors taken from the "14 μm" epitaxy (red curve) and "20 μm" epitaxy (black curve) wafers, illuminated with an ^{55}Fe source. The charge collected is shown for the seed pixel (top left), the 2x2 cluster made of the pixels sharing most of the charge (top right), as well as the 3x3 (bottom left) and the 5x5 (bottom right) clusters centered on the seed pixel.

-15). On the contrary, the charge collected with the "20 μm" epitaxy sensor is significantly smaller (in the order of 30 %). Copies of three other sensors (MIMOSA-16, -17 and -18) coming from the two different wafers were tested in the same way. The charge distributions of the "20 μm" epitaxy option was systematically shifted towards values below those of the distributions obtained with the "14 μm" epitaxy.

Summarising, there is evidence that the signal electrons produced with "20 μm" epitaxy are not collected as efficiently as those produced with "14 μm" epitaxy, i.e. they seem to recombine before reaching a sensing diode. The next steps of the development will therefore, a priori, rely on the standard "14 μm" epitaxy process.

3.2 New generation of real size sensors

The engineering run provides more than 50 copies (reticles) per wafer of each different sensor hosted a the reticle. Some of the real size sensors (MIMOSA-20, -17, -18) will be mounted on detector demonstrators and operated in real experimental conditions. This new generation of large sensors differs from the previous one (MIMOSA-5) mainly on the following aspects :

- its read-out frequency is one or two orders of magnitude higher (about thousand frames per second);
- its pixels are ionising radiation tolerant;
- the sensors can be operated at room temperature (no cooling required);
- most of them are equipped with an integrated JTAG steering logic.

The gain in experience with these devices is expected to provide useful input to the next steps of the R&D for the ILC.

Before dicing the sensors of the 2007 production, probe station tests will be performed in ordre to estimate the fabrication yield. This evaluation is currently under way.

It is foreseen to buy several additionnal wafers of the second (and perhaps also first) production batch from the foundry. Some of them will be used for thinning studies, as mentionned in section 5.

3.3 Exploration of other fabrication processes

The AMS-0.35 OPTO process is well adapted to several, mid-term applications and provides a relatively economical framework to the R&D for the ILC vertex detector. But it is not foreseen to be used for the final fabrication of the sensors developed for the ILC. This has several reasons:

- the availability of the process in the next decade;
- the too restricted number of metal layers (only 4, while at least 6 are needed);
- the relatively large feature size.

The search for new fabrication processes is therefore a permanent activity, which aims to find a process providing a feature size $< 0.2\ \mu m$, at least 6 metal layers, a sufficient transistor polarisation voltage, an epitaxial layer of at least 10 μm, etc. A privileged contact with the founder, especially with its designer teams, is a very valuable bonus when chosing a fabrication process.

In 2006, a new fabrication process was explored, triggered by the development of an imaging device. It is BiCMOS technology provided by S.T.Microelectronics with a 0.25 μm feature size. A prototype (called MIMOSA-21) was designed in Autumn, in close contact with the founder expert team for this fabrication process. This allowed to learn details about the doping profile and to simulate them with the 3D software ISE-TCAD. The first test results of MIMOSA-21, confirm quite well the predictions of these simulations. This contact with the founder, which allows to better understand and control the behavious of the sensor, may thus open up for attractive perspectives in terms of future technologies with smaller feature size.

4 Operation at room temperature and radiation tolerance

The integrated radiation dose which the sensors are required to tolerate is almost fully determined by the rate of beamstrahlung $e^{\pm}_{BS}$. This statement is definitely true for ionising radiation; it applies also in a large extend to non-ionising radiation, as the fluence related to the neutron gas propagating inside the apparatus is at least one ordre of magnitude below the fluence associated to the beamstrahlung $e^{\pm}$.

High radiation doses have generally two kinds of consequences on the sensor performances: first, they tend to increase the leakage current, which enhances the noise; second, they introduce intersticial traps, and thus reduce the charge collection efficiency due to electron-hole recombination. The increase of noise may be marginal for the short read-out times relevant for the ILC (i.e. 25 - 150 μs), but a cautious pixel design may still be useful as it may allow running at room temperature, a condition which allows for reduced material budget. The appearance of traps can be more disturbing, especially for CMOS sensors, where the signal

electrons diffuse thermally in the epitaxial layer until reaching a sensing diode. Running at a temperature close to 0°C is known to improve substantially the sensor tolerance, but it may conflict with the goal to squeeze the material budget.

4.1 Ionising radiation

The ionising radiation dose which the sensors are supposed to tolerate has been estimated to O(100) kRad per year, accounting for a safety factor of 3 w.r.t. to the simulated $e^{\pm}$ rate [3].

The tolerance to ionising radiation was significantly improved by modifying the pixel design in order to reduce the increase of the leakage current consecutive to large integrated dose exposures. Arrays of MIMOSA-11 and -15 were designed for this purpose with pixels where the thick oxide near the sensing diode was removed and a P+ guard ring was implemented around the diode. The tolerance of MIMOSA-11 was studied in Spring 2005 with an ^{55}Fe source for values of the integrated dose delivered by a 10 keV X-Ray source ranging up to 1 MRad.

Figure 10 shows how the residual noise, measured with standard pixels and with radiation tolerant ones, varies as a function of the integration time at different temperatures, after exposure to an integrated dose of 500 kRad (i.e. several times the upper limit on the yearly dose mentioned above).

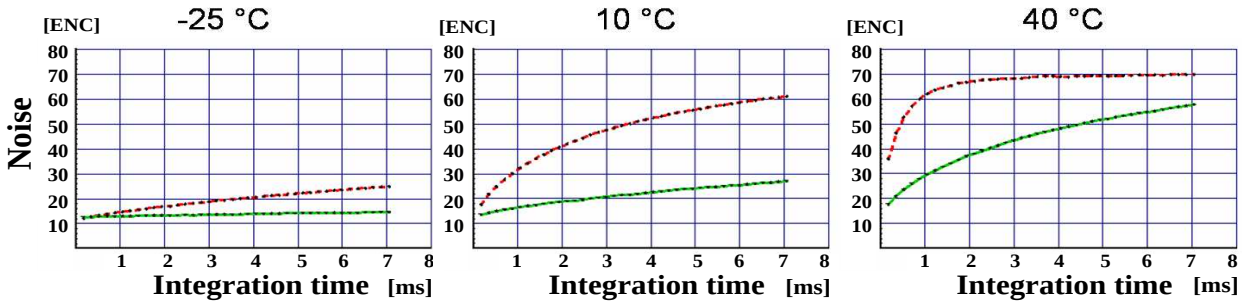


Figure 10: MIMOSA-11 tests with an ^{55}Fe source after exposure to an integrated dose of 500 kRad. The residual noise is shown as a function of the integration time for pixels designed without special care w.r.t. radiation damage (upper dotted line) and for radiation tolerant pixels (lower dotted line). The measurements are displayed for three different coolant temperatures (- 25°C, + 10°C, + 40°C).

One observes that, contrary to the standard pixel, the radiation tolerant structure stands 500 kRad at room temperature (i.e. the noise remains well below 20 e^-ENC) for the range of integration time values foreseen at the ILC (typically 25 to 150 μs).

These radiation tolerance studies were extended with the prototype MIMOSA-15, which features pixels designed with the same architecture modifications as MIMOSA-11, slightly optimised in terms of noise and CCE. The radiation tolerance of MIMOSA-15 sensors was assessed in 2006 on a $\sim$ 5 GeV/c e^- beam at DESY. One among the chips tested had been exposed to an integrated dose of $\sim$ 1 MRad (obtained with a 10 keV X-Ray source). The results of the measurement are summarised in table 4.

One observes that the irradiated sensor still exhibits a S/N ratio of $\sim$ 19, to be compared to $\sim$ 28 before irradiation, and a detection efficiency of $\sim$ 99.9 % at a coolant temperature

Integrated Dose	Noise	S/N (MPV)	Detection Efficiency
0	9.0 ± 1.1	27.8 ± 0.5	100 %
1 MRad	10.7 ± 0.9	19.5 ± 0.2	99.96 ± 0.04 %

Table 4: Tests of MIMOSA-15 (30 μm pitch) with a $\sim$ 5 GeV e^- beam at DESY. Noise, S/N and detection efficiency are displayed for a non-irradiated sensor and for another one irradiated with 1 MRad of 10 keV X-Rays. The coolant temperature was -20°C.

of -20°C (with 180 μs integration time). These performances validate the pixel architecture implemented against parasitic leakage current generated by ionising radiation. These results need still to be confirmed at room temperature, but no substantial change is expected for the short integration times under consideration.

4.2 Non-ionising radiation

Bulk damage is expected to come mainly from the neutron gas and from the beamstrahlung $e^{\pm}$. While the fluence corresponding to the neutron gas rate is $\lesssim 10^{10}$ n_{eq} /cm^2, that due to beamstrahlung is about one ordre of magnitude more (assuming a NIEL factor of 1/30 for the $e^{\pm}$ in the relevant energy range). As a consequence, one may consider a fluence of $\lesssim 10^{12}$ n_{eq} /cm^2 as a safe requirement for the sensor tolerance.

The radiation tolerance may be quite different from one fabrication process to another. The first sensor fabricated in the AMS-0.35 OPTO technology to be tested against non-ionising radiation was MIMOSA-9, which was exposed to $\sim$ 1 MeV neutrons in Dubna, and consecutively tested on the DESY electron beam. It was observed that even for a fluence of $\sim 10^{12} n_{eq}/cm^2$, the sensor still exhibited a S/N ratio of $\sim$ 19, and a detection efficiency of $\sim$ 99.5 % at a coolant temperature of -20°C [2].

The study was completed with the MIMOSA-15 prototype, which was exposed to fluences of up to $\sim 6{\cdot}10^{12} n_{eq}/cm^2$. Figure 11 summarises the results. It shows the detection efficiency as a function of the fluence. One observes that a sensor exposed to $\sim 2{\cdot}10^{12} n_{eq}/cm^2$ still exhibits a detection efficiency above 99 % at a coolant temperature of -20°C. For a fluence of $\sim 6{\cdot}10^{12} n_{eq}/cm^2$, the detection efficiency drops to $\sim$ 80 %. The next steps of this study will consist in assessing the sensor performances at room temperature.

Beyond the tests of sensors with analog output and no signal conditionning in the pixels, it is foreseen to also test the sensors providing a digital output. In this case, the noise before irradiation is slightly larger (12 - 15 e^- ENC). The study needs therefore to show up to which fluence the S/N is still high enough, for various operating temperatures.

5 Other results

Besides the activities focussing on the sensor design, progress was also achieved on other issues. Some significant steps were in particular made on assessing the thinning procedure and on refining the vertex detector geometry taking best advantage of CMOS sensors. Progress was also achieved in cycling the steering power in ordre to reduce the average power consumption.

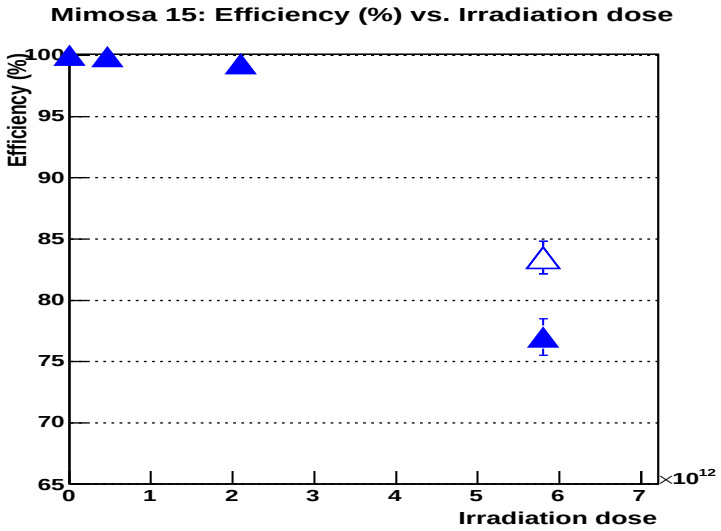


Figure 11: Tests of MIMOSA-15 with a $\sim$ 5 GeV e^- beam at DESY. Preliminary values of the detection efficiency of sensors exposed to various values of the fluence.

5.1 Industrial thinning

Thinning trials were made at several occasions with sensors of various sizes. One of the questions addressed was whether individual sensors, even smaller than a reticle, could be thinned down reliably. The trials showed that the thinning of individual sensors tends to generate a non uniform thickness (thickness variations of a factor of 2 over the sensor surface were measured). Nevertheless, MIMOSA-14 sensors (25 mm^2 large) seem to have been successfuly thinned to 50 $\pm$ 5 μm. They were mounted on prototype ladders and installed recently in the STAR experiment for tests.

Next, the recently fabricated 1 x 2 cm^2 MIMOSA-20 sensors will be thinned to $\sim$ 50 μm. They are foreseen to be consecutively mounted on new prototype ladders in perspective of tests inside the STAR experiment.

5.2 Vertex detector geometry

One of the most attractive aspects of CMOS sensors is the flexibility of their design. This may be exploited to reduce the power dissipation and improve the read-out speed, as well as to reduce slightly the material budget.

This specific aspect of a vertex detector based on the CMOS sensor technology was already discussed in the previous PRC report [2]. Since then, detailed studies were performed in order to evaluate the impact parameter resolution achievable with each geometry option considered.

The scenarios considered are summarised hereafter:

- **S1:** single point resolution varied from 2 μm in the inner most layer to 4 μm in the outer one, by steps of 0.5 μm per layer;
- **S2:** single point resolution varied from 2.5 μm in the inner most layer to 5 μm in the outer one, by steps of $\sim$ 0.6 μm per layer;
- **S3:** same as S2, but with double material budget: 0.2 % X_0/layer instead of 0.1 %;

- **S4:** single point resolution of 2.2 μm in the two inner layers and 3.3 μm in the outer ones.

The result of the study is summarised in table 5. The values shown are those obtained for the parameters a and b entering the usual expression of the impact parameter resolution[5]. They were fitted to the momentum resolution reconstructed for each scenario. Also shown are the values obtained with the geometry of the TESLA TDR and a single point resolution of 2.5 μm in each layer (made of 0.1 % X_0 equivalent material). This latter case is a reference to which the performances obtained with the CMOS sensor based geometry should be compared.

scenario	S1	S2	S3	S4	TDR
a (μm)	2.89 ± 0.02	3.59 ± 0.02	3.62 ± 0.02	3.23 ± 0.02	3.40 ± 0.02
b (μm)	8.7 ± 0.1	8.8 ± 0.1	10.4 ± 0.1	8.7 ± 0.1	8.5 ± 0.1

Table 5: Values of the parameters a and b entering the expression of the impact parameter resolution, for various values of the pixel pitch (and two different layer thicknesses). The column called "TDR" stands for the TESLA TDR geometry with a constant single point resolution of 2.5 μm in each layer.

One observes that the resolutions obtained with the CMOS sensor based geometries compare very well with the reference one. Actually the study also showed that doubling the pitch in the outer layer increases the value of "a" only by about 5 %.

As far as the material budget is concerned, considering 0.2 % X_0/layer instead of 0.1 %, was motivated by the difference in challenge between the two target values. One observes that, even if the material budget happened to be 0.2 % X_0, the parameter "b" would not degrade dramatically, despite its increase by $\sim$ 20 % (assuming a 400 μm thick beryllium beam pipe). On the other hand, one should not allow for thicker layers.

5.3 Power cycling

The most recent estimates of the power dissipated by the full detector are of the ordre of 500 watts. In ordre to keep the material introduced by the cooling system at a moderate level, the plan is to switch off most of the sensor steering power inbetween bunch trains.

The relevant time scale for switching the sensors on and off is typically 1 ms. The possibility to cycle a CMOS sensor at such a frequency was investigated with the MIMOSA-5 sensor, which features a $\sim$ 3.5 cm^2 sensitive area composed of 1 million of pixels. This sensor was fabricated several years ago and was not aimed to run at high frequency. It is therefore not at all optimised for such an exercise, but should nevertheless allow to spot fundamental problems in cycling a sensor at the relevant frequencies.

The measurements performed show that 1.2 ms after having turned on the power of the output buffers, the performance of the sensor has already come back to a stable behaviour. The consequence was a reduction of the total sensor power dissipation by a factor of 8, assuming a machine duty cycle of 1/200.

Future sensor designs will include power saving features which are expected to still allow improving the reduction factor above by a on ordre of magnitude. It remains now to prove

[5] $\sigma_{sp} = a \oplus b/(p \cdot sin^{3/2}\theta)$, with the following requirements: a < 5 μm and b < 10 μm.

that the functionnalities of the sensors remain unaffected by the alternate switching mode, i.e. that no reprogramming of the sensors will be required within short periods.

6 Plans until 2009-2010

The next steps of the R&D will aim for real size sensors with digital output and integrated data compression logic. These are a 1x2 cm^2 pixel matrix with $\lesssim 100\ \mu s$ read-out time for the EUDET telescope, and a 2x2 cm^2 sensor with $\lesssim 200\ \mu s$ read-out time for the STAR HFT. Both sensors should be fabricated by 2009. They will however not incorporate ADCs because the required single point resolution ($\sim 5\ \mu m$) can be accommodated with a binary encoding of the charge (i.e. raw discriminator output). The pixel size is however limited to $\sim 18\ \mu m$.

These sensors will thus not yet integrate all the functionnalities needed for running at the ILC. They will however provide important milestones on the way to their achievement. Among the most significant obstacles these two sensors offer to overcome, there are several aspects of a fast running architecture over a large area, based on a large number of rows and columns (switches). Moreover, the sensors will be operated in real experimental conditions, which is expected to be very useful for this new technology. In particular, several issues related to system integration will be addressed within these projects.

6.1 Milestones until the final sensor

The milestones bridging the gap between the present most mature prototype (i.e. MIMOSA-16) and the final sensors for EUDET and STAR are summarised hereafter:

- Pixel design:
  - adapt the existing pixel architectures to a smaller pitch ($\sim 18\ \mu m$ instead of $25\ \mu m$);
  - optimise the sensing diode dimensions in ordre to obtain simultaneously sufficient CCE (which calls for a large diode) and sufficient gain (which calls for a small diode).
- Column read-out architecture:
  - adapt the existing discriminating logic to the smaller pitch;
  - integrate data compression micro-circuits and output memories.
- Row and pixel steering (consequence of a large active area):
  - adapt the pixel steering inside columns to the required read-out speed by reducing the capacitance loading due to the large number of switches inside each column;
  - adapt the row steering to their length (~ 2 cm).
- Sensor autonomy and testability:
  - integrate a programmable JTAG steering logic and bias DACs;
  - integrate the necessary DC voltage sources to emulate the column's output for independent mixed and digital logic testing (e.g. discriminators and zero suppression micro-circuits).

The R&D for the ILC requires some additionnal milestones, which reflect the more demanding requirements in terms of read-out speed, spatial resolution and the different time scale:

- replace the discriminators by ADCs at the column's ends;

- adapt the data compression logic to the higher data rate;
- adapt the pixel and column architectures to the pixel pitch of the inner layers ($\gtrsim 20\ \mu m$) and of the outer ones ($\gtrsim 30\ \mu m$);
- find and assess a fabrication process with a feature size $< 0.2\ \mu m$.

6.2 Chip fabrication schedule

The strategy followed to address the milestones listed in the previous section for EUDET and STAR relies essentially on two prototypes, called MIMOSA-22 and (provisionally) MIMOSA-22+. Their main features are summarised hereafter.

6.2.1 Main features of MIMOSA-22

The pitch retained for EUDET and STAR is as small as $\sim 18\ \mu m$, in order to meet the spatial resolution requirements with binary charge encoding (i.e. no ADC).

MIMOSA-22 will address the question of adapting the architecture of MIMOSA-16 to this pitch. It will also deal with the optimisation of the sensing diode surface ($\sim$ 10–15 μm^2), and with the problem of steering long columns ($\lesssim 1$ cm) at high speed. It will be composed of 64 columns with digital output and 8 columns with analog output (for test purposes). The number of rows will lie inbetween 500 and 600. The active surface will be subdivided in several sub-arrays of typically 64 rows, each featuring different pixels. The ambitionned read-out speed is the nominal value fo $\sim 100\ \mu s$.

The design of the prototype is well advanced and its submission is scheduled for the end of Septembre 2007.

6.2.2 Main features of MIMOSA-22+

The main motivation for MIMOSA-22+ is to complement MIMOSA-22 with the integrated zero suppression logic developed through the SUZE prototype (see section 2.3). It will therefore feature at least 256 columns with digital output (i.e. 4 blocks of 64 columns). Based on the test results of MIMOSA-22, the sensor will host more mature pixel architectures and should therefore not be subdivided in more than 2 sub-arrays with different pixels. It is not clear whether columns with analog output will still be necessary for tests.

This final EUDET prototype should be submitted to foundry in Spring 2008. The fabrication of the final sensor, which would mainly differ from MIMOSA-22+ by the number of columns, all with discriminated output ($\sim$ 1088 instead of 256), would take place late in 2008 or early in 2009.

The sensor required for the STAR HFT has twice the surface of the EUDET prototype. It may therefore require and alternative version of MIMOSA-22+, featuring 1088 rows instead of 544. It would be manufactured together with MIMOSA-22+, making the case for an engineering run allowing to fabricate other sensors on the same reticle. The final sensor for the STAR HFT may then be fabricated in the second half of 2009.

6.2.3 Additionnal prototyping for the ILC

While developing the sensors for EUDET and STAR, the ADC needed for the ILC will mature through additionnal tests and prototypes fabricated in 2007. It is likely that the first ADC

matching all requirements will be ready early in 2008. The data compression logic of the SUZE prototype will also be adapted to higher data flow with a new prototype (SUZE-02) in 2008.

The next step will consist in adapting MIMOSA-16 to the pitch of the inner most layer ($20 - 22\ \mu m$) and in replacing the discriminators ending the columns with ADCs. The design of this prototype could be ready for fabrication by the end of Spring 2008. In case of success, the development could carry on with a new prototype integrating the data compression logic of SUZE-02 and featuring the number of rows foreseen in the inner most layer (between 256 and 320) and at least 128 columns.

In this scenario, the final prototype could be fabricated by 2010. Meanwhile however, a new fabrication technology should come up, which would need some additionnal prototyping.

7 Summary

Substantial effort was invested during the last two years in the most demanding goal of the R&D on CMOS sensors for the ILC vertex detector: a fast architecture suited to a data rate accounting for conservative safety margins w.r.t. the nominal Monte-Carlo simulations. Important progress was achieved: a fast, column parallel, prototype (MIMOSA-8) with integrated signal discrimination was validated with particle beams, and translated into a manufacturing process (AMS 0.35 OPTO) featuring a thicker epitaxial layer. This second prototype, called MIMOSA-16, exhibits however a poor CCE for the pixels equipped with a small sensing diode in ordre to maximise the gain. One of the sub-arrays composing the sensor did not suffer from this weakness, showing that the problem can be solved.

The development of fast ADCs has also progressed well, and a mature ADC seems to be achievable for early 2008. The first sensor equipped with an ADC should thus be fabricated next year.

A first prototype (SUZE-01) featuring a zero suppression logic and output memories is being designed, adapted to the STAR and EUDET requirements, which are less demanding than the ILC ones. A second generation of this chip, adapted to the ILC requirements, is foreseen to be fabricated in 2008. It may be integrated in a fast and medium size sensor equipped with ADCs by 2009.

The EUDET and STAR projects will lead to devices made of MIMOSA sensors operated in experimental conditions starting from 2007. Running the sensors in real conditions and developing dedicated fast, column parallel sensors for these applications will be very beneficial to the R&D for the ILC vertex detector, including system integration aspects.

The sensors devoted to EUDET and STAR will be fabricated in the AMS 0.35 OPTO technology, which is also the baseline process of the R&D for the ILC. This technology was further studied in the last two years. In particular, its tolerance to ionising and non-ionising radiation was evaluated and found well sufficient to cope with the most pessimistic pronostics for the integrated doses expected in the ILC vertex detector.

Close to ten sensors have now been fabricated in this technology, which offers since recently a thick epitaxial layer option, labelled "$20\ \mu m$". The latter was studied with several sensors fabricated via an engineering run. It came out that this option does not provide a better S/N ratio than the standard ("$14\ \mu m$") technology. The latter will thus remain the baseline. It has however a weakness, which has drawbacks for certain fast pixel architectures: a high charge-to-voltage gain inside the pixel calls for a small sensing diode, but small diodes were shown to have a very poor CCE. Sizeable diodes are therefore required, at the expense of the

gain. The necessary optimisation of the pixel architecture is part of the next steps of the R&D.

A relatively detailed list of milestones and plan for the chip submissions until 2010 has been established. It includes the search for a new fabrication technology based on a feature size shorter than 0.2 μm, which would still be available in the next decade. The AMS 0.18 OPTO technology, which has been announced for 2007/2008, is a favoured candidate.

CMOS sensors don't need to have the same features for all detector layers. One of the attractive perspectives of this flexibility concerns the pixel pitch. The latter may actually be optimised for each of the 5 detector layers (e.g. 20, 25, 30, 35 and 40 μm when going from the inner most layer towards the external ones). This modulation takes advantage from the fact that the resolution requirement is not as stringent in the outer layers as in the inner ones. Enlarging the pitch of the outer layers profits to the power dissipation and to the read-out speed. One may actually restrict oneself to two different pitch values: $20 - 22$ μm in the two inner most layers and $30 - 33$ μm in the three outer layers. The consequence of various pitch values on the impact resolution was evaluated, as well as the consequence of doubling the material budget in the layers. To perform the study, a substantially more realistic description of the vertex detector geometry, which includes individual ladders, was developed and installed in the general LDC software. It came out from the study that all the geometries considered lead to an impact parameter resolution satisfying the ILC requirement. This validates the geometries based on a variable pitch.

Overall, from the present status of the R&D, one can conclude that the ambitionned requirements, which are substantialy more severe in terms of read-out speed and radiation tolerance than in the TESLA TDR, seem more or less within reach. The question remains, however, of the adapted fabrication process for the final sensors, which cannot be AMS 0.35 OPTO, and should be chosen by the end of the decade. Besides this open question, the issue of system integration is still not taken over by a group of experts. This situation needs to evolve within relatively short time if a complete ladder has to be fabricated by $\sim$ 2010.

References

[1] R.Turchetta et al., Nucl. Inst. Meth. A458, 677 (2001);

[2] M.Winter et al., PRC report of May 2005;

[3] M.Winter et al.,
Proc. of International Linear Collider Workshop, Stanford (USA), March 2005, and
Proc. of International Linear Collider Workshop, Bangalore (India)), March 2006;

[4] J.Thomas, talk at Int. Conf. on Strangeness in Quark Matter, Los Angeles (USA), March 2006;

[5] EUDET home page: http://www-zeus.desy.de/ haas/eudet-jra1/

[6] TESLA Technical Design Report;

[7] W.Dulinski et al., *Optimization of tracking performance of CMOS monolithic active pixel sensors*, IEEE-Transactions on Nuclear Science (2007), 54-284;
A.Besson et al., *CMOS sensors for the vertex detector of the future international linear collider* , Nucl. Inst. Meth. A572 (2007) 300;
IPHC web site : *http://iphc.in2p3.fr/Cmos.html*;

[8] Y. Degerli et al., IEEE Trans. on Nucl. Science, Vol.52, n6, December 2005, pp. 3186-3193

APPENDIX A: Summary of fabricated MIMOSA sensors mentionned in the report

MIMOSA-8	fabrication	2003 - TSMC-0.25 techno. - epitaxy thickness $< 7\ \mu m$
	geometry	25 μm pitch - 128 rows - 24/8 col. with digital/analog output - 4 sub-arrays with different pixels
	features	column parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
MIMOSA-9	fabrication	2003 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim 11\ \mu m$ (also with "high-res" substrate without epitaxy)
	geometry	20, 30 & 40 μm pitch - various pixel architectures
	features	technology exploration - analog output - serial read-out
MIMOSA-11	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim 11\ \mu m$
	geometry	20 & 30 μm pitch - 106x106 pixels - 4 sub-arrays
	features	analog output - serial read-out
MIMOSA-14	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim 11\ \mu m$
	geometry	30 μm pitch - 2 groups of 64x128 pixels
	features	STAR prototype - ionising rad. tol. pixels - analog output - serial read-out
MIMOSA-15	fabrication	2005 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim 11\ \mu m$
	geometry	20 & 30 μm pitch - 4 sub-arrays with various pixels
	features	non-ionising rad.tol. pixels - analog output - serial read-out
MIMOSA-16	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	25 μm pitch - 128 rows - 24/8 col. with digital/analog output - 4 sub-arrays with different pixels
	features	column parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\gtrsim$ 6 MHz
MIMOSA-17	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	30 μm pitch - 4 groups of 64x256 pixels
	features	EUDET demonstrator - 4 analog outputs - serial read-out inside each group
MIMOSA-18	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	10 μm pitch - 512x512 pixels
	features	EUDET sensor - sub-micron resolution - analog output - serial read-out inside each group
MIMOSA-20	fabrication	2006/7 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 & 15 μm
	geometry	30 μm pitch - ionising rad.tol.pixels - 2 groups of 320x320 pixels
	features	STAR demonstrator (final prototype) - 2 analog outputs - serial read-out inside each group
MIMOSA-21	fabrication	2006 - STM-0.25 BICMOS techno. - sensitive volume includes "high-res" substrate
	geometry	128x192 pixels with 10 μm pitch - 64x96 pixels with 20 μm pitch
	features	beta-imager - analog outputs - serial read-out

APPENDIX B: Sensors and micro-circuits to be fabricated $\leq$ 2010

MIMOSA-22	fabrication	2007 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for EUDET	geometry	18 μm pitch - 500-600 rows - 64/8 col. with digital/analog output - 6-8 sub-arrays with different pixels
and STAR)	features	col. parallel read-out - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
SUZE-01	fabrication	2007 - AMS-0.35 OPTO techno. - no epitaxy
(for EUDET & STAR)	features	zero suppression logic & memories - specific to EUDET & STAR
MIMOSA-22+E	fabrication	2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for EUDET)	geometry	18 μm pitch - 500-600 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. zero suppression - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
MIMOSA-22+S	fabrication	2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for STAR)	geometry	18 μm pitch - 1088 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. zero suppression - clock frequency $\geq$ 100 MHz - row read-out frequency $\sim$ 6 MHz
MIMOSA-22++E	fabrication	2008/2009 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for EUDET)	geometry	18 μm pitch - 500-600 rows - 1088 col. with digital output
	features	final chip equipping telescope - col. parallel read-out with integ. zero suppression - read-out time $\sim$ 100 μs
MIMOSA-22++S	fabrication	2009 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for STAR)	geometry	18 μm pitch - 1088 rows - 1088 col. with digital output
	features	final chip for HFT col. parallel read-out with integ. 0 supp. - read-out time $\lesssim$ 200 μs
ADC	fabrication	2007/2008 - AMS-0.35 OPTO techno. - no epitaxy
(for ILC)	features	various architectures - 4 or 5 bits - $\geq$ 8 channels - specif. for EUDET & STAR
MIMOSA16+	fabrication	2008 - AMS-0.35 OPTO techno. - epitaxy thickness $\sim$ 11 μm
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 64 col. with digital output - $\geq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. ADC
SUZE-02	fabrication	2008 - AMS-0.35 OPTO techno. - no epitaxy
(for ILC)	features	0 suppression micro-circuits & memories - specific to ILC
MIMOSA-X	fabrication	2008/2009 - various technologies with $<$ 0.2 μm feature size
ADC-X	fabrication	2008/2009 - various technologies with $<$ 0.2 μm feature size
SUZE-X	fabrication	2008/2009 - selected technology with $<$ 0.2 μm feature size
MIMOSA16++	fabrication	2009 - AMS-0.35 OPTO techno.? - epitaxy thickness $\sim$ 11 μm ?
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	col. parallel read-out with integ. ADC & zero suppression
MIMOSA16+++	fabrication	2010 - technology ?
(for ILC)	geometry	20-22 μm pitch - 256-320 rows - $\geq$ 256 col. with digital output - $\leq$ 2 sub-arrays with different pixels
	features	final sensor - col. parallel read-out with integ. ADC & 0 suppression